# ADP3334—SPECIFICATIONS[1, 2, 3] ($V_{IN}$ = 6.0 V, $C_{IN}$ = $C_{OUT}$ = 1.0 µF, $T_A$ = –40°C to +85°C, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT | | | | | | |
| Voltage Accuracy[4] | $V_{OUT}$ | $V_{IN}$ = $V_{OUT(NOM)}$ + 0.4 V to 11 V<br>$I_L$ = 0.1 mA to 500 mA<br>$T_A$ = 25°C | –0.9 | | +0.9 | % |
| | | $V_{IN}$ = $V_{OUT(NOM)}$ + 0.4 V to 11 V<br>$I_L$ = 0.1 mA to 500 mA<br>$T_A$ = 85°C | –1.8 | | +1.8 | % |
| | | $V_{IN}$ = $V_{OUT(NOM)}$ + 0.4 V to 11 V<br>$I_L$ = 0.1 mA to 500 mA<br>$T_J$ = 150°C | –2.3 | | +2.3 | % |
| Line Regulation[4] | | $V_{IN}$ = $V_{OUT(NOM)}$ + 0.4 V to 11 V<br>$I_L$ = 0.1 mA<br>$T_A$ = 25°C | | 0.04 | | mV/V |
| Load Regulation | | $I_L$ = 0.1 mA to 500 mA<br>$T_A$ = 25°C | | 0.04 | | mV/mA |
| Dropout Voltage | $V_{DROP}$ | $V_{OUT}$ = 98% of $V_{OUT(NOM)}$ | | | | |
| | | $I_L$ = 500 mA | | 200 | 400 | mV |
| | | $I_L$ = 300 mA | | 140 | 250 | mV |
| | | $I_L$ = 100 mA | | 60 | 140 | mV |
| | | $I_L$ = 1 mA | | 10 | | mV |
| Peak Load Current | $I_{LDPK}$ | $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V | | 800 | | mA |
| Output Noise | $V_{NOISE}$ | f = 10 Hz–100 kHz, $C_L$ = 10 µF<br>$I_L$ = 500 mA, $C_{NR}$ = 10 nF | | 27 | | µV rms |
| | | f = 10 Hz–100 kHz, $C_L$ = 10 µF<br>$I_L$ = 500 mA, $C_{NR}$ = 0 nF | | 45 | | µV rms |
| GROUND CURRENT[5] | | | | | | |
| In Regulation | $I_{GND}$ | $I_L$ = 500 mA | | 4.5 | 10 | mA |
| | | $I_L$ = 300 mA | | 2.6 | 6 | mA |
| | | $I_L$ = 50 mA | | 0.5 | 1.5 | mA |
| | | $I_L$ = 0.1 mA | | 90 | 130 | µA |
| In Dropout | $I_{GND}$ | $V_{IN}$ = $V_{OUT(NOM)}$ – 100 mV<br>$I_L$ = 0.1 mA | | 150 | 450 | µA |
| In Shutdown | $I_{GNDSD}$ | SD = 6 V, $V_{IN}$ = 11 V | | 0.9 | 3 | µA |
| SHUTDOWN | | | | | | |
| Threshold Voltage | $V_{THSD}$ | LDO OFF | 2.0 | | | V |
| | | LDO ON | | | 0.4 | V |
| SD Input Current | $I_{SD}$ | 0 ≤ SD ≤ 5 V | | 1.2 | 3 | µA |
| Output Current in Shutdown | $I_{OSD}$ | SD = 2 V, $V_{IN}$ = 11 V | | 0.01 | 5 | µA |

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods.

[2]Ambient temperature of 85°C corresponds to a junction temperature of 125°C under pulsed full load test conditions.

[3]Application stable with no load.

[4]$V_{IN}$ = 2.6 V to 11 V for $V_{OUT(NOM)}$ ≤ 2.2 V.

[5]Ground current includes current through external resistors.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATSINGS***

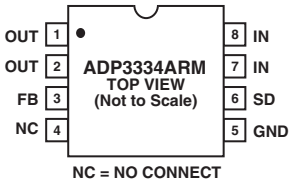
| | |
|---|---|
| Input Supply Voltage | –0.3 V to +16 V |
| Shutdown Input Voltage | –0.3 V to +16 V |
| Power Dissipation | Internally Limited |
| Operating Ambient Temperature Range | –40°C to +85°C |
| Operating Junction Temperature Range | –40°C to +150°C |
| Storage Temperature Range | –65°C to +150°C |
| $\theta_{JA}$ 2-Layer SOIC-8 | 122.3°C/W |
| $\theta_{JA}$ 4-Layer SOIC-8 | 86.6°C/W |
| $\theta_{JA}$ 2-Layer LFCSP-8 | 62°C/W |
| $\theta_{JA}$ 4-Layer LFCSP-8 | 48°C/W |
| $\theta_{JA}$ 2-Layer MSOP-8 | 220°C/W |
| $\theta_{JA}$ 4-Layer MSOP-8 | 158°C/W |
| Lead Temperature Range (Soldering 6 sec) | 300°C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

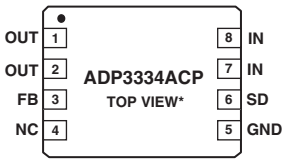
**PIN FUNCTION DESCRIPTIONS**

| Mnemonic | Function |
|---|---|
| GND | Ground Pin. |
| SD | Shutdown Control. Pulling this pin low turns on the regulator. |
| IN | Regulator Input. |
| OUT | Output. Bypass to ground with a 1.0 µF or larger capacitor. |
| FB | Feedback Input. FB should be connected to an external resistor divider that sets the output voltage. |
| NC | No Connection. |

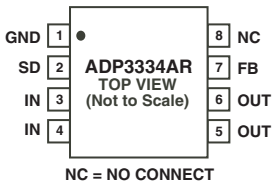
**PIN CONFIGURATIONS**



NC = NO CONNECT



*PINS UNDERSIDE
NC = NO CONNECT
The EPAD should be connected to VIN.

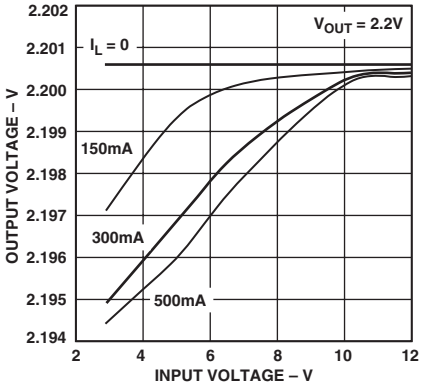


NC = NO CONNECT

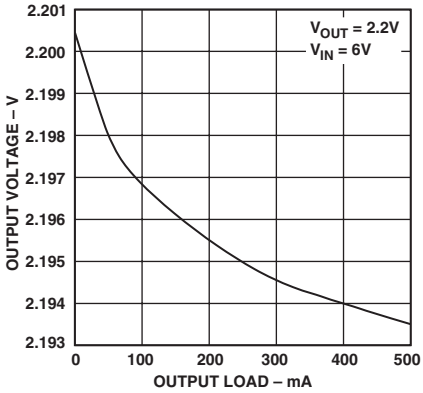
**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3334 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

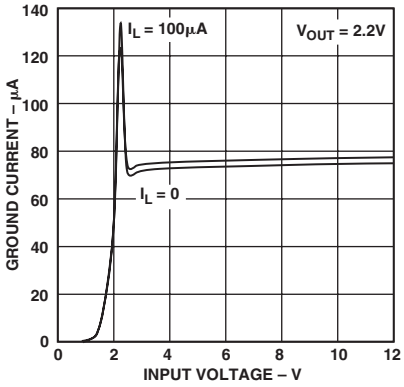
# ADP3334–Typical Performance Characteristics



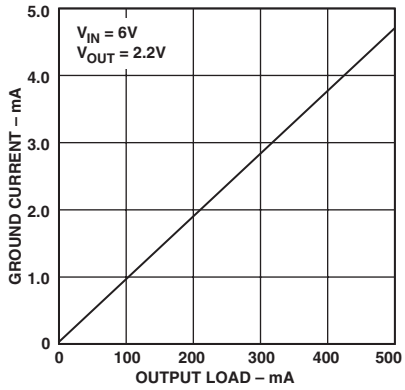

*TPC 1. Line Regulation Output Voltage vs. Supply Voltage*



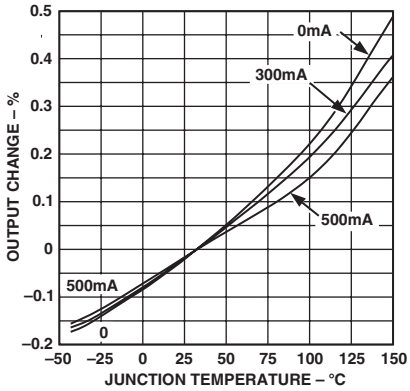

*TPC 2. Output Voltage vs. Load Current*



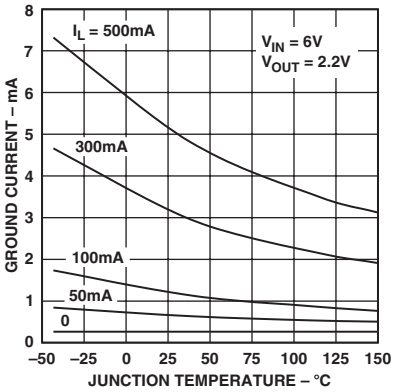

*TPC 3. Ground Current vs. Supply Voltage*



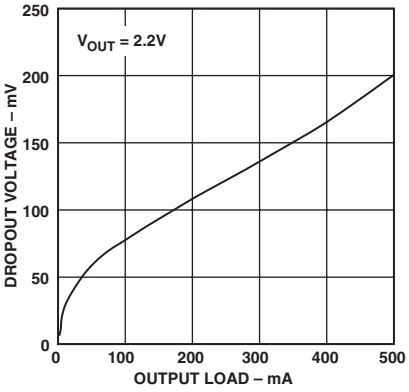

*TPC 4. Ground Current vs. Load Current*



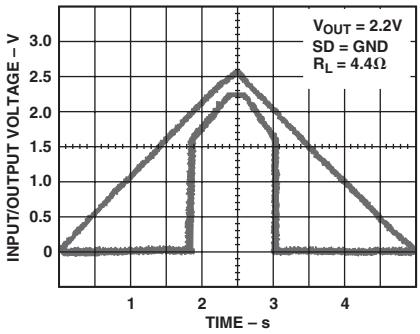

*TPC 5. Output Voltage Variation % vs. Junction Temperature*



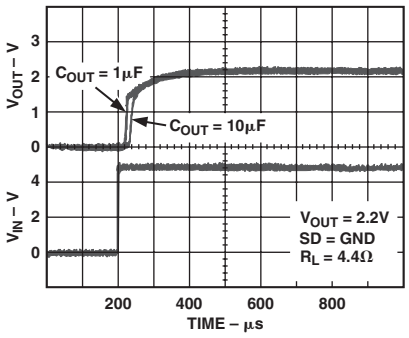

*TPC 6. Ground Current vs. Junction Temperature*



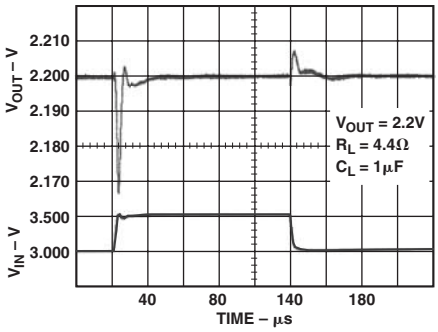

*TPC 7. Dropout Voltage vs. Output Current*



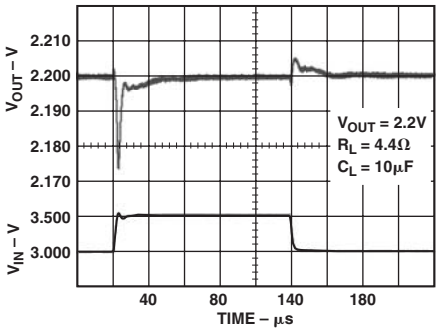

*TPC 8. Power-Up/Power-Down*



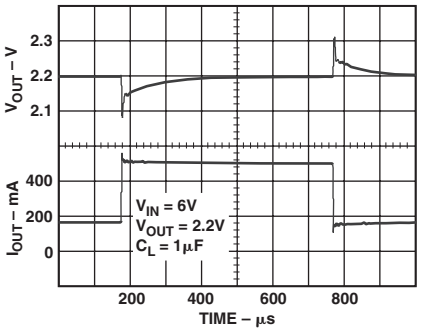

*TPC 9. Power-Up Response*



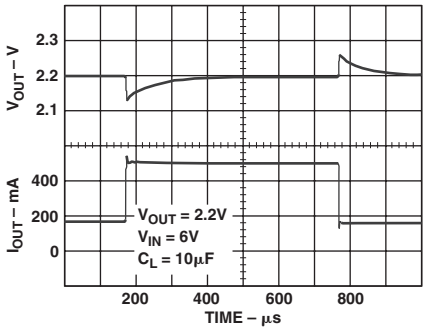

TPC 10. Line Transient Response



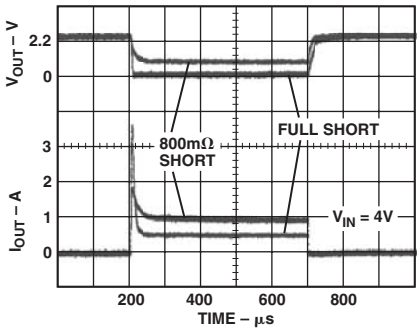

TPC 11. Line Transient Response



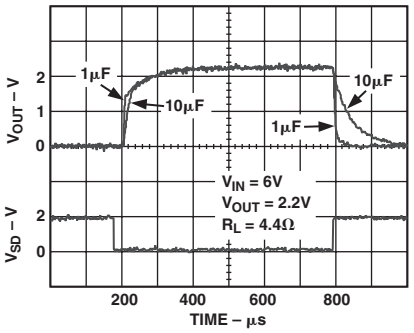

TPC 12. Load Transient Response



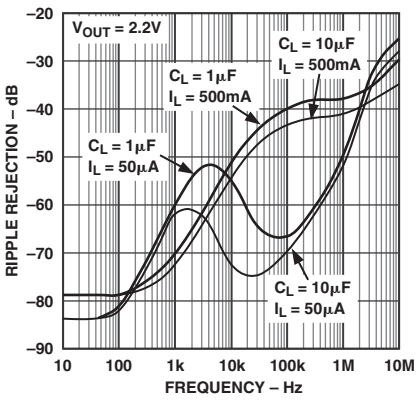

TPC 13. Load Transient Response



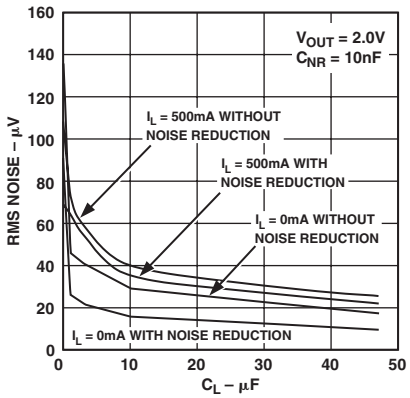

TPC 14. Short Circuit Current



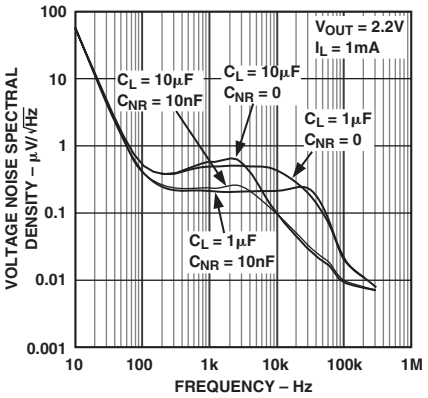

TPC 15. Turn Off/On Response




TPC 16. Power Supply Ripple Rejection




TPC 17. RMS Noise vs. $C_L$ (10 Hz to 100 kHz)




TPC 18. Output Noise Density

## THEORY OF OPERATION

The new anyCAP LDO ADP3334 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 that is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

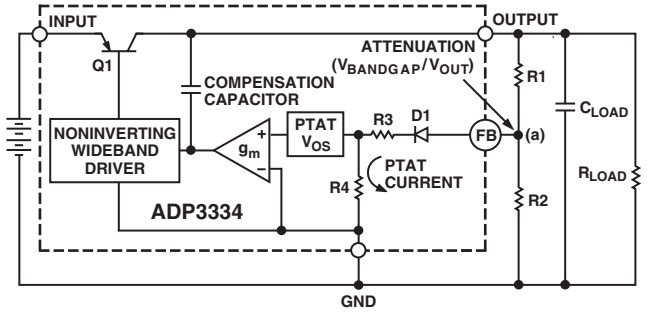



*Figure 2. Functional Block Diagram*

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that equilibrium produces a large, temperature-proportional input, "offset voltage" that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a "virtual band gap" voltage, implicit in the network although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider, thus avoiding the error resulting from base current loading in conventional circuits.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole-splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3334 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 µF capacitor on the output. Additional advantages of the pole-splitting scheme include superior line noise rejection and very high regulator gain, which lead to excellent line and load regulation. An impressive ±1.8% accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit and thermal shutdown.

## APPLICATION INFORMATION

### Output Capacitor

As with any micropower device, output transient response is a function of the output capacitance. The ADP3334 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3334 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types may fall below the minimum over the operating temperature range or with the application of a dc voltage.

### Input Bypass Capacitor

An input bypass capacitor is not strictly required but is advisable in any application involving long input wires or high source impedance. Connecting a 1 µF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

### Noise Reduction Capacitor

A noise reduction capacitor ($C_{NR}$) can be placed between the output and the feedback pin to further reduce the noise by 6 dB to 10 dB (TPC 18). Low leakage capacitors in the 100 pF to 1 nF range provide the best performance. Since the feedback pin (FB) is internally connected to a high impedance node, any connection to this node should be carefully done to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible, and long PC board traces are not recommended.

When adding a noise reduction capacitor, maintain a minimum load current of 1 mA when not in shutdown.

It is important to note that as $C_{NR}$ increases, the turn-on time will be delayed. With $C_{NR}$ values of 1 nF, this delay may be on the order of several milliseconds.

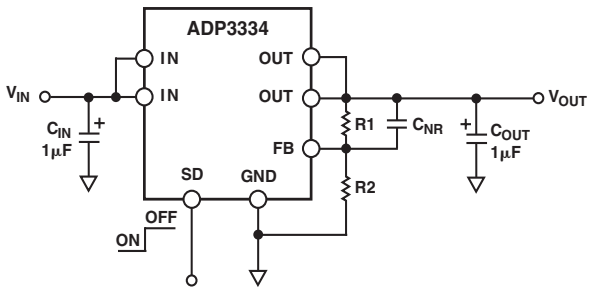



*Figure 3. Typical Application Circuit*

### Output Voltage

The ADP3334 has an adjustable output voltage that can be set by an external resistor divider. The output voltage will be divided by R1 and R2 and then fed back to the FB pin.

To have the lowest possible sensitivity of the output voltage to temperature variations, it is important that the value of the parallel resistance of $R1$ and $R2$ be kept as close as possible to 50 kΩ.

$$\frac{R1 \times R2}{R1 + R2} = 50\ k\Omega \quad (1)$$

Also, for the best accuracy over temperature, the feedback voltage should be set for 1.178 V:

$$V_{FB} = V_{OUT} \times \left( \frac{R2}{R1 + R2} \right) \quad (2)$$

where $V_{OUT}$ is the desired output voltage and $V_{FB}$ is the virtual band gap voltage. Note that $V_{FB}$ does not actually appear at the FB pin due to loading by the internal PTAT current.

Combining the above equations and solving for $R1$ and $R2$ gives the following formulas:

$$R1 = 50\ k\Omega \times \left( \frac{V_{OUT}}{V_{FB}} \right) \quad (3)$$

$$R2 = \frac{50\ k\Omega}{\left( 1 - \frac{V_{FB}}{V_{OUT}} \right)} \quad (4)$$

**Table I. Feedback Resistor Selection**

| $V_{OUT}$ (V) | R1 (1% Resistor) (kΩ) | R2 (1% Resistor) (kΩ) |
|---|---|---|
| 1.5 | 63.4 | 232.0 |
| 1.8 | 76.8 | 147.0 |
| 2.2 | 93.1 | 107.0 |
| 2.7 | 115.0 | 88.7 |
| 3.3 | 140.0 | 78.7 |
| 5.0 | 210.0 | 64.9 |
| 10.0 | 422.0 | 56.2 |

Using standard 1% values, as shown in Table I, will sacrifice some output voltage accuracy. To estimate the overall output voltage accuracy, it is necessary to take into account all sources of error. The accuracy given in the specifications table does not take into account the error introduced by the feedback resistor divider ratio or the error introduced by the parallel combination of the feedback resistors.

The error in the parallel combination of the feedback resistors causes the reference to have a wider variation over temperature. To estimate the variation, calculate the worst-case error from 50 kΩ, and then use the graph in Figure 4 to estimate the additional change in the output voltage over the operating temperature range.

For example:

$V_{IN}$ = 5 V
$V_{OUT}$ = 3.3 V
R1 = 140 kΩ, 1%
R2 = 78.7 kΩ, 1%

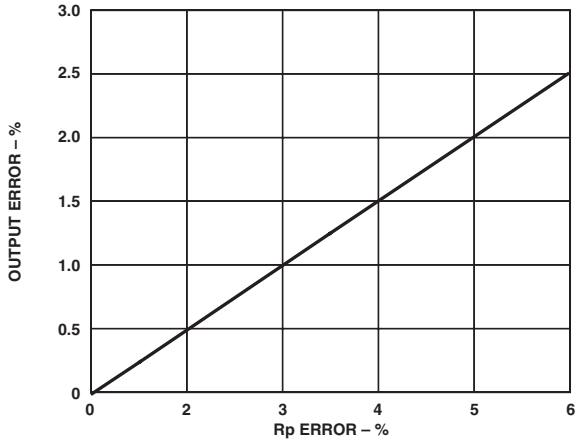



*Figure 4. Output Voltage Error vs. Parallel Resistance Error*

The actual output voltage can be calculated using the following equation.

$$V_{OUT} = 1.178\ V \times \left( \frac{R1}{R2} + 1 \right)$$
$$V_{OUT} = 3.274\ V \quad (5)$$

So worst-case error will occur when R1 has a –1% tolerance and R2 has a +1% tolerance. Recalculating the output voltage, the parallel resistance and error are:

$$V_{OUT} = 1.178\ V \times \left( \frac{138.6}{79.5} + 1 \right)$$
$$V_{OUT} = 3.232\ V \quad (6)$$
$$Resistor\ Divider\ Error = \left( \frac{3.232}{3.3} - 1 \right) \times 100\% = -2.1\%$$

$$R_{PARALLEL} = \frac{R1 \times R2}{R1 + R2} = \frac{138.6 \times 79.5}{138.6 + 79.5} = 50.51\ k\Omega$$
$$R_{PARALLEL}\ Error = \left( \frac{50.51}{50} - 1 \right) \times 100\% = 1.02\% \quad (7)$$

So, from the graph in Figure 4, the output voltage error is estimated to be an additional 0.25%. The error budget is 1.8% (the initial output voltage accuracy over temperature), plus 2.1% (resistor divider error), plus 0.25% (parallel resistance error) for a worst-case total of 4.15%.

**Thermal Overload Protection**

The ADP3334 is protected against damage from excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 150°C.

**Calculating Junction Temperature**

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) I_{LOAD} + (V_{IN}) I_{GND} \quad (8)$$

where $I_{LOAD}$ and $I_{GND}$ are load current and ground current, $V_{IN}$ and $V_{OUT}$ are input and output voltages, respectively.

Assuming $I_{LOAD}$ = 400 $mA$, $I_{GND}$ = 4 $mA$, $V_{IN}$ = 5.0 $V$ and $V_{OUT}$ = 2.8 $V$, device power dissipation is:

$$P_D = (5 - 2.8)\,400\,mA + 5.0\,(4\,mA) = 900\,mW \quad (9)$$

As an example, the proprietary package used in the ADP3334 has a thermal resistance of 86.6°C/W, significantly lower than a standard SOIC-8 package. Assuming a 4-layer board, the junction temperature rise above ambient temperature will be approximately equal to:

$$\Delta T_{JA} = 0.900W \times 86.6°C/W = 77.9°C \quad (10)$$

To limit the maximum junction temperature to 150°C, maximum allowable ambient temperature will be:

$$T_{AMAX} = 150°C - 77.9°C/W = 72.1°C \quad (11)$$

The maximum power dissipation versus ambient temperature for each package is shown in Figure 5.

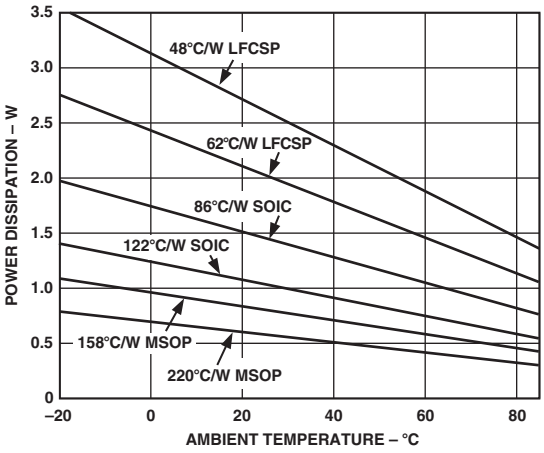



*Figure 5. Power Derating Curve*

**Printed Circuit Board Layout Consideration**

All surface-mount packages rely on the traces of the PC board to conduct heat away from the package.

In standard packages, the dominant component of the heat resistance path is the plastic between the die attach pad and the individual leads. In typical thermally enhanced packages, one or more of the leads are fused to the die attach pad, significantly decreasing this component. To make the improvement meaningful, however, a significant copper area on the PCB must be attached to these fused pins.

As an example, the patented thermal coastline lead frame design of the ADP3334 uniformly minimizes the value of the dominant portion of the thermal resistance. It ensures that heat is conducted away by all pins of the package. This yields a very low 86.6°C/W thermal resistance for the SOIC-8 package, without any special board layout requirements, relying only on the normal traces connected to the leads. This yields a 15% improvement in heat dissipation capability as compared to a standard SOIC-8 package. The thermal resistance can be decreased by an additional 10% by attaching a few square centimeters of copper area to the IN or OUT pins of the ADP3334 package.

It is not recommended to use solder mask or silkscreen on the PCB traces adjacent to the ADP3334's pins since it will increase the junction-to-ambient thermal resistance of the package.

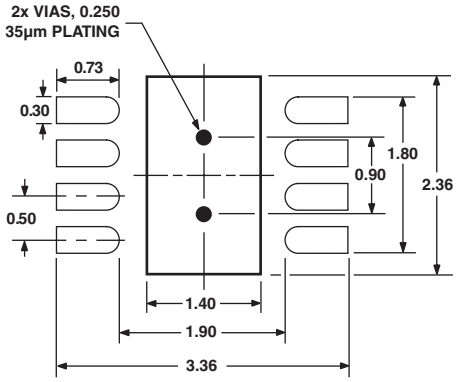



*Figure 6. 3 mm x 3 mm LFCSP Pad Pattern (Dimensions shown in millimeters)*

**LFCSP Layout Considerations**

The LFCSP package has an exposed die paddle on the bottom, which efficiently conducts heat to the PCB. In order to achieve the optimum performance from the LFCSP package, special consideration must be given to the layout of the PCB. Use the following layout guidelines for the LFCSP package.

1. The pad pattern is given in Figure 6. The pad dimension should be followed closely for reliable solder joints while maintaining reasonable clearances to prevent solder bridging.
2. The thermal pad of the LFCSP package provides a low thermal impedance path (approximately 20°C/W) to the PCB. Therefore the PCB must be properly designed to effectively conduct the heat away from the package. This is achieved by adding thermal vias to the PCB, which provide a thermal path to the inner or bottom layers. See Figure 5 for the recommended via pattern. Note that the via diameter is small to prevent the solder from flowing through the via and leaving voids in the thermal pad solder joint.

   Note that the thermal pad is attached to the die substrate, so the thermal planes that the vias attach the package to must be electrically isolated or connected to $V_{IN}$. Do NOT connect the thermal pad to ground.

3. The solder mask opening should be about 120 microns (4.7 mils) larger than the pad size resulting in a minimum 60 micron (2.4 mils) clearance between the pad and the solder mask.
4. The paste mask opening is typically designed to match the pad size used on the peripheral pads of the LFCSP package. This should provide a reliable solder joint as long as the stencil thickness is about 0.125 mm.

   The paste mask for the thermal pad needs to be designed for the maximum coverage to effectively remove the heat from the package. However, due to the presence of thermal vias and the size of the thermal pad, eliminating voids may not be possible.
5. The recommended paste mask stencil thickness is 0.125 mm. A laser cut stainless steel stencil with trapezoidal walls should be used.

   A "No Clean" Type 3 solder paste should be used for mounting the LFCSP package. Also, a nitrogen purge during the reflow process is recommended.
6. The package manufacturer recommends that the reflow temperature should not exceed 220°C and the time above liquidus is less than 75 seconds. The preheat ramp should be 3°C/second or lower. The actual temperature profile depends on the board density and must determined by the assembly house as to what works best.

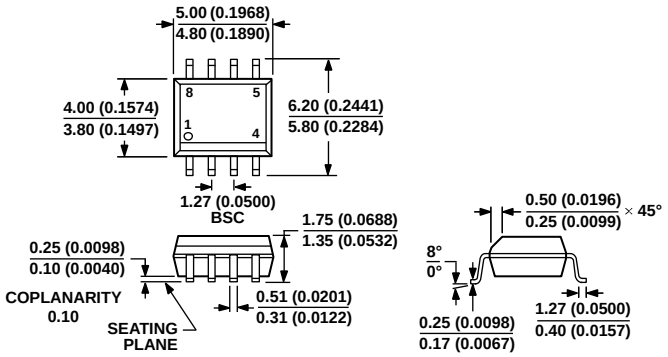
Use the following general guidelines when designing printed circuit boards.

1. Keep the output capacitor as close as possible to the output and ground pins.
2. Keep the input capacitor as close as possible to the input and ground pins.
3. PC board traces with larger cross sectional areas will remove more heat from the ADP3334. For optimum heat transfer, specify thick copper and use wide traces.
4. Use additional copper layers or planes to reduce the thermal resistance. When connecting to other layers, use multiple vias if possible.

**Shutdown Mode**

Applying a TTL high signal to the shutdown (SD) pin or the input pin will turn the output off. Pulling SD down to 0.4 V or below or tying it to ground will turn the output on. In shutdown mode, quiescent current is reduced to much less than 1 μA.

# OUTLINE DIMENSIONS

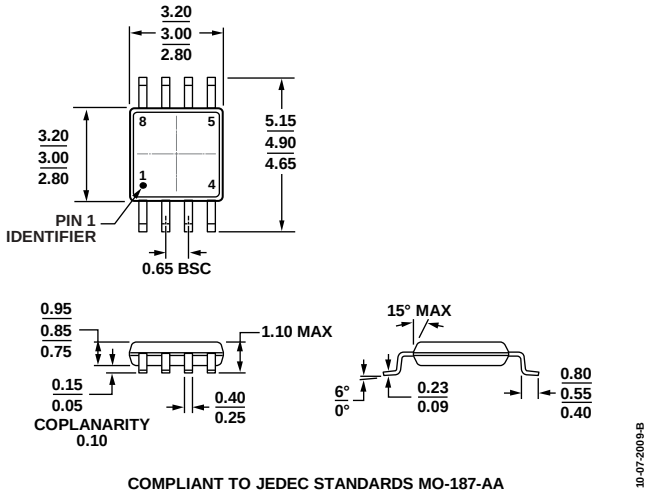



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

*Figure 7. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*




COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

*Figure 8. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

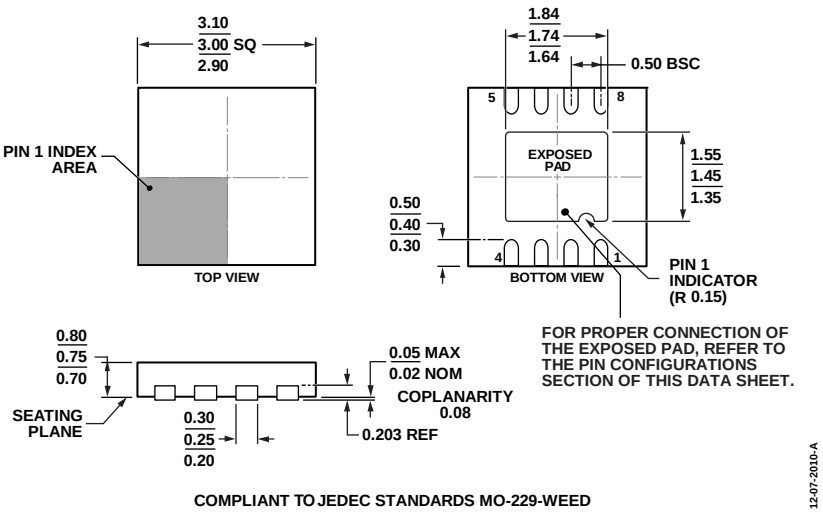



*Figure 9. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]*
*3 mm × 3 mm Body, Very Very Thin, Dual Lead*
*(CP-8-13)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Package Description | Package Option | Branding |
|---|---|---|---|
| ADP3334ARZ | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADP3334ARZ-REEL | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADP3334ARZ-REEL7 | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADP3334ACPZ-REEL7 | 8-Lead Lead Frame Chip Scale Package [LFCSP_WD] | CP-8-13 | LLA |
| ADP3334ARMZ-REEL7 | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | L1N |

[1] Z = RoHS Compliant Part.

## REVISION HISTORY

**1/14—Rev. B to Rev. C**

Added EPAD Note ..... 3
Changes to Figure 9, Outline Dimensions ..... 10
Changes to Ordering Guide ..... 11

**3/03—Rev. A to Rev. B**

Edits to Specifications ..... 2
Edits to Output Voltage ..... 6
Added text to Output Voltage section ..... 7
Added Figure 4 ..... 7
Edits to Calculating Junction Temperature section ..... 8
Renumbered Figures 5 and 6 ..... 8

**1/03—Rev. 0 to Rev. A**

Added 8-Lead LFCSP and 8-Lead MSOP Package ..... Universal
Edits to product title ..... 1
Edits to Features ..... 1
Edits to Applications ..... 1
Edits to General Description ..... 1
Removed pin numbers from Figure 1 ..... 1
Edits to Specifications ..... 2
Edits to Absolute Maximum Ratings ..... 3
Edits to Ordering Guide ..... 3
Added pinouts to Pin Configurations ..... 3
Added text to Calculating Junction Temperature section ..... 8
Added LFCSP Layout Considerations section ..... 8
Added Figure 5 ..... 8
Updated 8-Lead SOIC Package ..... 10