TABLE OF CONTENTS

REVISION HISTORY

8/12—Rev. B to Rev. C

Change to Features Section ... 1
Added ADIsimPower Design Tool Section ... 10
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 14

4/08—Rev. A to Rev. B

Change General Description Section ... 1
Deleted Figure 2 ... 1
Change to FB Regulation Voltage Parameter ... 3
Change to MOSFET Section ... 11
Changes to Ordering Guide ... 14

2/07—Rev 0. to Rev. A

Updated Format ... Universal
Changes to Figure 1 ... 1
Changes to General Description ... 2
Changes to Specifications ... 3
Change to Figure 13 ... 8
Replaced Layout Considerations Section ... 12
Replaced Example Applications Circuits Section ... 13

10/05—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 5 V, T_J = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage	V_{IN}		3.15		14	V
Quiescent Current	I_Q	V_{IN} = 3.15 V to 14 V, PGATE = IN		235	360	µA
Shutdown Supply Current	I_{SD}	V_{IN} = 3.15 V to 14 V, COMP = GND		7	15	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling, T_J = −40°C to +125°C	2.75	2.90	3.01	V
		V_{IN} rising, T_J = −40°C to +125°C	2.85	3.00	3.15	V
ERROR AMPLIFIER						
FB Input Current	I_{FB}	V_{FB} = 0.8 V, T_J = 25°C	−20	−2	+20	nA
		V_{FB} = 0.8 V, T_J = −40°C to +125°C	−40	−2	+40	nA
Amplifier Transconductance		V_{FB} = 0.8 V, I_{COMP} = ±5 µA		0.24		mmho
COMP Startup Threshold		V_{IN} = 3.15 V to 14 V, T_J = −40°C to +125°C	0.55	0.67	0.80	V
COMP Shutdown Threshold		V_{IN} = 3.15 V to 14 V, T_J = −40°C to +125°C	0.15	0.3	0.55	V
COMP Start-Up Current Source		COMP = GND	0.25	0.6	0.95	µA
FB Regulation Voltage		V_{IN} = 3.15 V to 14 V, T_J = −40°C to +125°C	0.790	0.8	0.810	V
Overvoltage Protection Threshold	V_{OVP}	Measured at FB, T_J = −40°C to +125°C	0.87	0.885	0.9	V
Overvoltage Protection Hysteresis				50		mV
CURRENT SENSE						
Peak Current Sense Voltage		T_J = −40°C to +125°C	90	125		mV
		V_{IN} = 3.15 V to 14 V, T_J = −40°C to +125°C	70	125		mV
Current Sense Gain		V_{CS} to V_{COMP}		12		V/V
OUTPUT REGULATION						
Line Regulation[1]		V_{IN} = 3.15 V to 14 V, V_{FB}/V_{IN}		0.12		mV/V
Load Regulation[2]		V_{FB}/V_{COMP}		−2		mV/V
OSCILLATOR						
Oscillator Frequency		V_{FB} = 0.8 V, T_J = −40°C to +125°C	500	580	650	kHz
		V_{FB} = 0 V		190		kHz
FB Frequency Foldback Threshold				0.35		V
GATE DRIVE						
Gate Rise Time		C_{GATE} = 3 nF		50		ns
Gate Fall Time		C_{GATE} = 3 nF		40		ns
Minimum On Time		PGATE minimum low duration		190		ns
SOFT START POWER-ON TIME				1.1		ms

[1] Line regulation is measured using the application circuit in Figure 1. Line regulation is specified as the change in the FB voltage resulting from a 1 V change in the IN voltage.

[2] Load regulation is measured using the application circuit in Figure 1. Load regulation is specified as the change in the FB voltage resulting from a 1 V change in the COMP voltage. The COMP voltage range is typically 0.9 V to 2.3 V for the minimum to maximum load current condition.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	−0.3 V to +16 V
CS, PGATE to GND	−0.3 V to (V_{IN} + 0.3 V)
FB, COMP to GND	−0.3 V to +6 V
θ_{JA} 2-Layer (SEMI Standard Board)	315°C/W
θ_{JA} 4-Layer (JEDEC Standard Board)	186°C/W
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Rework Temperature (J-STD-020B)	260°C
Peak Reflow Temperature, (20 sec to 40 sec, J-STD-020B)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

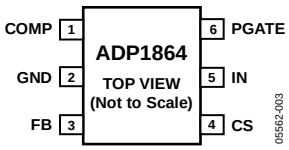


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	Regulator Compensation Node. COMP is the output of the internal transconductance error amplifier. Connect a series RC from COMP to GND to compensate for the control loop. Add an extra high frequency capacitor between COMP and GND to further reduce switching jitter. The value of this is typically one-tenth of the main compensation capacitor. Pulling the COMP pin below 0.3 V disables the ADP1864 and turns off the external PFET.
2	GND	Analog Ground. Directly connect the compensation and feedback networks to GND, preferably with a small analog GND plane. Connect GND to the power ground (PGND) plane with a narrow track at a single point close to the GND pin. See the Layout Considerations section for more information.
3	FB	Feedback Input. Connect a resistive voltage divider from the output voltage to FB to set the output voltage. The regulation feedback voltage is 0.8 V. Place the feedback resistors as close as possible to the FB pin.
4	CS	Current Sense Input. CS is the negative input of the current sense amplifier. It provides the current feedback signal used to terminate the PWM on time. Place a current sense resistor between IN and CS to set the current limit. The current limit threshold is typically 125 mV.
5	IN	Power Input. IN is the power supply to the ADP1864 and the positive input of the current sense amplifier. Connect IN to the positive side of the input voltage source. Bypass IN to PGND with a 10 µF or larger capacitor as close as possible to the ADP1864. For additional high frequency noise reduction, add a 0.1 µF capacitor to PGND at the IN pin.
6	PGATE	Gate Drive Output. PGATE drives the gate of the external P-channel MOSFET. Connect PGATE to the gate of the external MOSFET.

TYPICAL PERFORMANCE CHARACTERISTICS

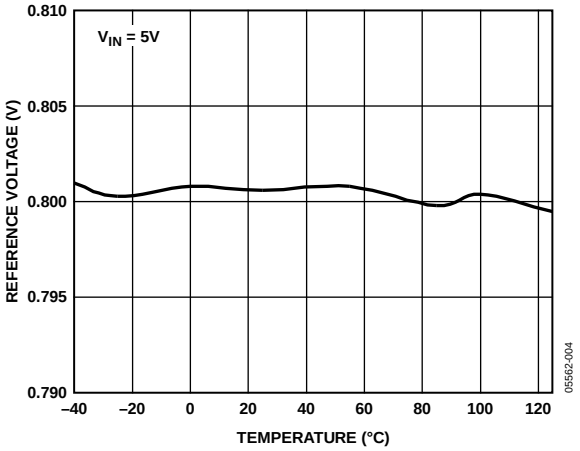


Figure 3. Reference Voltage vs. Temperature

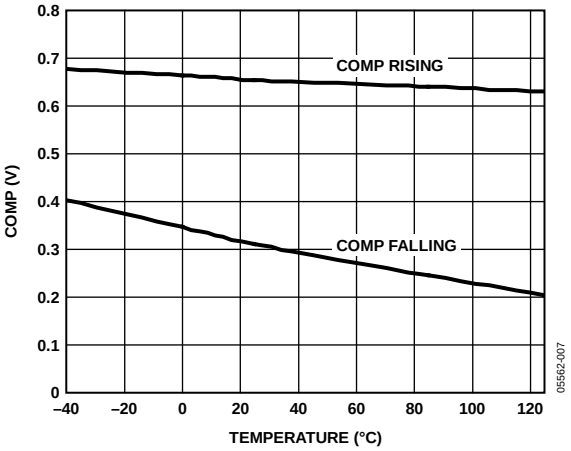


Figure 6. COMP Shutdown Threshold vs. Temperature

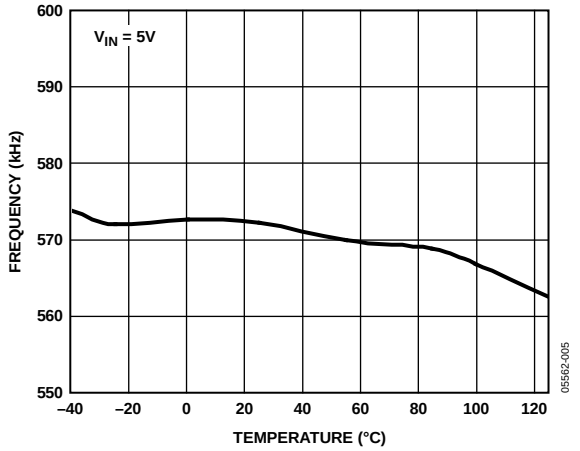


Figure 4. Normalized Oscillator Frequency vs. Temperature

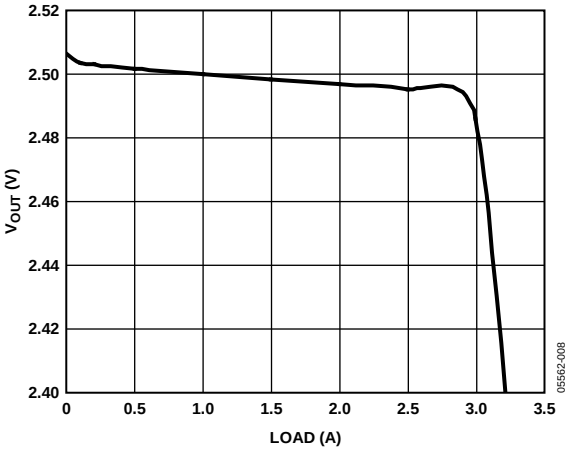


Figure 7. Typical Load Regulation (V_{IN} = 5 V; See Figure 1)

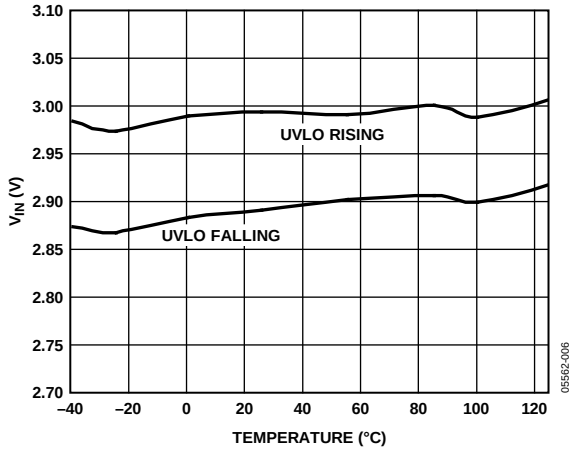


Figure 5. UVLO Voltage vs. Temperature (V_{IN} Rising and V_{IN} Falling)

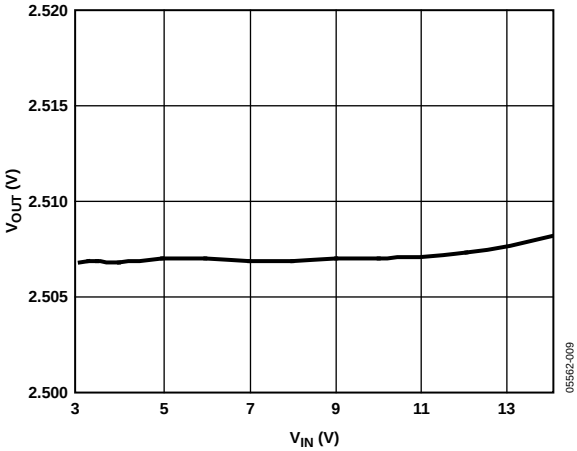


Figure 8. Typical Line Regulation vs. Input Voltage (See Figure 19)

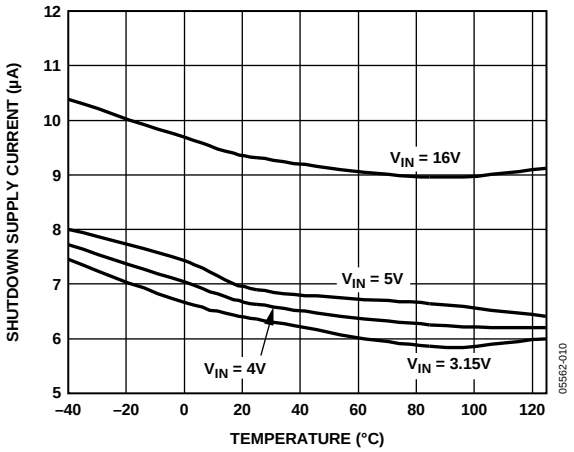


Figure 9. Shutdown Supply Current vs. Temperature

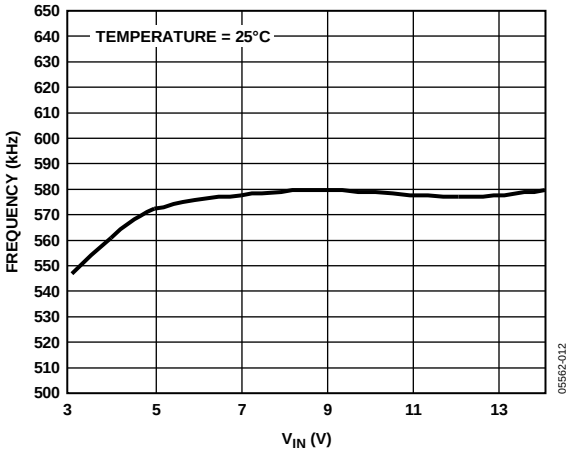


Figure 11. Oscillator Frequency vs. Input Voltage

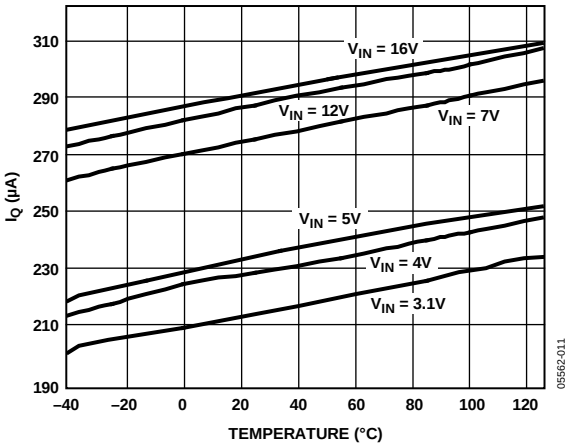


Figure 10. Quiescent Current vs. Temperature

THEORY OF OPERATION

The ADP1864 is a constant frequency (580 kHz), current-mode buck controller. PGATE drives the gate of the external P-channel FET. The duty cycle of the external FET dictates the output voltage and the current supplied to the load.

The peak inductor current is measured across the external sense resistor, while the system output voltage is fed back through an external resistor divider to the FB pin.

At the start of every oscillator cycle, PGATE turns on the external FET, causing the inductor current, and therefore the current sense amplifier voltage, to increase. The inductor current increases until the current amplifier voltage equals the voltage at the COMP pin. This resets the internal flip-flop, causing PGATE to go high and turning off the external FET. The inductor current decreases until the beginning of the next oscillator period.

The voltage at the COMP node is the output of the internal error amplifier. The negative input of the error amplifier is the output voltage scaled by an external resistive divider, and the positive input to the error amplifier is driven by a 0.8 V band gap reference. An increase in the load current causes a small drop in the feedback voltage, in turn causing an increase in the COMP voltage and, therefore, the duty cycle. The resulting increase in the on time of the FET provides the additional current required by the load.

LOOP STARTUP

Pulling the COMP pin to GND disables the ADP1864. When the COMP pin is released from GND, an internal 0.6 µA current source charges the external compensation capacitor on the COMP node. Once the COMP voltage has charged to 0.67 V, the internal control blocks are enabled and COMP is pulled up to its minimum normal operating voltage (0.9 V). As the voltage at COMP continues to increase, the on time of the external FET increases to supply the required inductor current. The loop stabilizes completely once the COMP voltage is sufficiently high to support the load current. The regulation voltage at FB is 0.8 V.

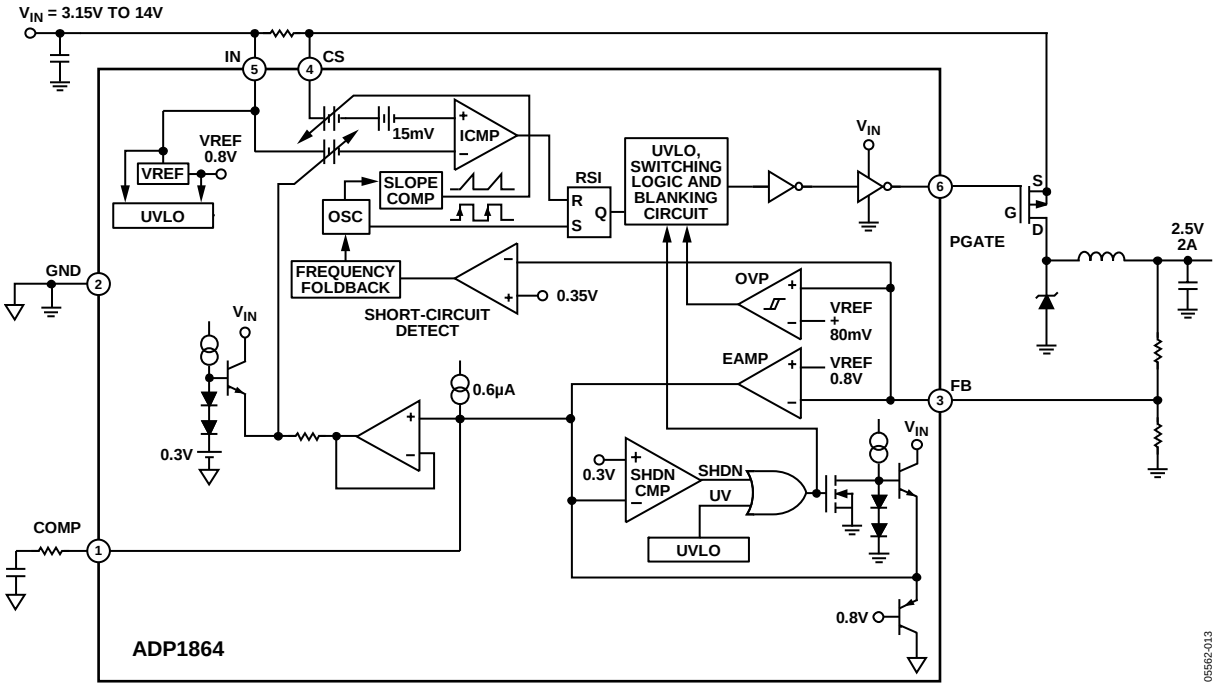


Figure 12. Functional Block Diagram

SHORT-CIRCUIT PROTECTION

If there is a short across the output load, the voltage at the feedback pin (FB) drops rapidly. When the FB voltage drops below 0.35 V, the ADP1864 reduces the oscillator frequency to 190 kHz. The increase in the oscillator period allows the inductor additional time to discharge, preventing the output current from running away. Once the output short is removed and the feedback voltage increases above the 0.35 V threshold, the oscillator frequency returns to 580 kHz.

UNDERVOLTAGE LOCKOUT (UVLO)

To prevent erratic operation when the input voltage drops below the minimum acceptable voltage, the ADP1864 has an undervoltage lockout (UVLO) feature. If the input voltage drops below 2.90 V, PGATE is pulled high and the ADP1864 continues to draw its typical quiescent current. Current consumption continues to drop toward the shutdown current as input voltage is reduced. The ADP1864 is re-enabled and begins switching once the IN voltage is increased above the UVLO rising threshold (3.0 V).

OVERVOLTAGE LOCKOUT PROTECTION (OVP)

The ADP1864 provides an overvoltage protection feature to protect the system against output short circuits to a higher voltage supply. If the feedback voltage increases to 0.885 V, PGATE is held high, turning the external FET off. The FET continues to be held high until the voltage at FB decreases to 0.84 V, at which time the ADP1864 resumes normal operation.

SOFT START

The ADP1864 includes a soft start feature that limits the rate of increase in the inductor current once the part is enabled. Soft start is activated when the input voltage is increased above the UVLO threshold or COMP is released from GND. Soft start limits the inrush current at the input and limits the output voltage overshoot. The soft start control slope is set internally.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP1864 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

DUTY CYCLE

To determine the worst-case inductor ripple current, output voltage ripple, and slope compensation factor, establish the system maximum and minimum duty cycle. The duty cycle is calculated by the equation

$$Duty\ Cycle\ (DC) = \frac{V_{OUT} + V_D}{V_{IN} + V_D} \quad (1)$$

where V_D is the diode forward drop.

A typical Schottky diode has a forward voltage drop of 0.5 V.

RIPPLE CURRENT

Choose the peak-to-peak inductor ripple current between 20% and 40% of the maximum load current at the system's highest input voltage. A good starting point for a design is to pick the peak-to-peak ripple current at 30% of the load current.

$$\Delta I_{(PEAK)} = 0.3 \times I_{LOAD(MAX)} \quad (2)$$

SENSE RESISTOR

Choose the sense resistor value to provide the desired current limit. The internal current comparator measures the peak current (sum of load current and positive inductor ripple current) and compares it against the current limit threshold. The current sense resistor value is calculated by the equation

$$R_{SENSE(MIN)} = \frac{PCSV}{I_{LOAD(MAX)} + \frac{\Delta I_{(PEAK)}}{2}} \quad (3)$$

where *PCSV* is the peak current sense voltage, typically 0.125 V.

To ensure the design provides the required output load current over all system conditions, consider the variation in PCSV over temperature (see the Specifications section) as well as increases in ripple current due to inductor tolerance.

If the system is being operated with >40% duty cycle, incorporate the slope compensation factor into the calculation.

$$R_{SENSE(MIN)} = \frac{SF \times PCSV}{I_{LOAD(MAX)} + \frac{\Delta I_{(PEAK)}}{2}} \quad (4)$$

where *SF* is the slope factor correction ratio, taken from Figure 13, at the system maximum duty cycle (minimum input voltage).

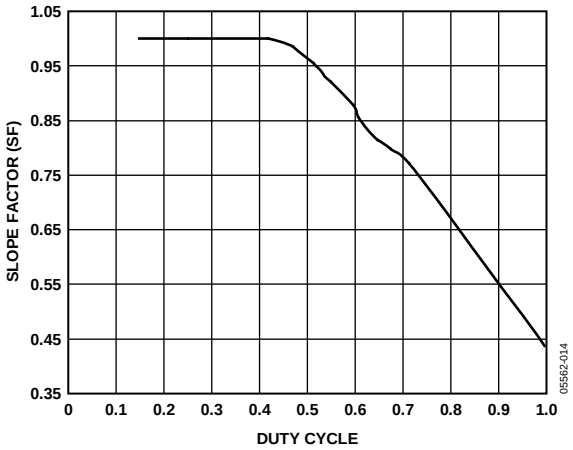


Figure 13. Slope Factor (SF) vs. Duty Cycle

INDUCTOR VALUE

The inductor value choice is important because it dictates the inductor ripple and, therefore, the voltage ripple at the output. When operating the part at >40% duty cycle, keep the inductor value low enough for the slope compensation to remain effective.

The inductor ripple current is inversely related to the inductor value.

$$\Delta I_{(PEAK)} = \frac{(V_{IN} - V_{OUT})}{L \times f} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \quad (5)$$

where *f* is the oscillator frequency.

Smaller inductor values are usually less expensive, but increase the ripple current and the output voltage ripple. Too large an inductor value results in added expenses and can impede effective load transient responses at >40% duty cycle because it reduces the effect of slope compensation.

Start with the highest input voltage, and assuming the ripple current is 30% of the maximum load current,

$$L = \frac{(V_{IN} - V_{OUT})}{0.3 \times I_{LOAD(MAX)} \times f} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \quad (6)$$

From this starting point, modify the inductance to obtain the right balance of size, cost, and output voltage ripple, while maintaining the inductor ripple current between 20% and 40% of the maximum load current.

MOSFET

Choose the external P-channel MOSFET based on the following: threshold voltage (V_T), maximum voltage and current ratings, $R_{DS(ON)}$, and gate charge.

The minimum operating voltage of the ADP1864 is 3.15 V. Choose a MOSFET with a V_T that is at least 1 V lower than the minimum input supply voltage used in the application.

Ensure that the maximum ratings for MOSFET V_{SG} and V_{SD} are a few volts greater than the maximum input voltage used with the ADP1864.

Estimate the rms current in the MOSFET under continuous conduction mode by

$$I_{FET\,(rms)} = \sqrt{\frac{V_{OUT} + V_D}{V_{IN} + V_D}} \times I_{LOAD} \quad (7)$$

Derate the MOSFET current by at least 20% to account for inductor ripple and changes in the diode voltage.

The MOSFET power dissipation is the sum of the conducted and switching losses:

$$PD_{FET(COND)} = (I_{FET(rms)})^2 \times (1 + T) \times R_{DS(ON)} \quad (8)$$

where $T = 0.005/°C \times T_{J\,(FET)} - 25°C$.

Ensure the maximum power dissipation calculated is significantly less than the maximum rating of the MOSFET.

DIODE

The diode carries the inductor current during the off time of the external FET. The average current of the diode is, therefore, dependent on the duty cycle of the controller as well as the output load current.

$$I_{DIODE(AV)} = \left(1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \times I_{LOAD} \quad (9)$$

where V_D is the diode forward drop.

A typical Schottky diode has a forward drop voltage of 0.5 V.

A Schottky diode is recommended for best efficiency because it has a low forward drop and faster switching speed than junction diodes. If a junction diode is used it must be an ultrafast recovery diode. The low forward drop reduces power losses during the FET off time, and fast switching speed reduces the switching losses during PFET transitions.

INPUT CAPACITOR

The input capacitor provides a low impedance path for the pulsed current drawn by the external P-channel FET. Choose an input capacitor whose impedance at the switching frequency is lower than the impedance of the voltage source (V_{IN}). The preferred input capacitor is a 10 µF ceramic capacitor due to its low ESR and low impedance.

For all types of capacitors, make sure the ripple current rating of the capacitor is greater than half of the maximum output load current.

Where space is limited, multiple capacitors can be placed in parallel to meet the rms current requirement. Place the input capacitor as close as possible to the IN pin of the ADP1864.

OUTPUT CAPACITOR

The ESR and capacitance value of the output capacitor determine the amount of output voltage ripple.

$$\Delta V \cong \Delta I \times \left(\frac{1}{8 \times f \times C_{OUT}} + ESR_{C_{OUT}}\right) \quad (10)$$

where f is the oscillator frequency (typically 580 kHz).

Because the output capacitance is typically >40 µF, the ESR dominates the voltage ripple. Ensure the output capacitor ripple rating is greater than the maximum inductor ripple.

$$I_{rms} \cong \frac{1}{2 \times \sqrt{3}} \times \left(\frac{(V_{OUT} + V_D) \times (V_{IN} - V_{OUT})}{L \times f \times V_{IN}}\right) \quad (11)$$

POSCAP™ capacitors from Sanyo offer a good size, ESR, ripple, and current capability trade-off.

FEEDBACK RESISTORS

The feedback resistors ratio sets the output voltage of the system.

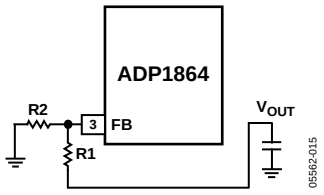


Figure 14. Two Feedback Resistors Used to Set Output Voltage

$$0.8\,V = V_{OUT} \times \frac{R2}{R1 + R2} \quad (12)$$

$$R1 = R2 \times \frac{(V_{OUT} - 0.8)}{0.8} \quad (13)$$

Choose 80.6 kΩ for R2. Using higher values for R2 results in reduced output voltage accuracy, and lower values cause an increased voltage divider current, thus increasing quiescent current consumption.

LAYOUT CONSIDERATIONS

Layout is important with all switching regulators, but is particularly important for high switching frequencies. Ensure all high current paths are as wide as possible to minimize track inductance, which causes spiking and electromagnetic interference (EMI). These paths are shown in bold in Figure 15. Place the current sense resistor and the input capacitor(s) as close to the IN pin as possible.

Keep the PGND connections for the diode, input capacitor(s), and output capacitor(s) as close together as possible on a wide PGND plane. Connect the PGND and GND planes at a single point with a narrow trace close to the ADP1864 GND connection.

Ensure the feedback resistors are placed as close as possible to the FB pin to prevent stray pickup. To prevent extra noise pickup on the FB line, do not allow the feedback trace from the output voltage to FB to pass right beside the drain of the external PFET. Add an extra copper plane at the connection of the FET drain and the cathode of the diode to help dissipate the heat generated by losses in those components.

All analog components are grouped together on the left side of the evaluation board (left side of the ADP1864 DUT, see Figure 16), including compensation and FB components. All power components are located on the right side of the board (MOSFET, inductor, input bypass capacitors, output capacitors, and power diode).

All noisy nodes (P-channel drain, power diode cathode, and inductor terminal) are located along the bottom portion of the evaluation board on the top layer (see Figure 16). A substantial amount of copper has been allocated for this area with ample track spacing to minimize coupling (crosstalk) effects during switching.

The FB tap is isolated and runs from the R_{TOP}, along the upper right portion of the board on the bottom layer (see Figure 17) to minimize EMI pickups emitted from the power components along the bottom portion of the evaluation board's top layer (see Figure 16). Sufficient track spacing is placed from the main power ground plane located near the center of the board to effectively decouple this track.

There are two ground planes on the top layer: the analog ground plane is on the left and the power ground plane on the right. An analog ground pickup point projects down to the bottom layer and through a single narrow and isolated track (see Figure 17).

The P-channel gate should have an isolated trace (bottom layer) tying back to Pin 6 of the DUT by via connections.

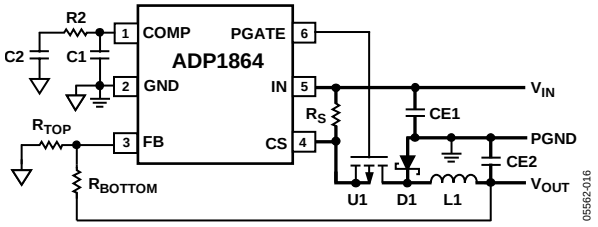


Figure 15. Application Circuit Showing High Current Paths (in Bold)

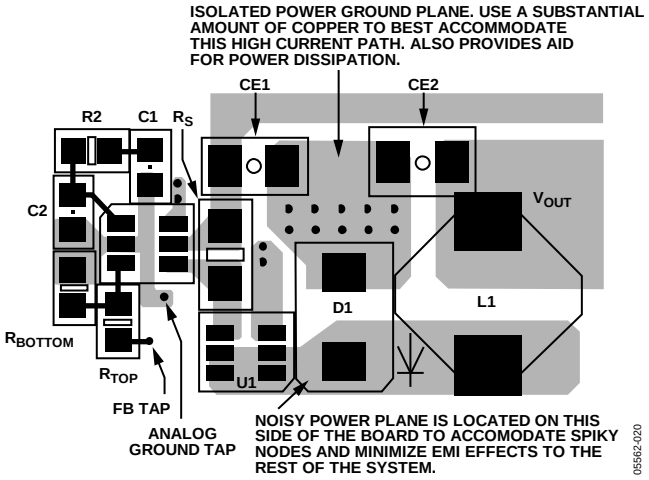
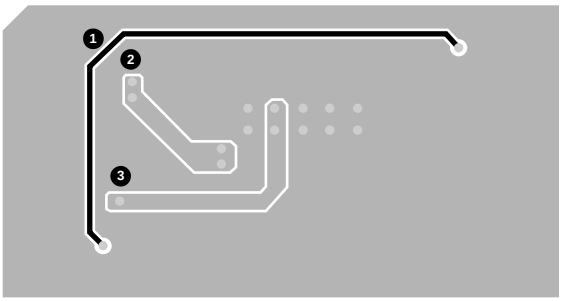


Figure 16. Top Layer of an Example Layout for an ADP1864 Application



1 FB TAP FROM OUTPUT TO R_{TOP}. TRACE SHOULD BE AWAY FROM POWER COMPONENTS TO MINIMIZE EMI PICKUP.

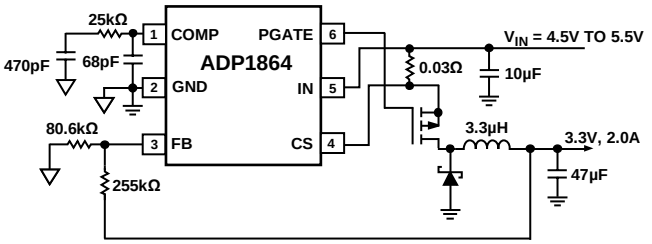
2 ISOLATED TRACE FOR GATE CONNECTION OF THE PFET. ROUTING OF THIS CONNECTION AWAY FROM THE CATHODE OF D1 AND DRAIN OF PFET IS TO ENSURE THAT NOISE DOES NOT COUPLE INTO THIS TRACK.

3 ISOLATED TRACK FOR CONNECTING AGND TO PGND. THIS HELPS MINIMIZE STRAY PARASITIC EFFECTS TOWARDS THE ANALOG COMPONENTS (FB AND COMPENSATION COMPONENTS).

05562-021

Figure 17. Bottom Layer of an Example Layout of an ADP1864 Application

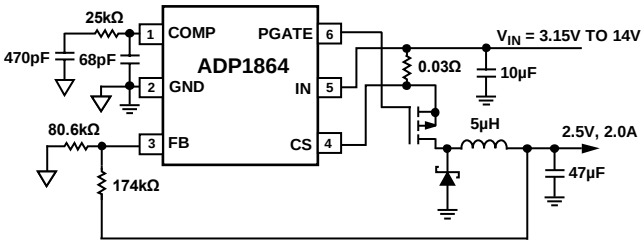
EXAMPLE APPLICATIONS CIRCUITS



RSENSE LRC-LR1206-01-R030-F
MOSFET FAIRCHILD SEMI FDC638P
INDUCTOR TOKO FDV0630-3R3M
DIODE SYNSEMI SK22
CIN LMK325BJ106KN
COUT SANYO POSCAP 6TPB47M

05562-018

Figure 18. Application Circuit for V_{OUT} = 3.3 V, 2 A Load



RSENSE LRC-LR1206-01-R030-F
MOSFET FAIRCHILD SEMI FDC658P
INDUCTOR SUMIDA CDRH6D38-5R0
DIODE VISHAY SSB43L
CIN LMK325BJ106KN
COUT SANYO POSCAP 6TPB47M

05562-019

Figure 19. Application Circuit for V_{OUT} = 2.5 V, 2 A Load

OUTLINE DIMENSIONS

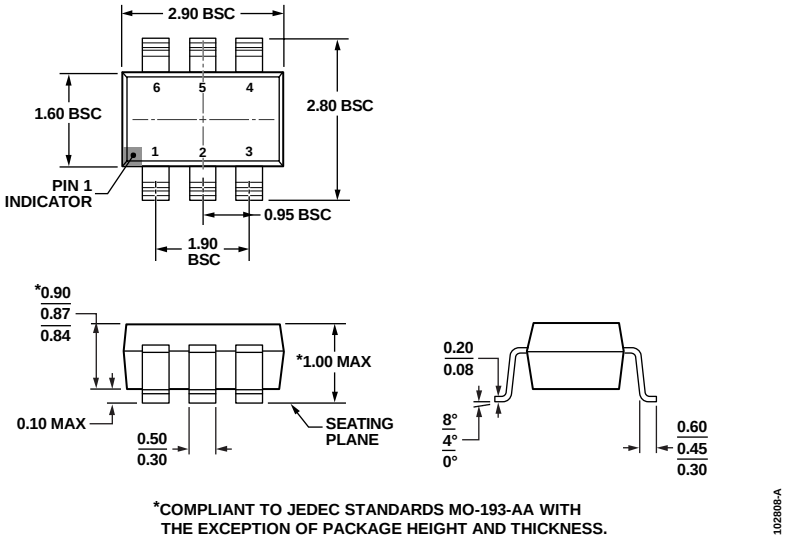


Figure 20. 6-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding
ADP1864AUJZ-R7	−40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	P0N
ADP1864-EVAL		Evaluation Board		
ADP1864-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] V_{OUT} = 2.5 V (variable), I_{LOAD} = 0 A to 3 A, V_{IN} = 3.15 V to 14 V.

NOTES

NOTES