ADL5382* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- ADL5382 Evaluation Board

Documentation

Application Notes

- AN-1236: Interfacing the ADL5382 Quadrature I/Q Demodulator to the AD9262 16-Bit Continuous Time Sigma-Delta ADC as an RF-to-Bits Solution

Data Sheet

- ADL5382: 700 MHz to 2.7 GHz Quadrature Demodulator Datasheet

User Guides

- UG-093: Evaluation Board User Guide for the Dual, Continuous Time Sigma-Delta Modulator

Tools and Simulations

- ADIsimPLL™
- ADIsimRF

Reference Materials

Product Selection Guide

- RF Source Booklet

Technical Articles

- Assess Quadrature-Demodulator Noise Figure Using Vector Signal Analysis
- Direct Conversion Receiver Designs Enable Multi-standard/ Multi-band Operation
- Semiconductors Simplify Direct-Conversion Design
- Semiconductors Simplify Direct-Conversion Design

Design Resources

- ADL5382 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADL5382 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

TABLE OF CONTENTS

REVISION HISTORY

5/12—Rev. 0 to Rev. A

Added θ_{JC} = 3°C/W to Table 2 ... 5
Added EPAD Note to Figure 2 ... 6
Updated Outline Dimensions ... 27

3/08—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{LO} = 900 MHz, f_{IF} = 4.5 MHz, P_{LO} = 0 dBm, BIAS pin open, Z_O = 50 Ω, unless otherwise noted. Baseband outputs differentially loaded with 450 Ω. Loss of the balun used to drive the RF port was de-embedded from these measurements.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO and RF Frequency Range		0.7		2.7	GHz
LO INPUT	LOIP, LOIN				
Input Return Loss	LO driven differentially through a balun at 900 MHz		−11		dB
LO Input Level		−6	0	+6	dBm
I/Q BASEBAND OUTPUTS	QHI, QLO, IHI, ILO				
Voltage Conversion Gain	450 Ω differential load on I and Q outputs at 900 MHz		3.9		dB
	200 Ω differential load on I and Q outputs at 900 MHz		3.0		dB
Demodulation Bandwidth	1 V p-p signal, 3 dB bandwidth		370		MHz
Quadrature Phase Error	At 900 MHz		0.2		Degrees
I/Q Amplitude Imbalance			0.05		dB
Output DC Offset (Differential)	0 dBm LO input at 900 MHz		±5		mV
Output Common Mode			VPOS − 2.8		V
0.1 dB Gain Flatness			50		MHz
Output Swing	Differential 200 Ω load		2		V p-p
Peak Output Current	Each pin		12		mA
POWER SUPPLIES	VPA, VPL, VPB, VPX				
Voltage		4.75		5.25	V
Current	BIAS pin open		220		mA
	R_{BIAS} = 4 kΩ		196		mA
DYNAMIC PERFORMANCE at RF = 900 MHz					
Conversion Gain			3.9		dB
Input P1dB			14.7		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		73		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		33.5		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−92		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−89		dBc
IQ Magnitude Imbalance			0.05		dB
IQ Phase Imbalance			0.2		Degrees
LO to IQ	RFIN, RFIP terminated in 50 Ω		−43		dBm
Noise Figure			14.0		dB
Noise Figure under Blocking Conditions	With a −5 dBm interferer 5 MHz away		19.9		dB
DYNAMIC PERFORMANCE at RF = 1900 MHz					
Conversion Gain			3.9		dB
Input P1dB			14.4		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		65		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		30.5		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−71		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−78		dBc
IQ Magnitude Imbalance			0.05		dB
IQ Phase Imbalance			0.2		Degrees
LO to IQ	RFIN, RFIP terminated in 50 Ω		−41		dBm
Noise Figure			15.6		dB
Noise Figure under Blocking Conditions	With a −5 dBm interferer 5 MHz away		20.5		dB

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE at RF = 2700 MHz	RFIP, RFIN				
Conversion Gain			3.3		dB
Input P1dB			14.5		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		52		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		28.3		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω, 1xLO appearing at RF port		−70		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−55		dBc
IQ Magnitude Imbalance			0.16		dB
IQ Phase Imbalance			0.1		Degrees
LO to IQ	RFIN, RFIP terminated in 50 Ω, 1xLO appearing at BB port		−42		dBm
Noise Figure			17.6		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VPA, VPL, VPB, VPX)	5.5 V
LO Input Power	13 dBm (re: 50 Ω)
RF Input Power	15 dBm (re: 50 Ω)
Internal Maximum Power Dissipation	1230 mW
θ_{JA}	54°C/W
θ_{JC}	3°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

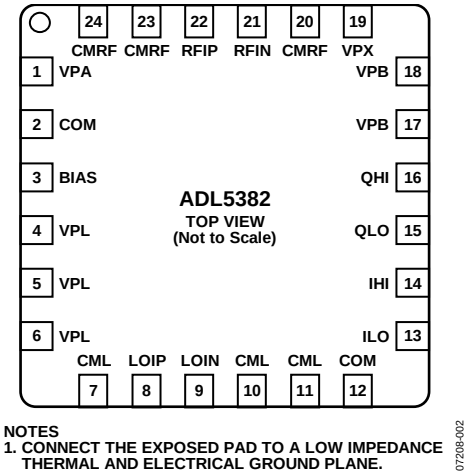

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4 to 6, 17 to 19	VPA, VPL, VPB, VPX	Supply. Positive supply for LO, IF, biasing, and baseband sections. These pins should be decoupled to the board ground using appropriate-sized capacitors.
2, 7, 10 to 12, 20, 23, 24	COM, CML, CMRF	Ground. Connect to a low impedance ground plane.
3	BIAS	Bias Control. A resistor (R_{BIAS}) can be connected between BIAS and COM to reduce the mixer core current. The default setting for this pin is open.
8, 9	LOIP, LOIN	Local Oscillator Input. Pins must be ac-coupled. A differential drive through a balun (recommended balun is the M/A-COM ETC1-1-13) is necessary to achieve optimal performance.
13 to 16	ILO, IHI, QLO, QHI	I Channel and Q Channel Mixer Baseband Outputs. These outputs have a 50 Ω differential output impedance (25 Ω per pin). The bias level on these pins is equal to VPOS − 2.8 V. Each output pair can swing 2 V p-p (differential) into a load of 200 Ω. Output 3 dB bandwidth is 370 MHz.
21, 22	RFIN, RFIP	RF Input. A single-ended 50 Ω signal can be applied to the RF inputs through a 1:1 balun (recommended balun is the M/A-COM ETC1-1-13). Ground-referenced inductors must also be connected to RFIP and RFIN (recommended values = 33 nH).
	EP	Exposed Paddle. Connect to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, LO drive level = 0 dBm, R_{BIAS} = open, RF input balun loss is de-embedded, unless otherwise noted.

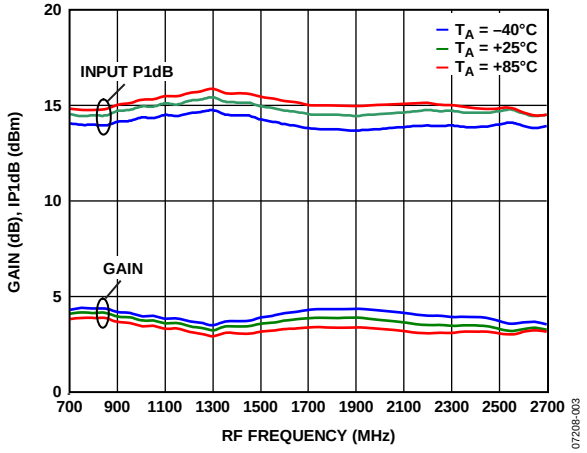

Figure 3. Conversion Gain and Input IP1 dB Compression Point (IP1dB) vs. RF Frequency

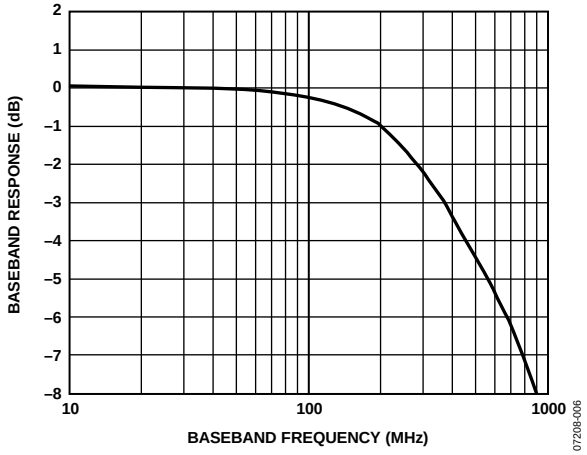

Figure 6. Normalized IQ Baseband Frequency Response

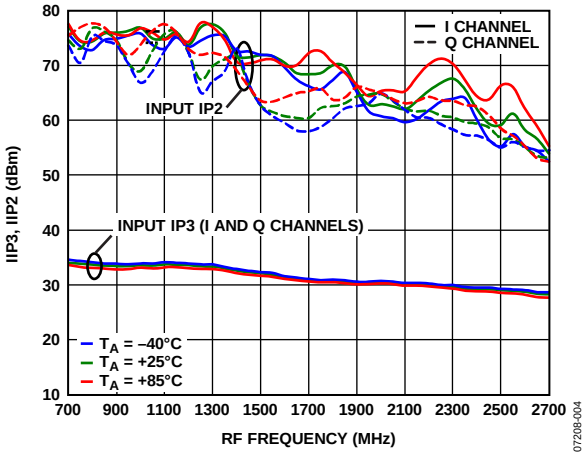

Figure 4. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. RF Frequency

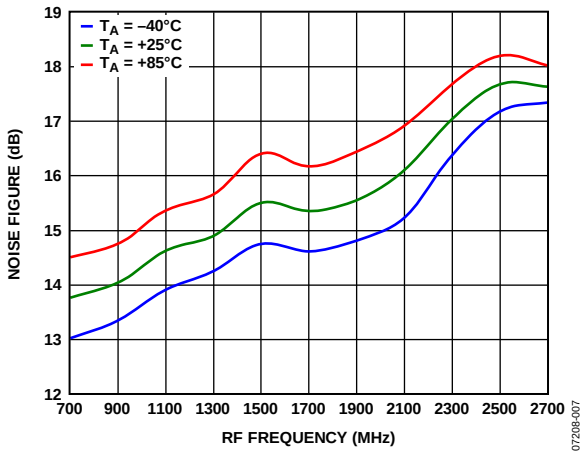

Figure 7. Noise Figure vs. RF Frequency

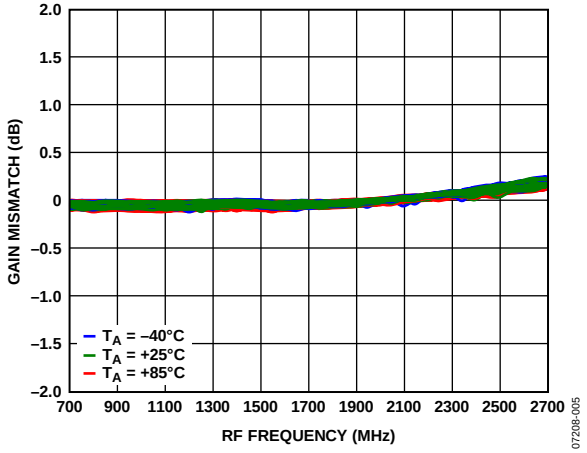

Figure 5. IQ Gain Mismatch vs. RF Frequency

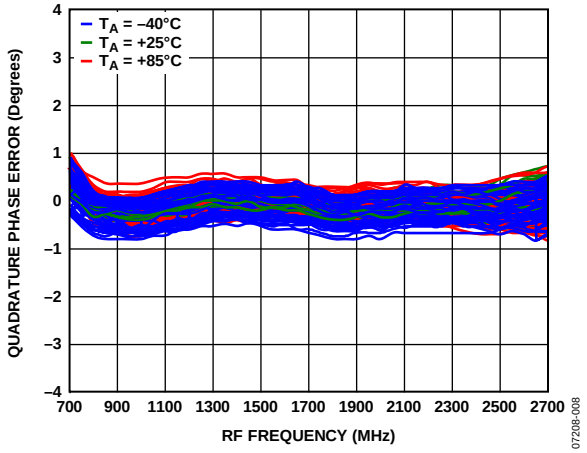

Figure 8. IQ Quadrature Phase Error vs. RF Frequency

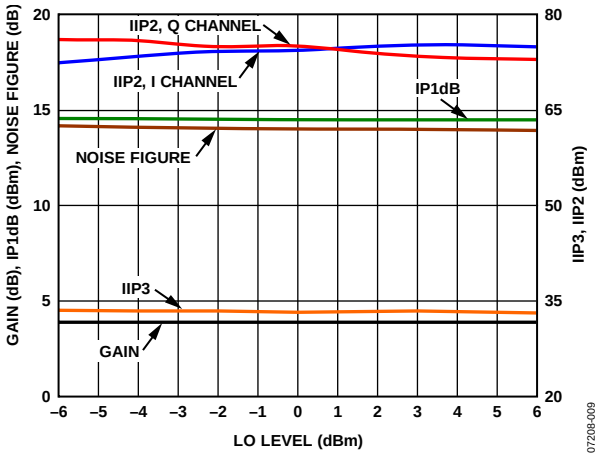

Figure 9. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{RF} = 900 MHz

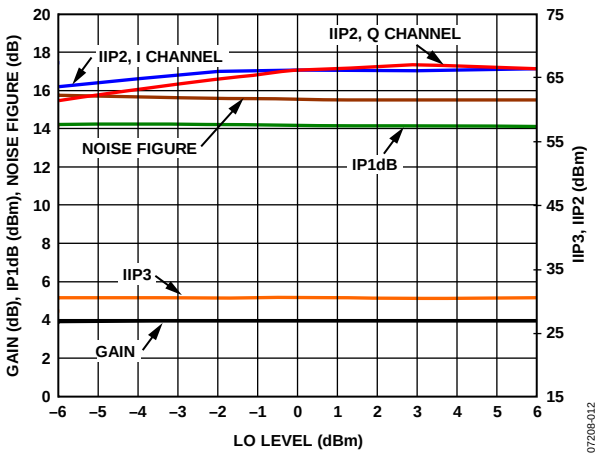

Figure 12. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{RF} = 1900 MHz

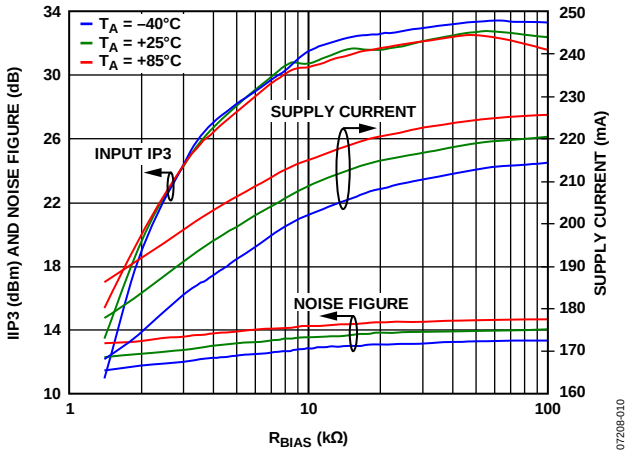

Figure 10. IIP3, Noise Figure, and Supply Current vs. R_{BIAS}, f_{RF} = 900 MHz

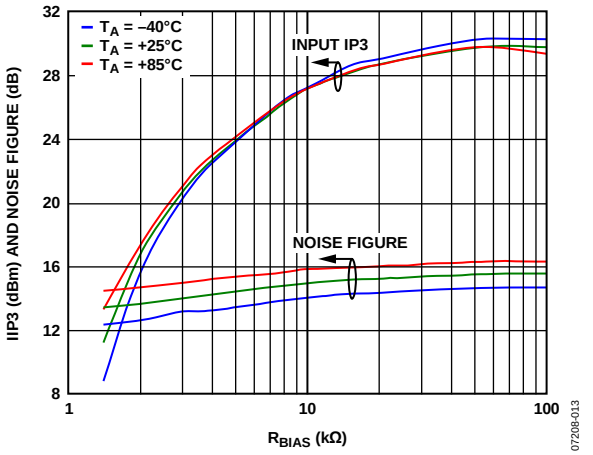

Figure 13. IIP3 and Noise Figure vs. R_{BIAS}, f_{RF} = 1900 MHz

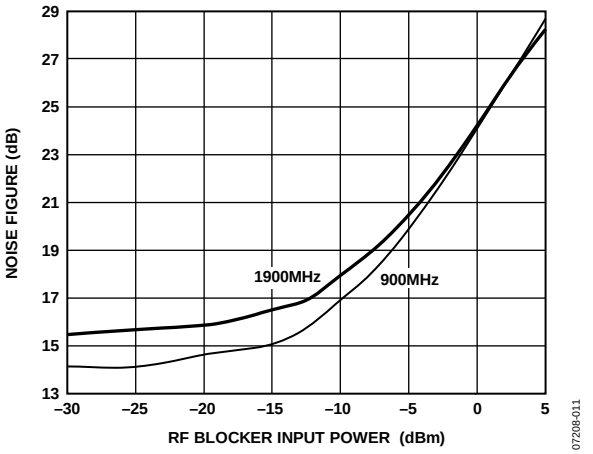

Figure 11. Noise Figure vs. Input Blocker Level, f_{RF} = 900 MHz, 1900 MHz (RF Blocker 5 MHz Offset)

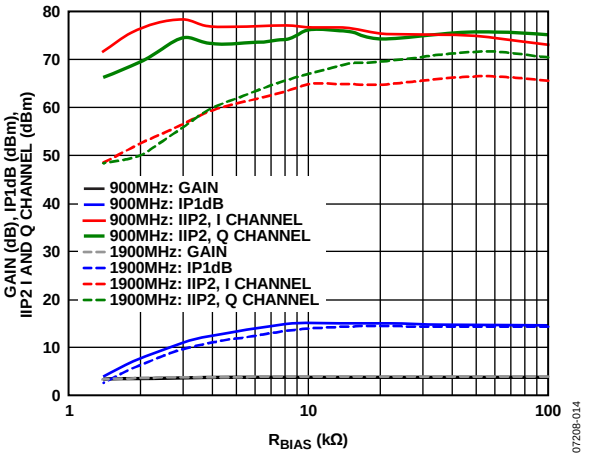

Figure 14. Conversion Gain, IP1dB, IIP2_I, and IIP2_Q vs. R_{BIAS}, f_{RF} = 900 MHz, 1900MHz

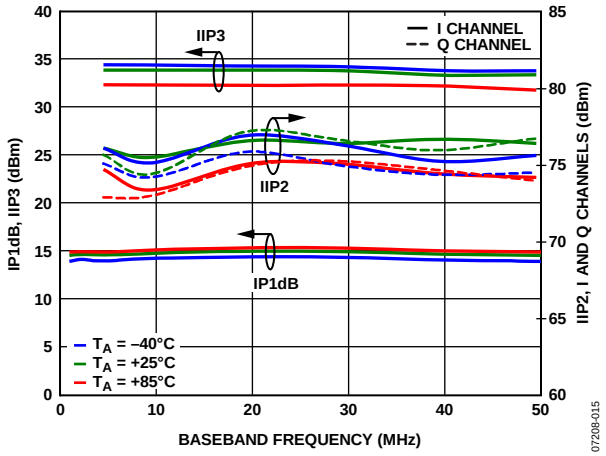

Figure 15. IP1dB, IIP3, and IIP2 vs. Baseband Frequency

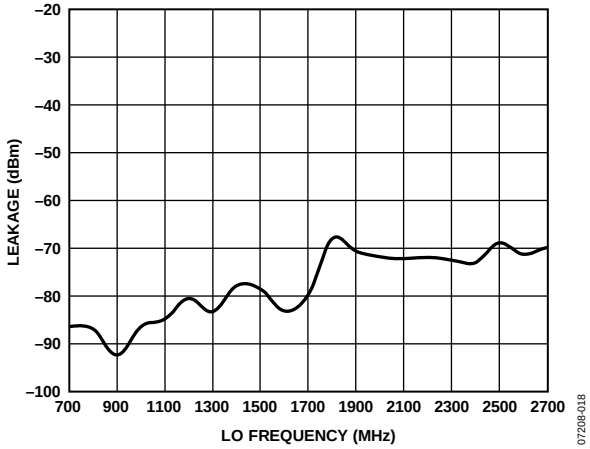

Figure 18. LO-to-RF Leakage vs. LO Frequency

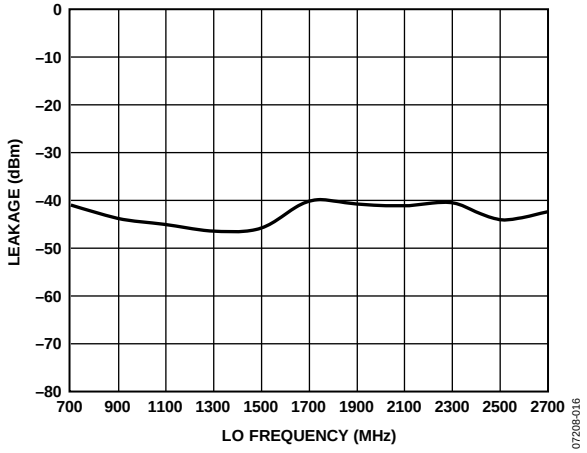

Figure 16. LO-to-BB Leakage vs. LO Frequency

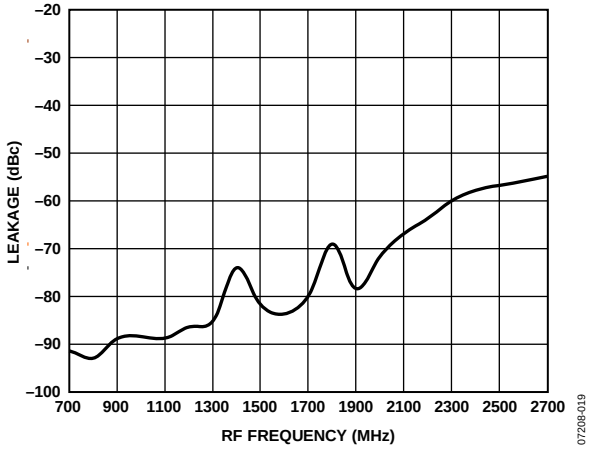

Figure 19. RF-to-LO Leakage vs. RF Frequency

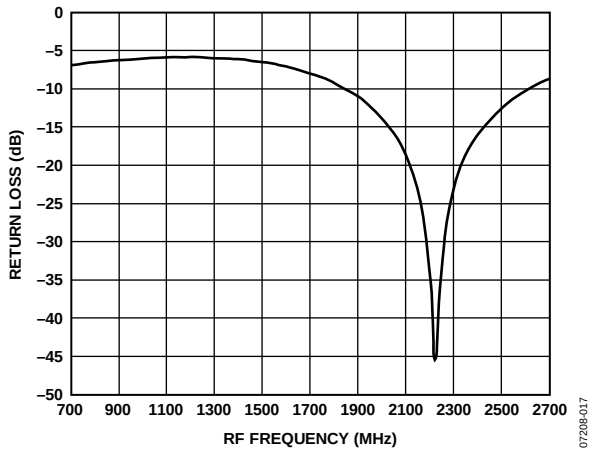

Figure 17. RF Port Return Loss vs. RF Frequency Measured on a Characterization Board through an ETC1-1-13 Balun with 33 nH Bias Inductors

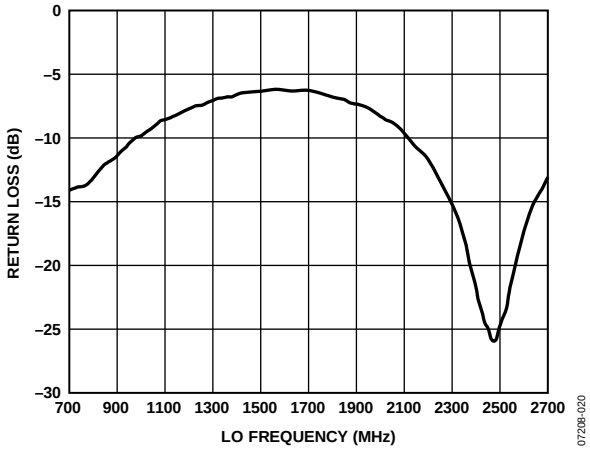

Figure 20. LO Port Return Loss vs. LO Frequency Measured on Characterization Board through an ETC1-1-13 Balun

DISTRIBUTIONS FOR f_{RF} = 900 MHz

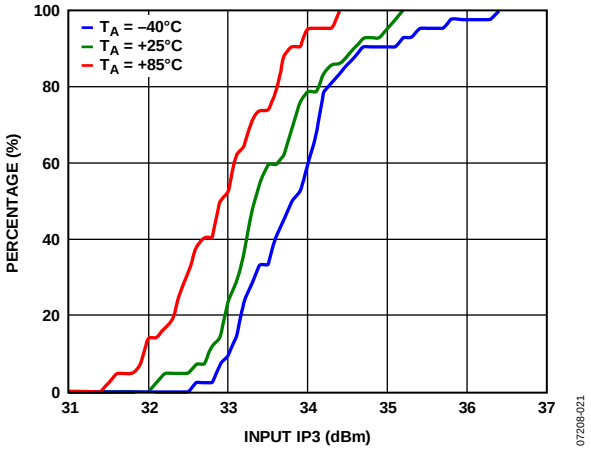

Figure 21. IIP3 Distributions, f_{RF} = 900 MHz

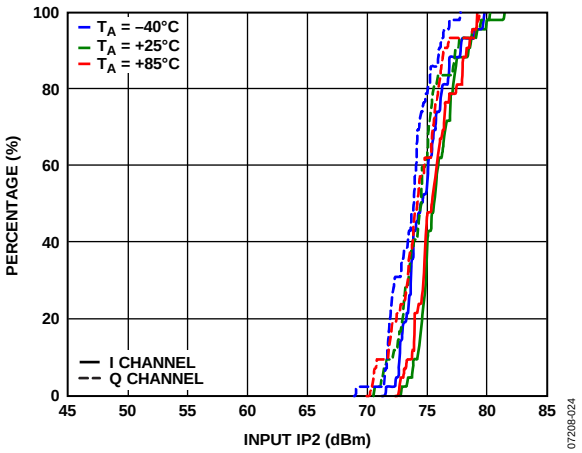

Figure 24. IIP2 Distributions for I Channel and Q Channel, f_{RF} = 900 MHz

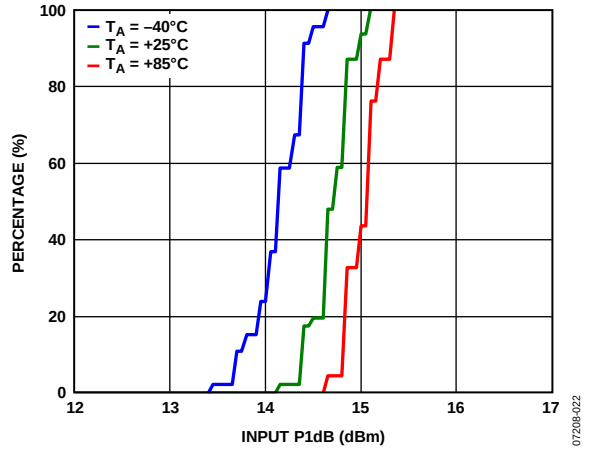

Figure 22. IP1dB Distributions, f_{RF} = 900 MHz

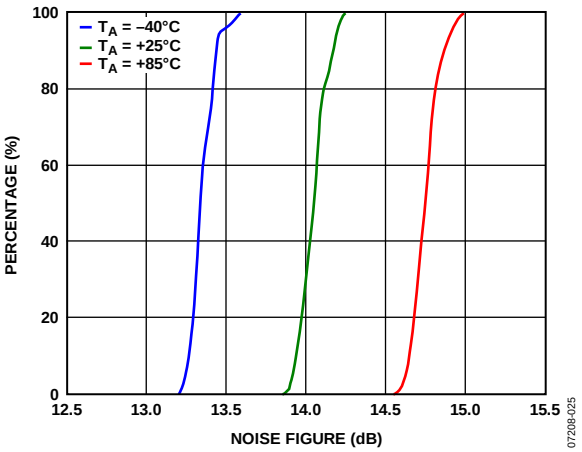

Figure 25. Noise Figure Distributions, f_{RF} = 900 MHz

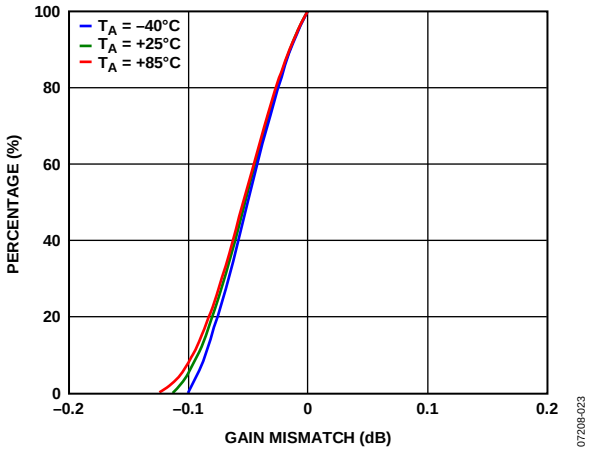

Figure 23. IQ Gain Mismatch Distributions, f_{RF} = 900 MHz

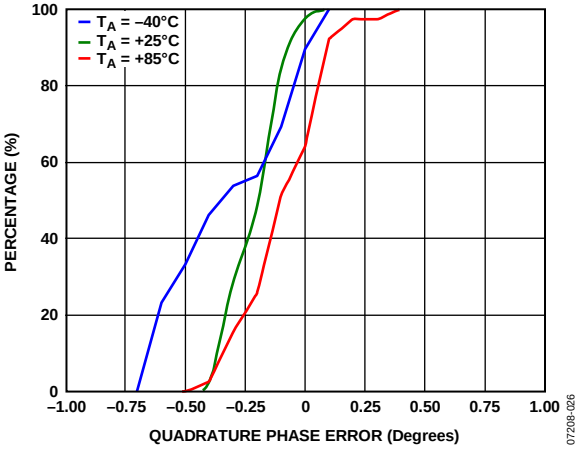

Figure 26. IQ Quadrature Phase Error Distributions, f_{RF} = 900 MHz

DISTRIBUTIONS FOR f_{RF} = 1900 MHz

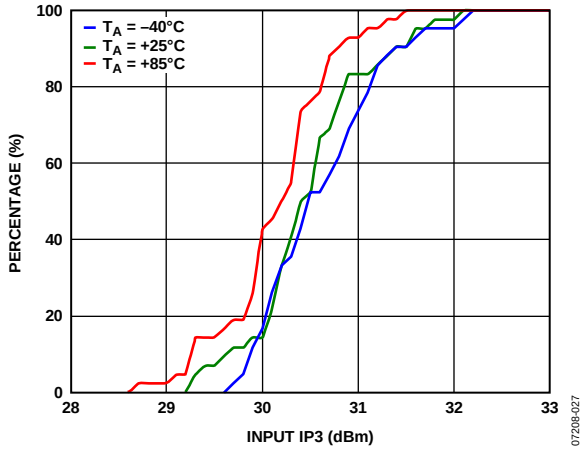

Figure 27. IIP3 Distributions, f_{RF} = 1900 MHz

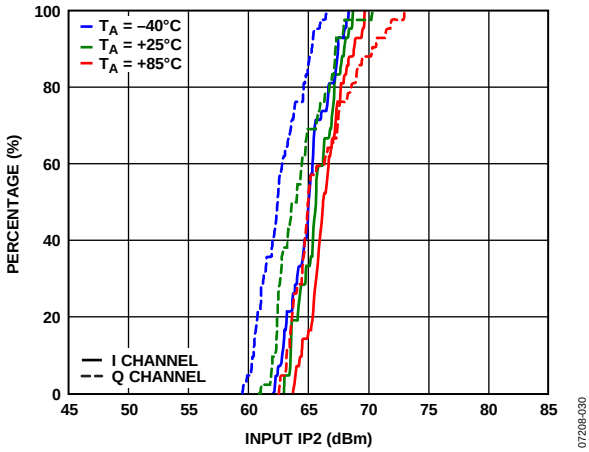

Figure 30. IIP2 Distributions for I Channel and Q Channel, f_{RF} = 1900 MHz

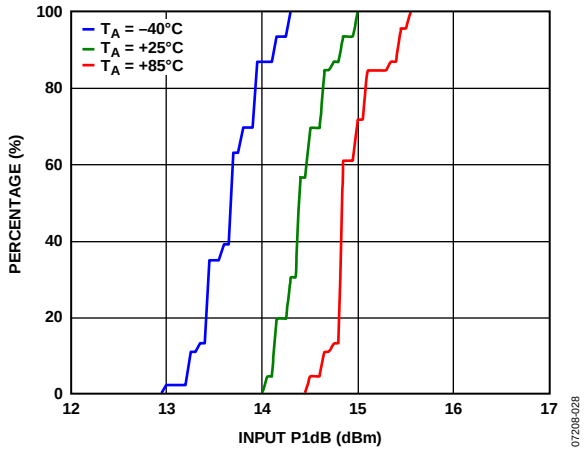

Figure 28. IP1dB Distributions, f_{RF} = 1900 MHz

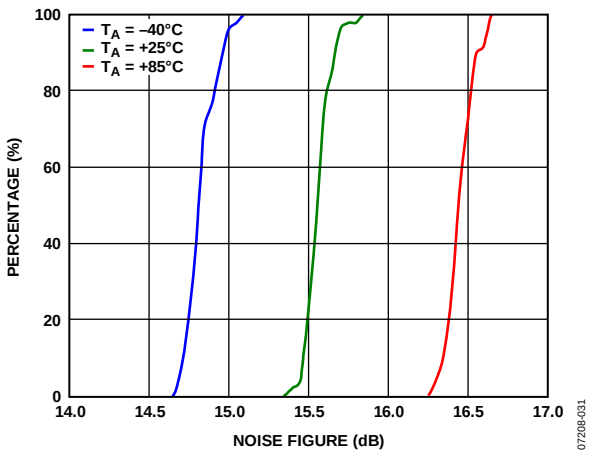

Figure 31. Noise Figure Distributions, f_{RF} = 1900 MHz

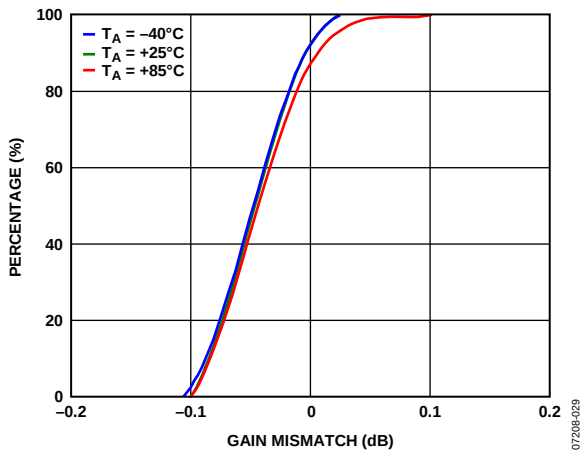

Figure 29. IQ Gain Mismatch Distributions, f_{RF} = 1900 MHz

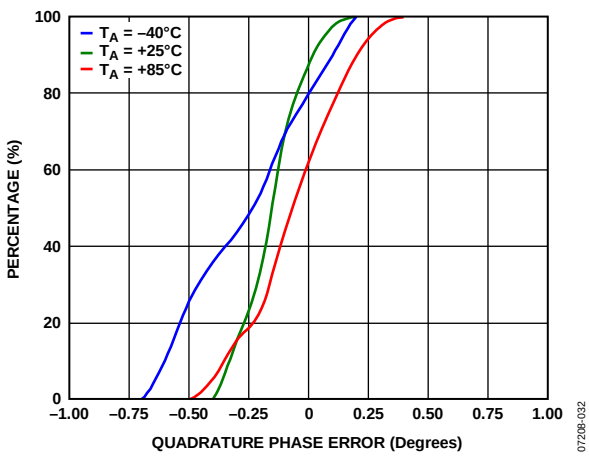

Figure 32. IQ Quadrature Phase Error Distributions, f_{RF} = 1900 MHz

DISTRIBUTIONS FOR f_{RF} = 2700 MHz

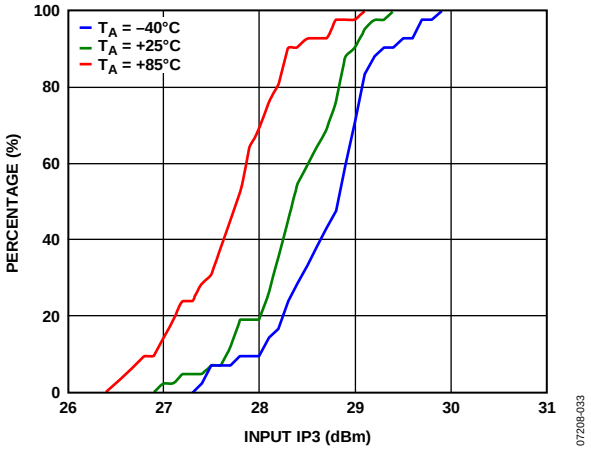

Figure 33. IIP3 Distributions, f_{RF} = 2700 MHz

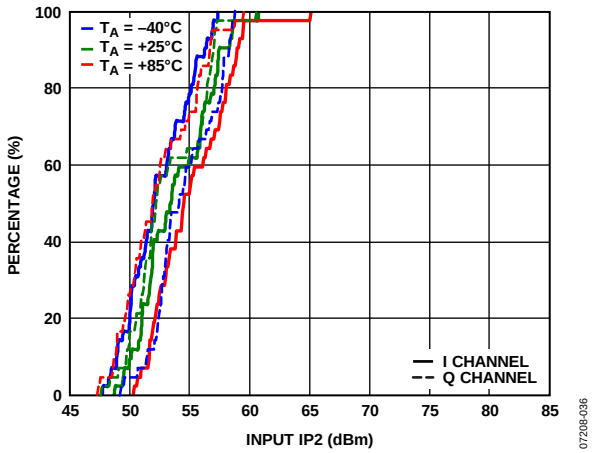

Figure 36. IIP2 Distributions for I Channel and Q Channel, f_{RF} = 2700 MHz

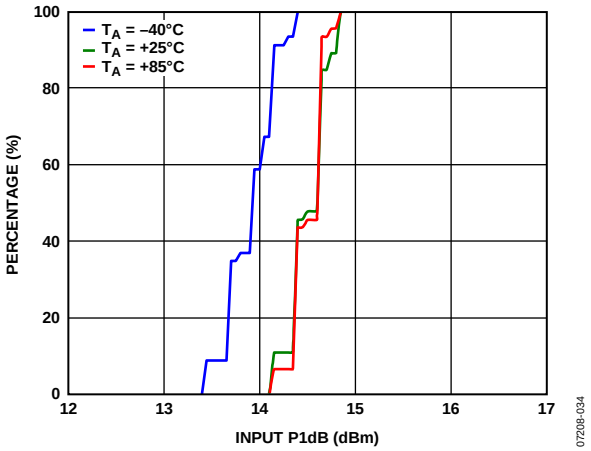

Figure 34. IP1dB Distributions, f_{RF} = 2700 MHz

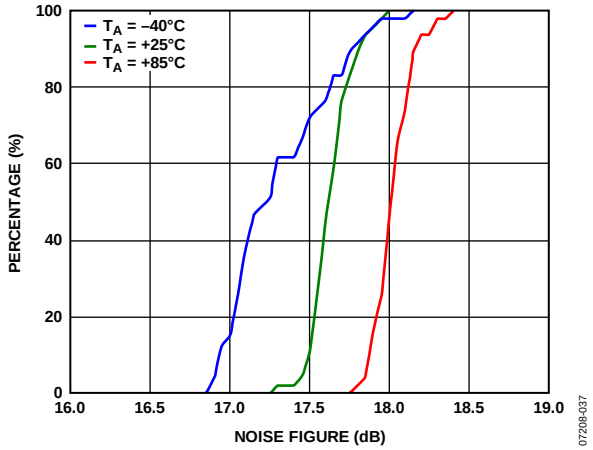

Figure 37. Noise Figure Distributions, f_{RF} = 2700 MHz

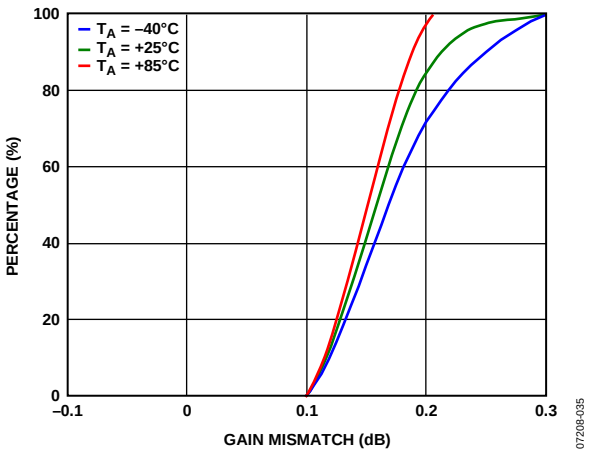

Figure 35. IQ Gain Mismatch Distributions, f_{RF} = 2700 MHz

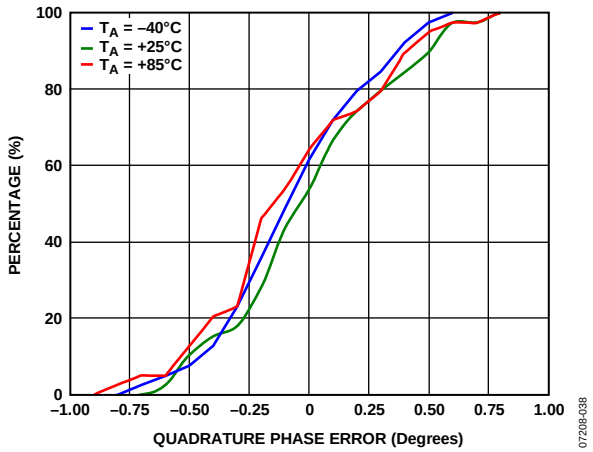

Figure 38. IQ Quadrature Phase Error Distributions, f_{RF} = 2700 MHz

CIRCUIT DESCRIPTION

The ADL5382 can be divided into five sections: the local oscillator (LO) interface, the RF voltage-to-current (V-to-I) converter, the mixers, the differential emitter follower outputs, and the bias circuit. A detailed block diagram of the device is shown in Figure 39.

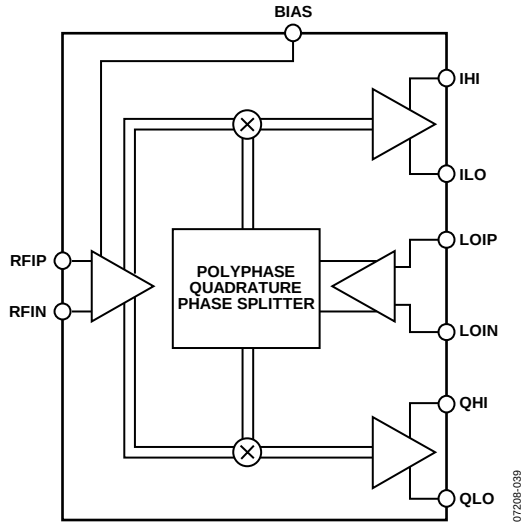

Figure 39. Block Diagram

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. RF signals are converted into currents by the V-to-I converters that feed into the two mixers. The differential I and Q outputs of the mixers are buffered via emitter followers. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of a polyphase quadrature splitter followed by a limiting amplifier. The LO input impedance is set by the polyphase, which splits the LO signal into two differential signals in quadrature. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal. For optimal performance, the LO inputs must be driven differentially.

V-TO-I CONVERTER

The differential RF input signal is applied to a resistively degenerated common base stage, which converts the differential input voltage to output currents. The output currents then modulate the two half frequency LO carriers in the mixer stage.

MIXERS

The ADL5382 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads that then feed into the subsequent emitter follower buffers.

EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off-chip. The output impedance is set by on-chip 25 Ω series resistors that yield a 50 Ω differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a 500 Ω differential load has 1 dB lower effective gain than a high (10 kΩ) differential load impedance.

BIAS CIRCUIT

A band gap reference circuit generates the proportional-to-absolute temperature (PTAT) as well as temperature-independent reference currents used by different sections. The mixer current can be reduced via an external resistor between the BIAS pin and ground. When the BIAS pin is open, the mixer runs at maximum current and therefore the greatest dynamic range. The mixer current can be reduced by placing a resistance to ground; therefore, reducing overall power consumption, noise figure, and IIP3. The effect on each of these parameters is shown in Figure 10, Figure 13, and Figure 14.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 41 shows the basic connections schematic for the ADL5382.

POWER SUPPLY

The nominal voltage supply for the ADL5382 is 5 V and is applied to the VPA, VPB, VPL, and VPX pins. Ground should be connected to the COM, CML, and CMRF pins. The exposed paddle on the underside of the package should also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, these layers should be stitched together with nine vias under the exposed paddle. The Application Note AN-772 discusses the thermal and electrical grounding of the LFCSP in detail. Each of the supply pins should be decoupled using two capacitors; recommended capacitor values are 100 pF and 0.1 µF.

LOCAL OSCILLATOR (LO) INPUT

For optimum performance, the LO port should be driven differentially through a balun. The recommended balun is the M/A-COM ETC1-1-13. The LO inputs to the device should be ac-coupled with 1000 pF capacitors. The LO port is designed for a broadband 50 Ω match from 700 MHz to 2.7 GHz. The LO return loss can be seen in Figure 20. Figure 40 shows the LO input configuration.

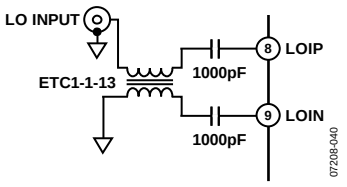

Figure 40. Differential LO Drive

The recommended LO drive level is between −6 dBm and +6 dBm. The applied LO frequency range is between 700 MHz and 2.7 GHz.

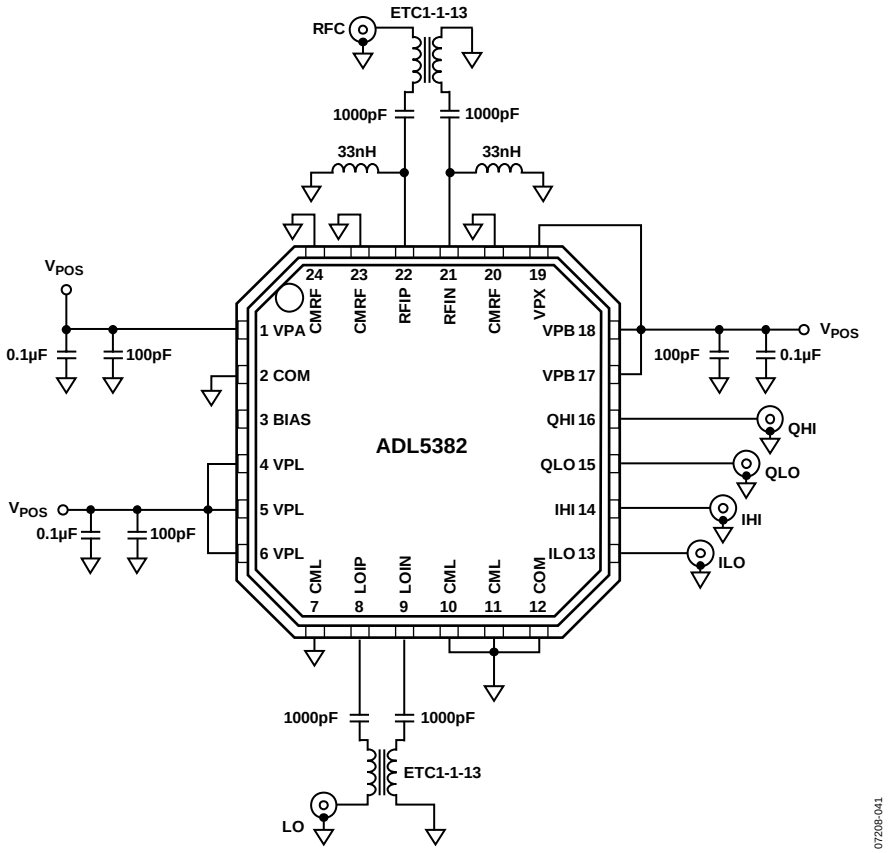

Figure 41. Basic Connections Schematic

RF INPUT

The RF inputs have a differential input impedance of approximately 50 Ω. For optimum performance, the RF port should be driven differentially through a balun. The recommended balun is the M/A-COM ETC1-1-13. The RF inputs to the device should be ac-coupled with 1000 pF capacitors. Ground-referenced choke inductors must also be connected to RFIP and RFIN (the recommended value is 33 nH, Coilcraft 0603CS-33NX) for appropriate biasing. Several important aspects must be taken into account when selecting an appropriate choke inductor for this application. First, the inductor must be able to handle the approximately 40 mA of standing dc current being delivered from each of the RF input pins (RFIP, RFIN). The suggested 0603 inductor has a 600 mA current rating. The purpose of the choke inductors is to provide a very low resistance dc path to ground and high ac impedance at the RF frequency so as not to affect the RF input impedance. A choke inductor that has a self-resonant frequency greater than the RF input frequency ensures that the choke is still looking inductive and therefore has a more predictable ac impedance (jωL) at the RF frequency. Figure 42 shows the RF input configuration.

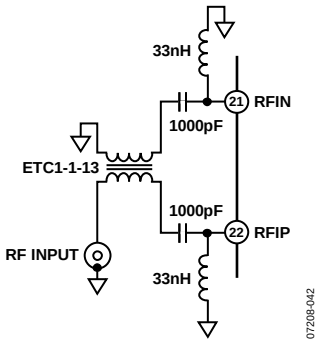

Figure 42. RF Input

The differential RF port return loss is characterized as shown in Figure 43.

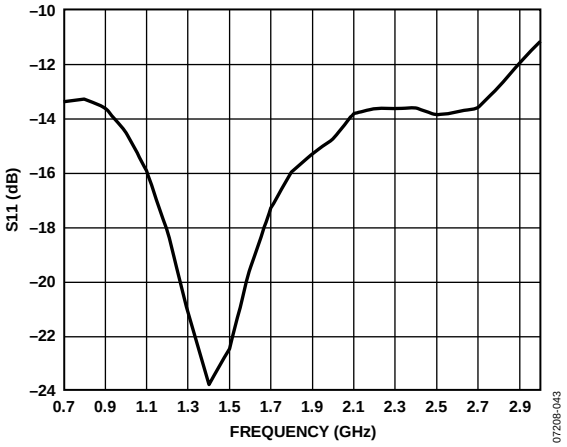

Figure 43. Differential RF Port Return Loss

BASEBAND OUTPUTS

The baseband outputs QHI, QLO, IHI, and ILO are fixed impedance ports. Each baseband pair has a 50 Ω differential output impedance. The outputs can be presented with differential loads as low as 200 Ω (with some degradation in gain) or high impedance differential loads (500 Ω or greater impedance yields the same excellent linearity) that is typical of an ADC. The TCM9-1 9:1 balun converts the differential IF output to single-ended. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The typical maximum linear voltage swing for these outputs is 2 V p-p differential. The bias level on these pins is equal to VPOS − 2.8 V. The output 3 dB bandwidth is 370 MHz. Figure 44 shows the baseband output configuration.

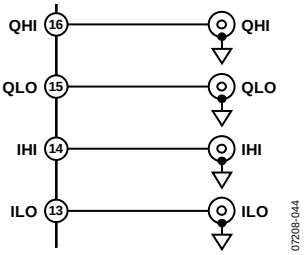

Figure 44. Baseband Output Configuration

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver would have all constellation points at the ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from the ideal locations.

The ADL5382 shows excellent EVM performance for various modulation schemes. Figure 45 shows the EVM performance of the ADL5382 with a 16 QAM, 200 kHz low IF.

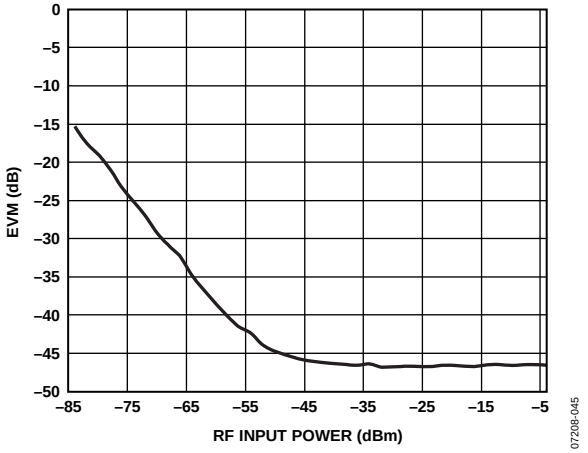

Figure 45. EVM, RF = 900 MHz, IF = 200 kHz vs. RF Input Power for a 16 QAM 160 ksym/s Signal

Figure 46 shows the zero-IF EVM performance of a 10 MHz IEEE 802.16e WiMAX signal through the ADL5382. The differential dc offsets on the ADL5382 are in the order of a few millivolts. However, ac coupling the baseband outputs with 10 µF capacitors eliminates dc offsets and enhances EVM performance. With a 10 MHz BW signal, 10 µF ac coupling capacitors with the 500 Ω differential load results in a high-pass corner frequency of ~64 Hz, which absorbs an insignificant amount of modulated signal energy from the baseband signal. By using ac-coupling capacitors at the baseband outputs, the dc offset effects, which can limit dynamic range at low input power levels, can be eliminated.

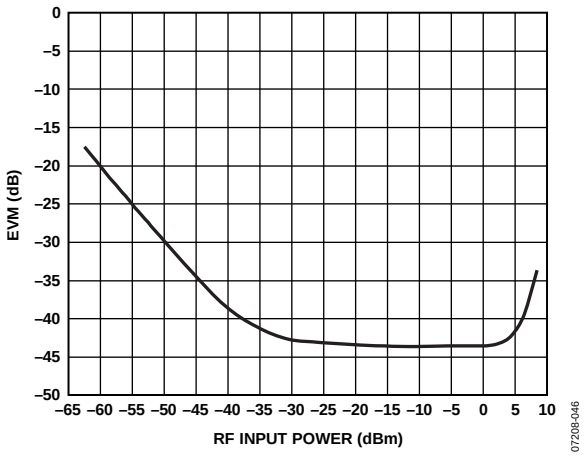

Figure 46. EVM, RF = 2.6 GHz, IF = 0 Hz vs. RF Input Power for a 16 QAM 10 MHz Bandwidth Mobile WiMAX Signal (AC-Coupled Baseband Outputs)

Figure 47 exhibits multiple W-CDMA low-IF EVM performance curves over a wide RF input power range into the ADL5382. In the case of zero-IF, the noise contribution by the vector signal analyzer becomes predominant at lower power levels, making it difficult to measure SNR accurately.

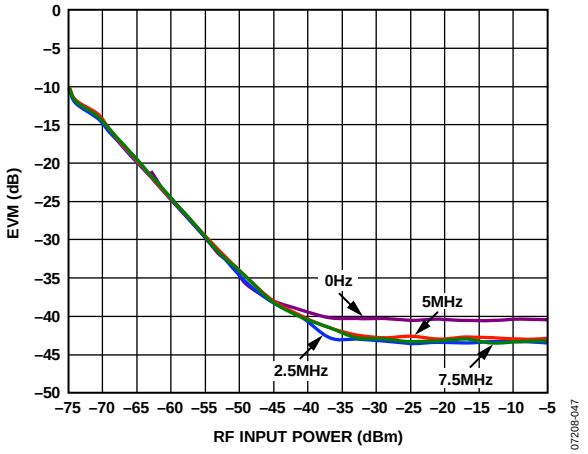

Figure 47. EVM, RF = 1900 MHz, IF = 0 Hz, 2.5 MHz, 5 MHz, and 7.5 MHz vs. RF Input Power for a W-CDMA Signal (AC-Coupled Baseband Outputs)

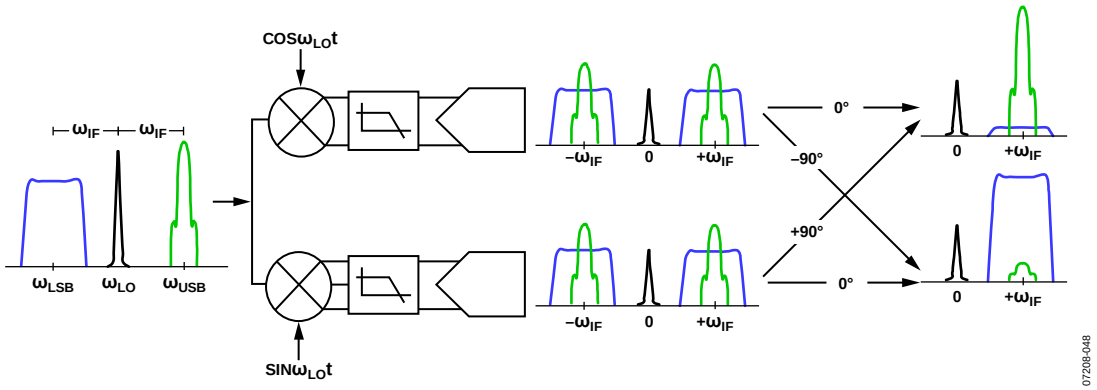

Figure 48. Illustration of the Image Problem

LOW IF IMAGE REJECTION

The image rejection ratio is the ratio of the intermediate frequency (IF) signal level produced by the desired input frequency to that produced by the image frequency. The image rejection ratio is expressed in decibels. Appropriate image rejection is critical because the image power can be much higher than that of the desired signal, thereby plaguing the down conversion process. Figure 48 illustrates the image problem. If the upper sideband (lower sideband) is the desired band, a 90° shift to the Q channel (I channel) cancels the image at the lower sideband (upper sideband). Phase and gain balance between I and Q channels are critical for high levels of image rejection.

Figure 49 shows the excellent image rejection capabilities of the ADL5382 for low IF applications, such as W-CDMA. The ADL5382 exhibits image rejection greater than 45 dB over a broad frequency range.

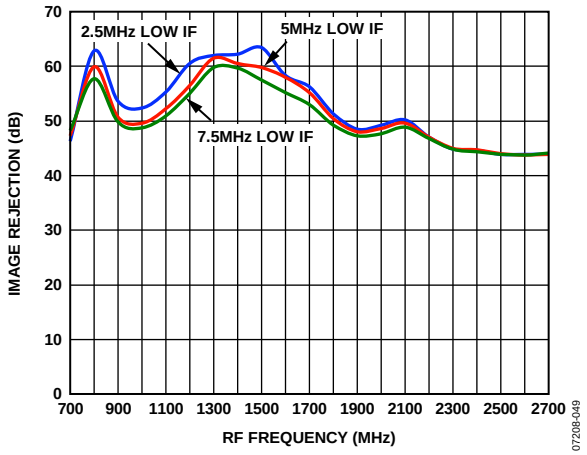

Figure 49. Image Rejection vs. RF Frequency for a W-CDMA Signal, IF = 2.5 MHz, 5 MHz, and 7.5 MHz

EXAMPLE BASEBAND INTERFACE

In most direct conversion receiver designs, it is desirable to select a wanted carrier within a specified band. The desired channel can be demodulated by tuning the LO to the appropriate carrier frequency. If the desired RF band contains multiple carriers of interest, the adjacent carriers would also be down converted to a lower IF frequency. These adjacent carriers can be problematic if they are large relative to the wanted carrier as they can overdrive the baseband signal detection circuitry. As a result, it is often necessary to insert a filter to provide sufficient rejection of the adjacent carriers.

It is necessary to consider the overall source and load impedance presented by the ADL5382 and ADC input to design the filter network. The differential baseband output impedance of the ADL5382 is 50 Ω. The ADL5382 is designed to drive a high impedance ADC input. It may be desirable to terminate the ADC input down to lower impedance by using a terminating resistor, such as 500 Ω. The terminating resistor helps to better define the input impedance at the ADC input at the cost of a slightly reduced gain (see the Circuit Description section for details on the emitter-follower output loading effects). The order and type of filter network depends on the desired high frequency rejection required, pass-band ripple, and group delay. Filter design tables provide outlines for various filter types and orders, illustrating the normalized inductor and capacitor values for a 1 Hz cutoff frequency and 1 Ω load. After scaling the normalized prototype element values by the actual desired cut-off frequency and load impedance, the series reactance elements are halved to realize the final balanced filter network component values.

As an example, a second-order Butterworth, low-pass filter design is shown in Figure 50 where the differential load impedance is 500 Ω and the source impedance of the ADL5382 is 50 Ω. The normalized series inductor value for the 10-to-1, load-to-source impedance ratio is 0.074 H, and the normalized shunt capacitor is 14.814 F. For a 10.9 MHz cutoff frequency, the single-ended equivalent circuit consists of a 0.54 µH series inductor followed by a 433 pF shunt capacitor.

The balanced configuration is realized as the 0.54 µH inductor is split in half to realize the network shown in Figure 50.

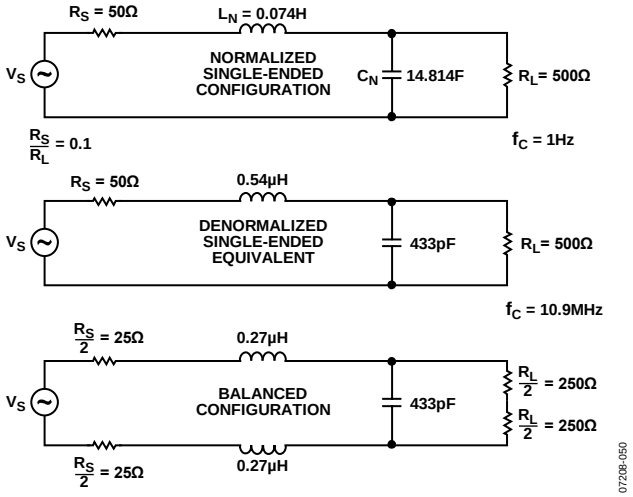

Figure 50. Second-Order Butterworth, Low-Pass Filter Design Example

A complete design example is shown in Figure 53. A sixth-order Butterworth differential filter having a 1.9 MHz corner frequency interfaces the output of the ADL5382 to that of an ADC input. The 500 Ω load resistor defines the input impedance of the ADC. The filter adheres to typical direct conversion W-CDMA applications, where 1.92 MHz away from the carrier IF frequency, 1 dB of rejection is desired and 2.7 MHz away 10 dB of rejection is desired.

Figure 51 and Figure 52 show the measured frequency response and group delay of the filter.

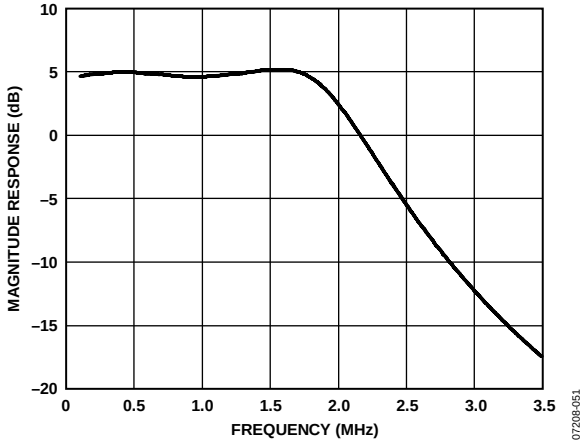

Figure 51. Sixth-Order Baseband Filter Response

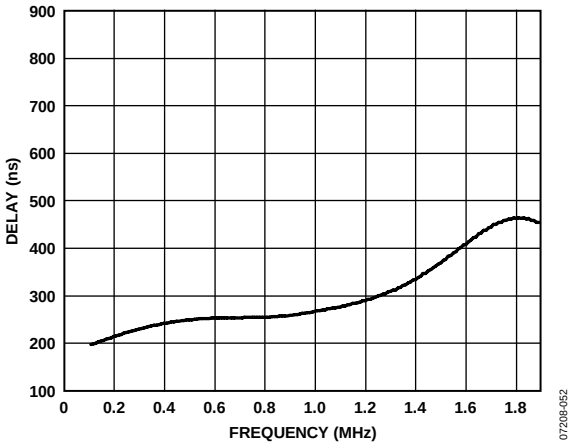

Figure 52. Sixth-Order Baseband Filter Group Delay

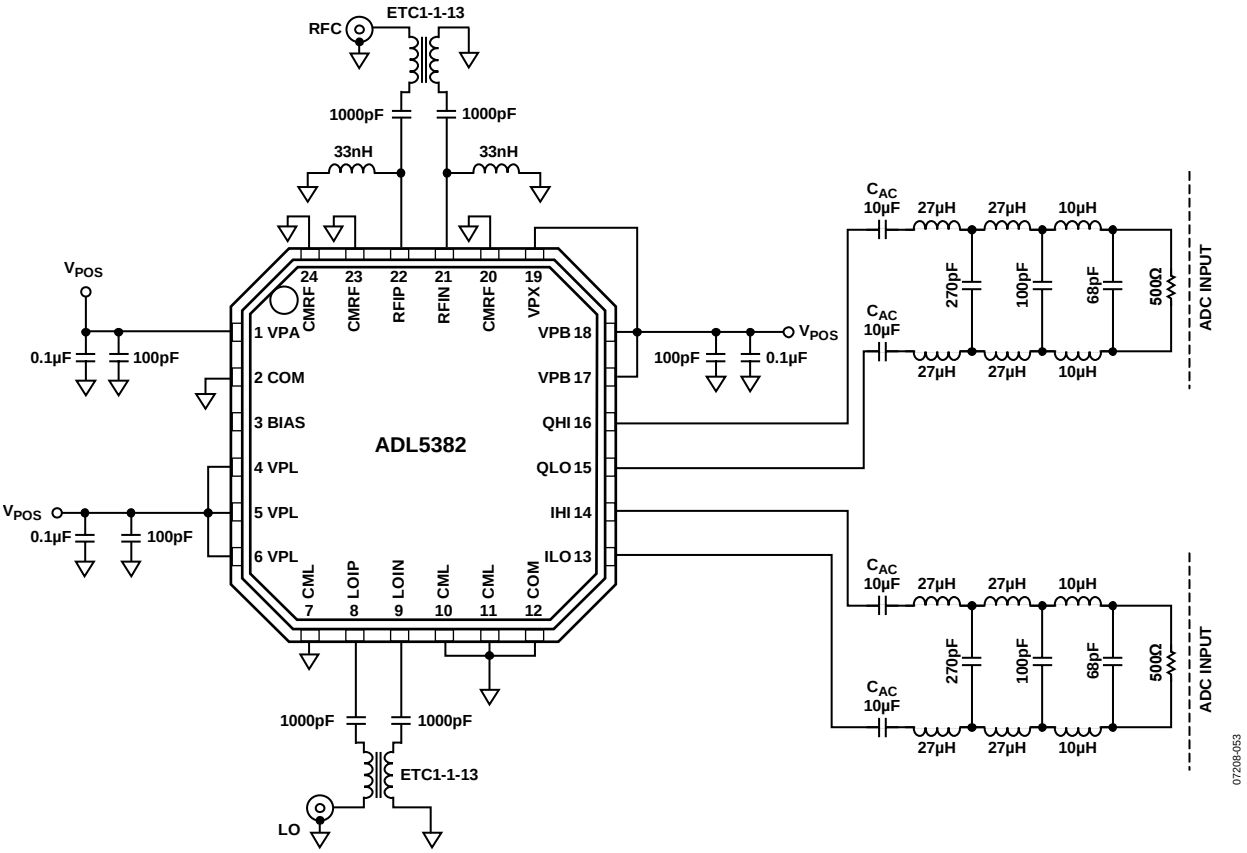

Figure 53. Sixth-Order Low-Pass Butterworth, Baseband Filter Schematic

As the load impedance of the filter increases, the filter design becomes more challenging in terms of meeting the required rejection and pass band specifications. In the previous W-CDMA example, the 500 Ω load impedance resulted in the design of a sixth-order filter that has relatively large inductor values and small capacitor values. If the load impedance is 200 Ω, the filter design becomes much more manageable. As shown in Figure 54, the resultant inductor and capacitor values become much more practical.

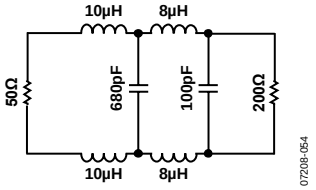

Figure 54. Fourth-Order Low-Pass W-CDMA Filter Schematic

Figure 55 and Figure 56 illustrate the magnitude response and group delay response of the fourth-order filter, respectively.

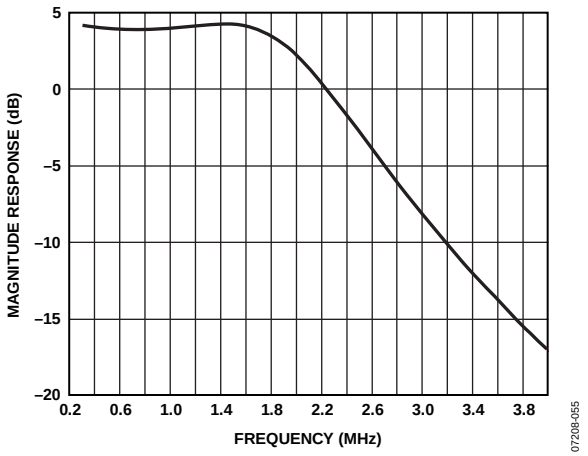

Figure 55. Fourth-Order Low-Pass W-CDMA Filter Magnitude Response

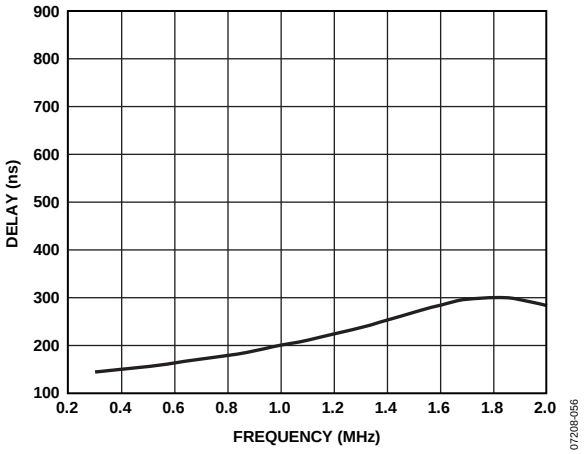

Figure 56. Fourth-Order Low-Pass W-CDMA Filter Group Delay Response

CHARACTERIZATION SETUPS

Figure 57 to Figure 59 show the general characterization bench setups used extensively for the ADL5382. The setup shown in Figure 59 was used to do the bulk of the testing and used sinusoidal signals on both the LO and RF inputs. An automated Agilent VEE program was used to control the equipment over the IEEE bus. This setup was used to measure gain, IP1dB, IIP2, IIP3, I/Q gain match, and quadrature error. The ADL5382 characterization board had a 9-to-1 impedance transformer on each of the differential baseband ports to do the differential-to-single-ended conversion, which presented a 450 Ω differential load to each baseband port, when interfaced with 50 Ω test equipment. For all measurements of the ADL5382, the loss of the RF input balun (the M/A-COM ETC1-1-13 was used on RF input during characterization) was de-embedded.

The two setups shown in Figure 57 and Figure 58 were used for making NF measurements. Figure 57 shows the setup for measuring NF with no blocker signal applied while Figure 58 was used to measure NF in the presence of a blocker. For both setups, the noise was measured at a baseband frequency of 10 MHz. For the case where a blocker was applied, the output blocker was at a 15 MHz baseband frequency. Note that great care must be taken when measuring NF in the presence of a blocker. The RF blocker generator must be filtered to prevent its noise (which increases with increasing generator output power) from swamping the noise contribution of the ADL5382. At least 30 dB of attention at the RF and image frequencies is desired. For example, assume a 915 MHz signal applied to the LO inputs of the ADL5382. To obtain a 15 MHz output blocker signal, the RF blocker generator is set to 930 MHz and the filters tuned such that there is at least 30 dB of attenuation from the generator at both the desired RF frequency (925 MHz) and the image RF frequency (905 MHz). Finally, the blocker must be removed from the output (by the 10 MHz low-pass filter) to prevent the blocker from swamping the analyzer.

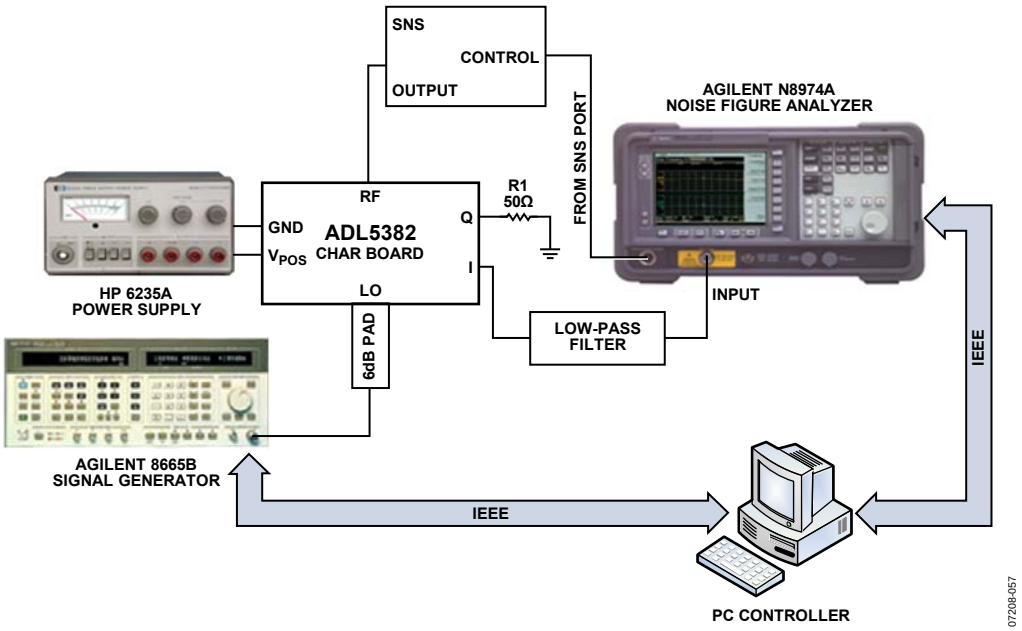

Figure 57. General Noise Figure Measurement Setup

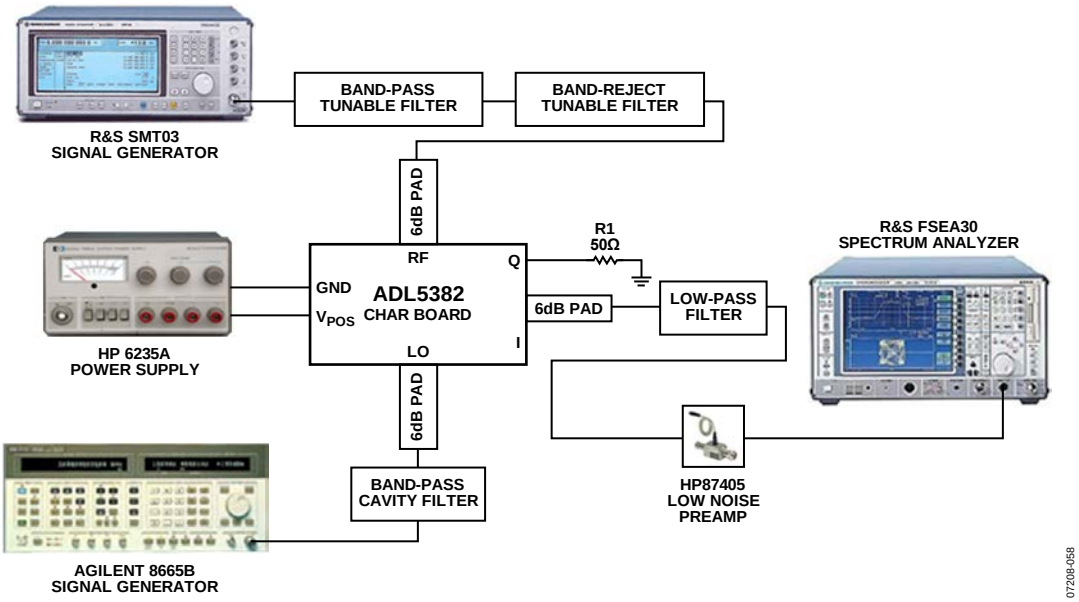

Figure 58. Measurement Setup for Noise Figure in the Presence of a Blocker

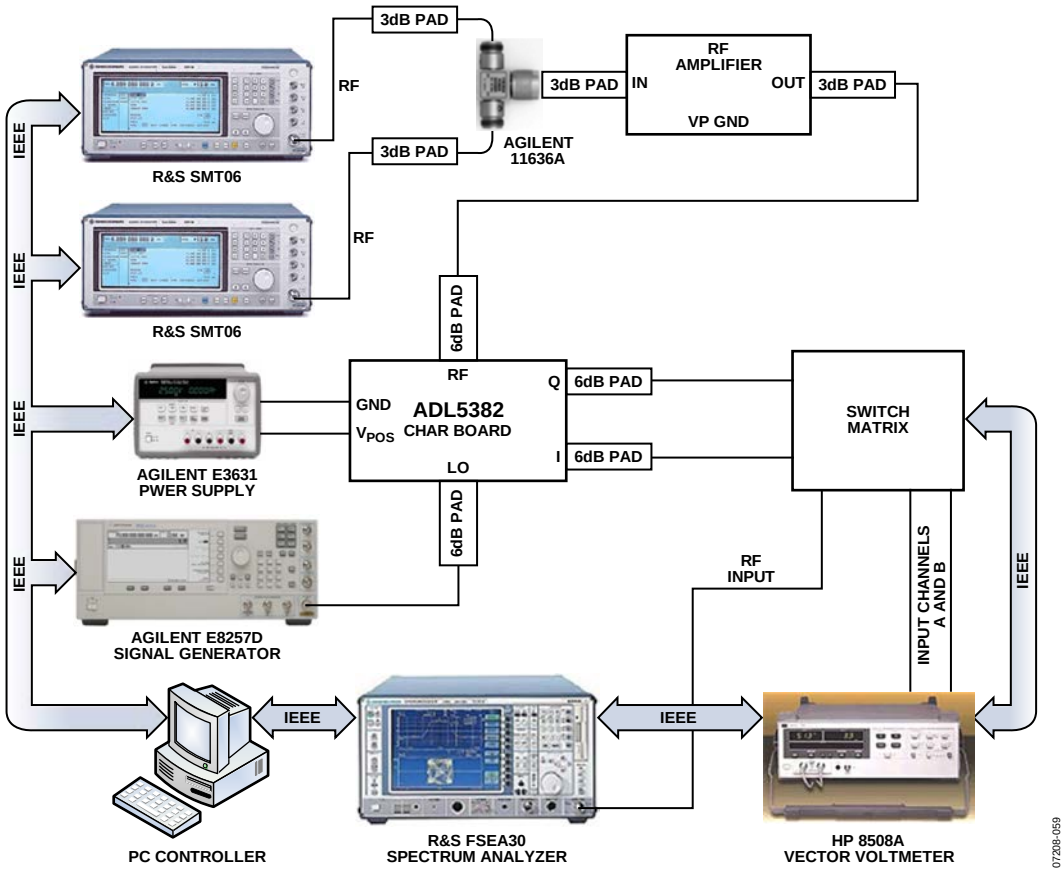

Figure 59. General Characterization Setup

EVALUATION BOARD

The ADL5382 evaluation board is available. The board can be used for single-ended or differential baseband analysis. The default configuration of the board is for single-ended baseband analysis.

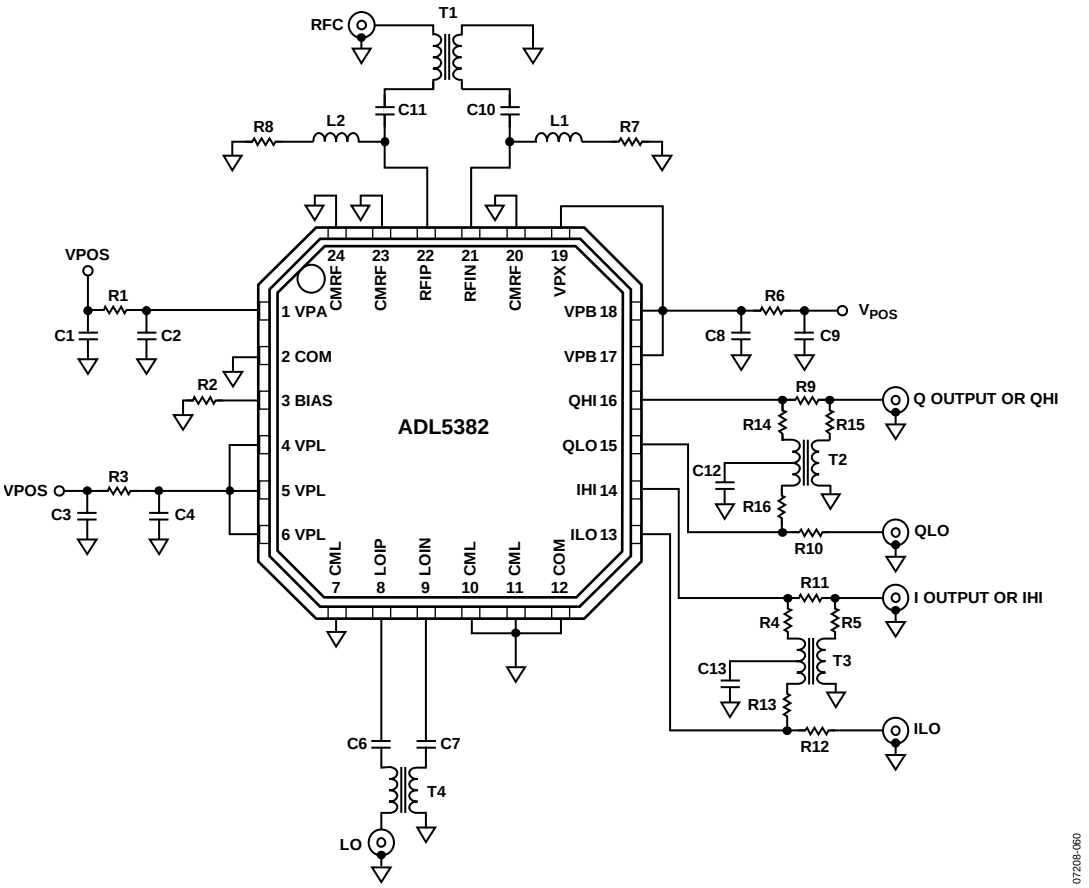

Figure 60. Evaluation Board Schematic

Table 4. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Power Supply and Ground Vector Pins.	Not applicable
R1, R3, R6	Power Supply Decoupling. Shorts or power supply decoupling resistors.	R1, R3, R6 = 0 Ω (0603)
C1, C2, C3, C4, C8, C9	These capacitors provide the required decoupling up to 2.7 GHz.	C2, C4, C8 = 100 pF (0402) C1, C3, C9 = 0.1 µF (0603)
C6, C7, C10, C11	AC Coupling Capacitors. These capacitors provide the required ac coupling from 700 MHz to 2.7 GHz.	C6, C10, C11 = 1000 pF (0402) C7 = open
R4, R5, R9 to R16	Single-Ended Baseband Output Path. This is the default configuration of the evaluation board. R14 to R16 and R4, R5, and R13 are populated for appropriate balun interface. R9, R10 and R11, R12 are not populated. Baseband outputs are taken from QHI and IHI. The user can reconfigure the board to use full differential baseband outputs. R9 to R12 provide a means to bypass the 9:1 TCM9-1 transformer to allow for differential baseband outputs. Access the differential baseband signals by populating R9 to R12 with 0 Ω and not populating R4, R5, R13 to R16. This way the transformer does not need to be removed. The baseband outputs are taken from the SMAs of Q_HI, Q_LO, I_HI, and I_LO.	R4, R5, R13 to R16 = 0 Ω (0402) R9 to R12 = open
L1, L2, R7, R8	Input Biasing. Inductance and resistance sets the input biasing of the common base input stage. The default value is 33 nH.	L1, L2 = 33 nH (0603CS-33NX, Coilcraft) R7, R8 = 0 Ω (0402)
T2, T3	IF Output Interface. TCM9-1 converts a differential high impedance IF output to a single-ended output. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The center tap can be decoupled through a capacitor to ground.	T2, T3 = TCM9-1, 9:1 (Mini-Circuits)
C12, C13	Decoupling Capacitors. C12 and C13 are the decoupling capacitors used to reject noise on the center tap of the TCM9-1.	C12, C13 = 0.1 µF (0402)
T4	LO Input Interface. The LO is driven differentially. ETC1-1-13 is a 1:1 RF balun that converts the single-ended RF input to differential signal.	T4 = ETC1-1-13, 1:1 (M/A-COM)
T1	RF Input Interface. ETC1-1-13 is a 1:1 RF balun that converts the single-ended RF input to differential signal.	T1 = ETC1-1-13, 1:1 (M/A-COM)
R2	R_{BIAS}. Optional bias setting resistor. See the Bias Circuit section to see how to use this feature.	R2 = open

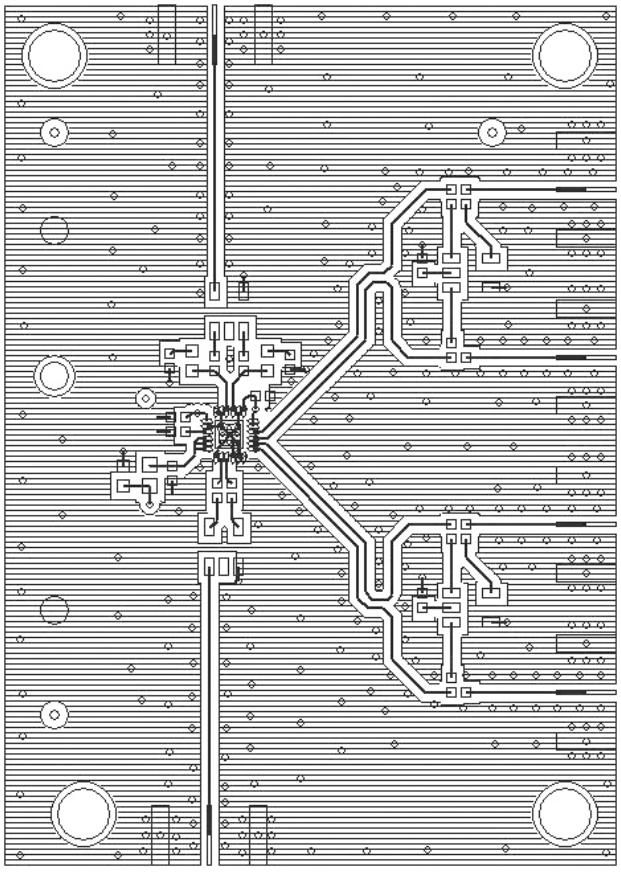

Figure 61. Evaluation Board Top Layer

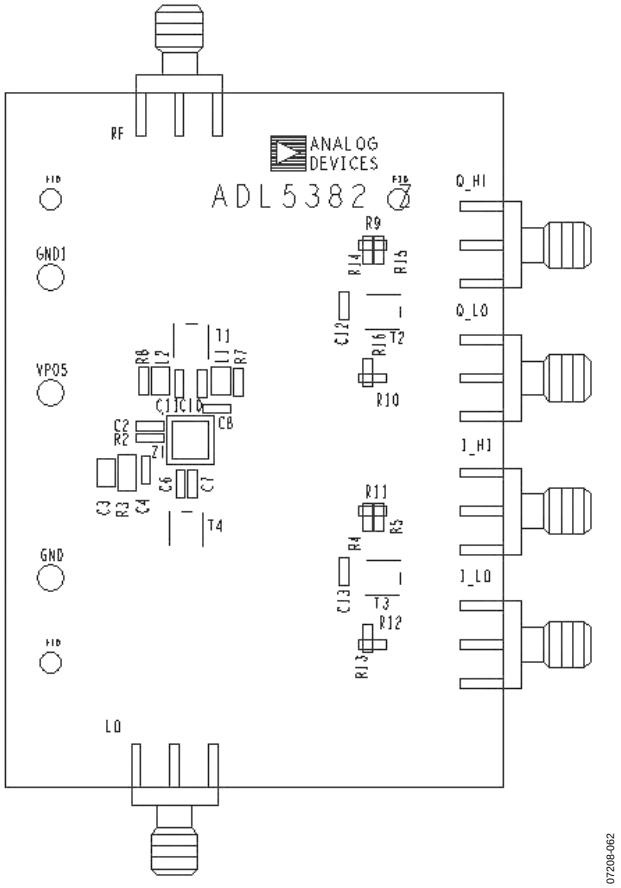

Figure 62. Evaluation Board Top Layer Silkscreen

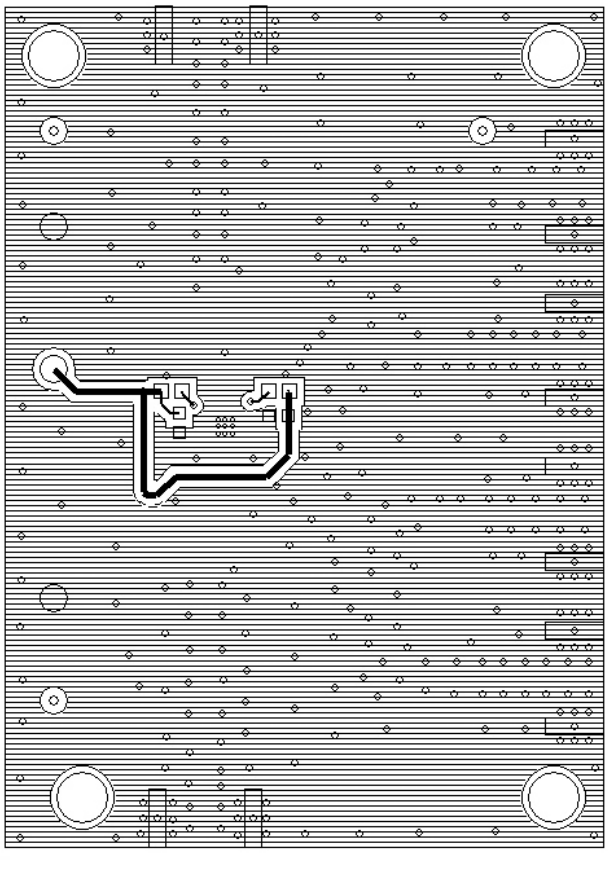

Figure 63. Evaluation Board Bottom Layer

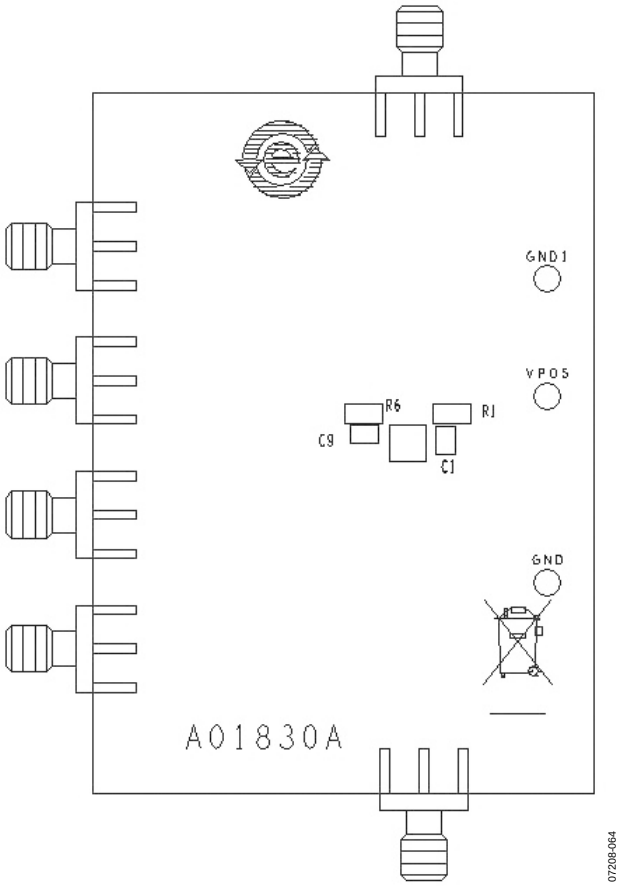

Figure 64. Evaluation Board Bottom Layer Silkscreen

OUTLINE DIMENSIONS

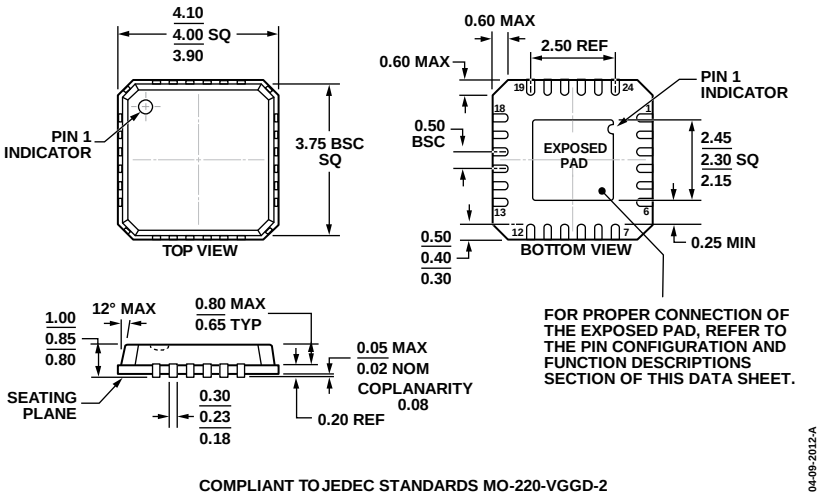

Figure 65. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5382ACPZ-R7	–40°C to +85°C	24-Lead LFCSP_VQ, 7″ Tape and Reel	CP-24-2	1,500
ADL5382ACPZ-WP	–40°C to +85°C	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2	64
ADL5382-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES