

ADG781/ADG782/ADG783—SPECIFICATIONS

($V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$ unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On Resistance (R _{ON})	2.5		Ω typ	V _S = 0 V to V _{DD} , I _S = −10 mA;
	4	4.5	Ω max	Test Circuit 1
On-Resistance Match Between Channels (ΔR _{ON})		0.05	Ω typ	V _S = 0 V to V _{DD} , I _S = −10 mA
		0.4	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ	V _S = 0 V to V _{DD} , I _S = −10 mA
		1.0	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = 5.5 V;
	±0.1	±0.2	nA max	V _S = 4.5 V/1 V, V _D = 1 V/4.5 V;
Drain OFF Leakage I _D (OFF)	±0.01		nA typ	Test Circuit 2
	±0.1	±0.2	nA max	V _S = 4.5 V/1 V, V _D = 1 V/4.5 V;
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	Test Circuit 2
	±0.1	±0.2	nA max	V _S = V _D = 1 V, or 4.5 V;
				Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current				
I _{INL} or I _{INH}	0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	11	16	ns typ	R _L = 300 Ω, C _L = 35 pF,
			ns max	V _S = 3 V; Test Circuit 4
t _{OFF}	6	10	ns typ	R _L = 300 Ω, C _L = 35 pF,
			ns max	V _S = 3 V; Test Circuit 4
Break-Before-Make Time Delay, t _D	6		ns typ	R _L = 300 Ω, C _L = 35 pF,
(ADG783 Only)		1	ns min	V _{S1} = V _{S2} = 3 V; Test Circuit 5
Charge Injection	3		pC typ	V _S = 2 V; R _S = 0 Ω, C _L = 1 nF;
				Test Circuit 6
Off Isolation	−58		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz
	−78		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 7
Channel-to-Channel Crosstalk	−90		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz;
				Test Circuit 8
Bandwidth −3 dB	200		MHz typ	R _L = 50 Ω, C _L = 5 pF; Test Circuit 9
C _S (OFF)	10		pF typ	f = 1 MHz
C _D (OFF)	10		pF typ	f = 1 MHz
C _D , C _S (ON)	22		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	0.001		μA typ	V _{DD} = 5.5 V
		1.0	μA max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature ranges are as follows: B Version: -40°C to $+85^{\circ}\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹(V_{DD} = 3 V ±10%, GND = 0 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On Resistance (R _{ON})	5	5.5	Ω typ	V _S = 0 V to V _{DD} , I _S = –10 mA; Test Circuit 1
		10	Ω max	
On-Resistance Match Between Channels (ΔR _{ON})	0.1		Ω typ	V _S = 0 V to V _{DD} , I _S = –10 mA
		0.5	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})		2.5	Ω typ	V _S = 0 V to V _{DD} , I _S = –10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = 3.3 V; V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2
	±0.1	±0.2	nA max	
Drain OFF Leakage I _D (OFF)	±0.01		nA typ	V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2
	±0.1	±0.2	nA max	
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	V _S = V _D = 1 V, or 3 V; Test Circuit 3
	±0.1	±0.2	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current I _{INL} or I _{INH}	0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	13		ns typ	R _L = 300 Ω, C _L = 35 pF, V _S = 2 V; Test Circuit 4
		20	ns max	
t _{OFF}	7		ns typ	R _L = 300 Ω, C _L = 35 pF, V _S = 2 V; Test Circuit 4
		12	ns max	
Break-Before-Make Time Delay, t _D (ADG783 Only)	7		ns typ	R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 2 V; Test Circuit 5
		1	ns min	
Charge Injection	3		pC typ	V _S = 1.5 V; R _S = 0 Ω, C _L = 1 nF; Test Circuit 6
Off Isolation	–58		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz
	–78		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	–90		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; Test Circuit 8
Bandwidth –3 dB	200		MHz typ	R _L = 50 Ω, C _L = 5 pF; Test Circuit 9
C _S (OFF)	10		pF typ	f = 1 MHz
C _D (OFF)	10		pF typ	f = 1 MHz
C _D , C _S (ON)	22		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	0.001		μA typ	V _{DD} = 3.3 V Digital Inputs = 0 V or 3.3 V
		1.0	μA max	

NOTES

¹Temperature ranges are as follows: B Version: –40°C to +85°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG781/ADG782/ADG783

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted.)

V _{DD} to GND	−0.3 V to +6 V
Analog, Digital Inputs ²	−0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Chip Scale Package	
θ _{JA} Thermal Impedance	32°C/W

Lead Temperature, Soldering (10 sec)	300°C
IR Reflow (<20 sec)	235°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

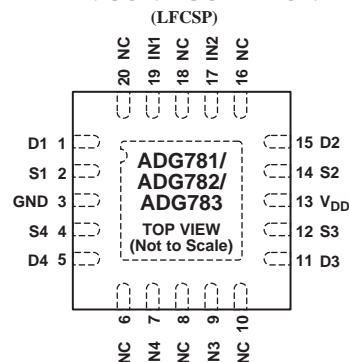
Table I. Truth Table (ADG781/ADG782)

ADG781 In	ADG782 In	Switch Condition
0	1	ON
1	0	OFF

Table II. Truth Table (ADG783)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

PIN CONFIGURATION



NOTES

1. NC = NO CONNECT.
2. EXPOSED PAD TIED TO SUBSTRATE, GND.

CAUTION

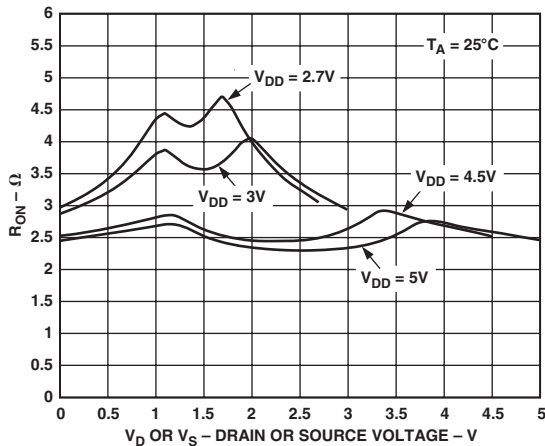
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG781/ADG782/ADG783 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



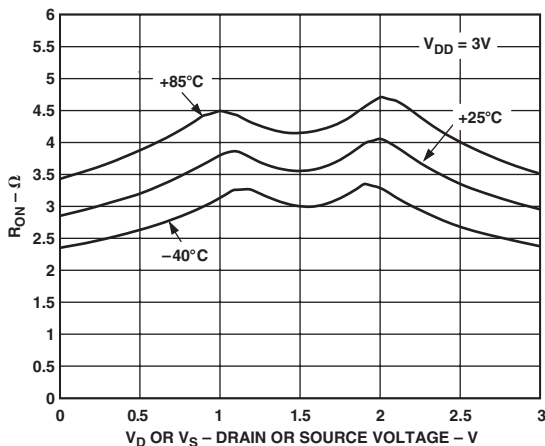
TERMINOLOGY

V_{DD}	Most positive power supply potential.	C_D, C_S (ON)	“ON” switch capacitance.
GND	Ground (0 V) reference.	t_{ON}	Delay between applying the digital control input and the output switching on.
S	Source terminal. May be an input or output.	t_{OFF}	Delay between applying the digital control input and the output switching off.
D	Drain terminal. May be an input or output.	t_D	“OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another (ADG783 only).
IN	Logic control input.	Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
R_{ON}	Ohmic resistance between D and S.	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
ΔR_{ON}	On-resistance match between any two channels (i.e., R_{ON} max and R_{ON} min).	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.	On Response	The frequency response of the “ON” switch.
I_S (OFF)	Source leakage current with the switch “OFF.”	On Loss	The loss due to the on resistance of the switch.
I_D (OFF)	Drain leakage current with the switch “OFF.”		
I_D, I_S (ON)	Channel leakage current with the switch “ON.”		
V_D (V_S)	Analog voltage on terminals D, S.		
C_S (OFF)	“OFF” switch source capacitance.		
C_D (OFF)	“OFF” switch drain capacitance.		

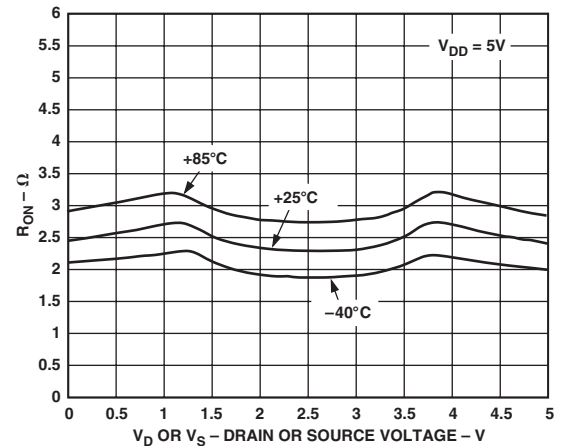
Typical Performance Characteristics



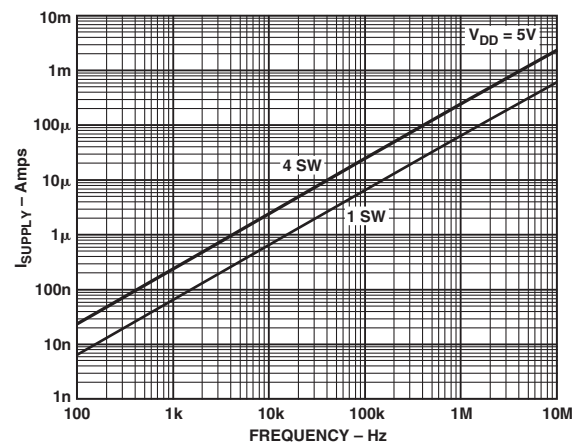
TPC 1. On Resistance as a Function of V_D (V_S)



TPC 2. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 3V$

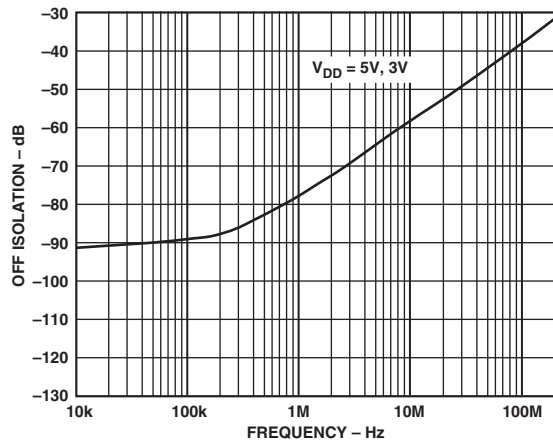


TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 5V$

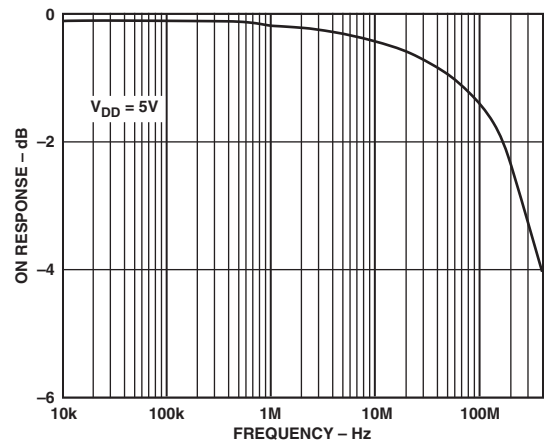


TPC 4. Supply Current vs. Input Switching Frequency

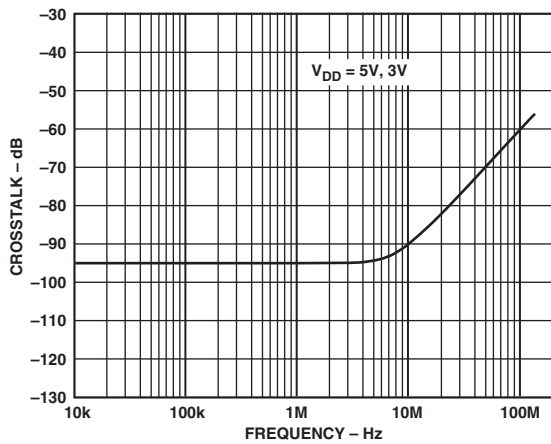
ADG781/ADG782/ADG783



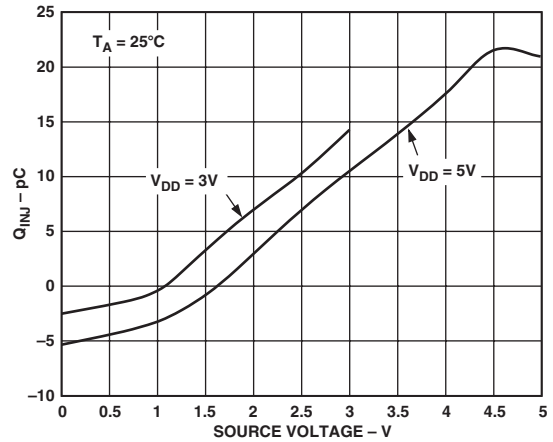
TPC 5. Off Isolation vs. Frequency



TPC 7. On Response vs. Frequency



TPC 6. Crosstalk vs. Frequency



TPC 8. Charge Injection vs. Source Voltage

APPLICATIONS

Figure 1 illustrates a photodetector circuit with programmable gain. An AD820 is used as the output operational amplifier. With the resistor values shown in the circuit, and using different combinations of the switches, gain in the range of 2 to 16 can be achieved.

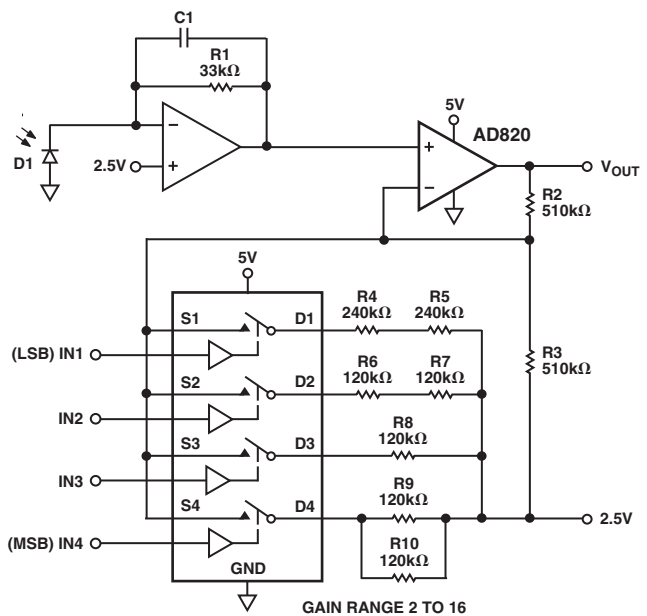
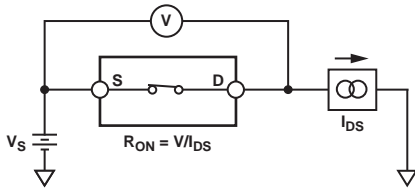
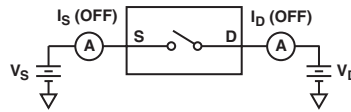


Figure 1. Photodetector Circuit with Programmable Gain

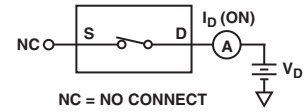
Test Circuits



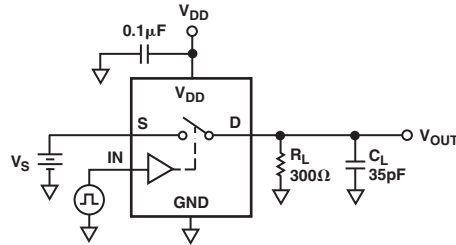
Test Circuit 1. On Resistance



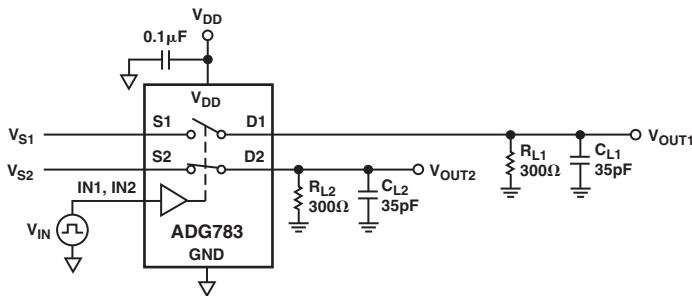
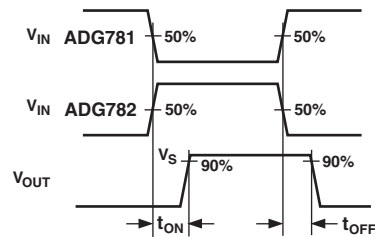
Test Circuit 2. Off Leakage



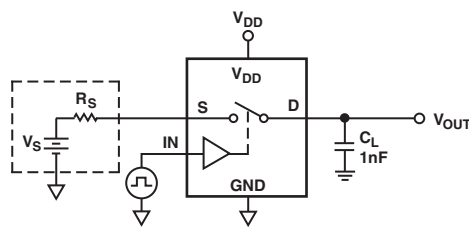
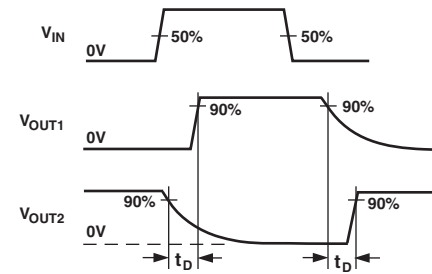
Test Circuit 3. On Leakage



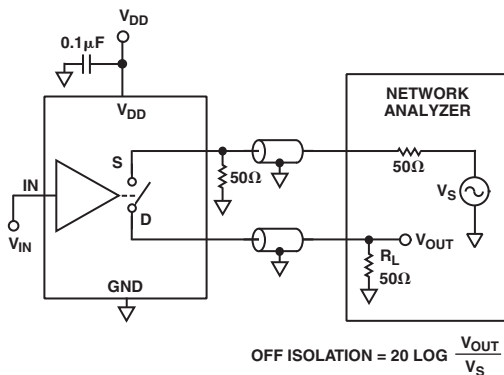
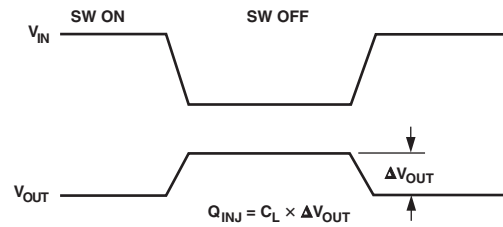
Test Circuit 4. Switching Times



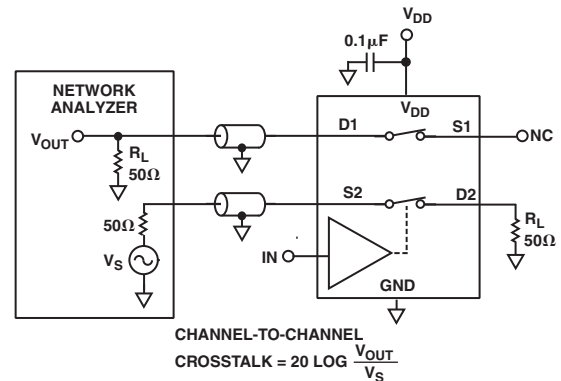
Test Circuit 5. Break-Before-Make Time Delay, t_D



Test Circuit 6. Charge Injection

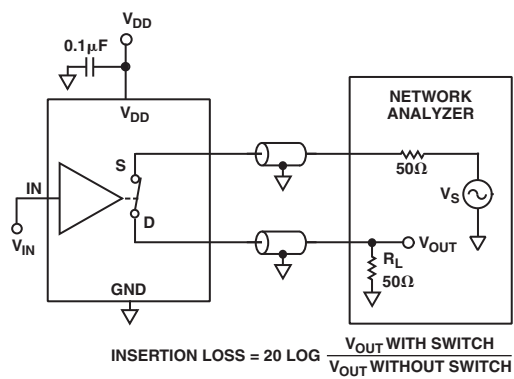


Test Circuit 7. Off Isolation



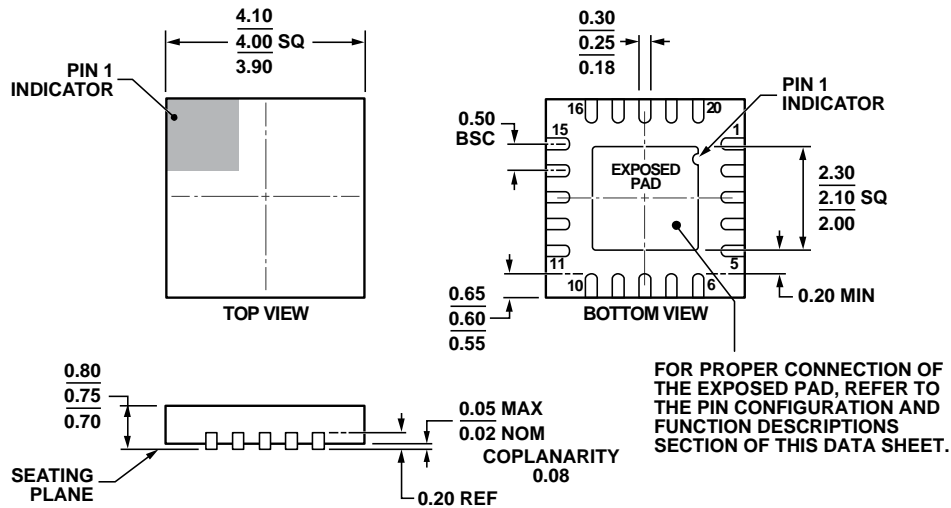
Test Circuit 8. Channel-to-Channel Crosstalk

ADG781/ADG782/ADG783



Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 2. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

08-16-2010-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG781BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG781BCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG782BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG782BCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG783BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG783BCPZ-REEL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG783BCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6

¹ Z = RoHS Compliant Part.

REVISION HISTORY

2/13—Rev. B to Rev. C

Changed Pin 4 from S3 to S44
Changes to Test Circuit 17
Changes to Ordering Guide.....9

8/12—Rev. A to Rev. B

Updated Outline Dimensions.....9
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3/02—Rev. 0 to Rev. A

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