

# ADG431/ADG432/ADG433—SPECIFICATIONS<sup>1</sup>

**Dual Supply** ( $V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = +5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version –40°C to		Unit	Test Conditions/Comments
	+25°C	+85°C		
ANALOG SWITCH				
Analog Signal Range	V <sub>DD</sub> to V <sub>SS</sub>		V	V <sub>D</sub> = ±8.5 V, I <sub>S</sub> = –10 mA; V <sub>DD</sub> = +13.5 V, V <sub>SS</sub> = –13.5 V
R <sub>ON</sub>	17		Ω typ	
	24	26	Ω max	
R <sub>ON</sub> vs. V <sub>D</sub> (V <sub>S</sub> )	15		% typ	
R <sub>ON</sub> Drift	0.5		%/°C typ	
R <sub>ON</sub> Match	5		% typ	V <sub>D</sub> = 0 V, I <sub>S</sub> = –10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.05		nA typ	V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = –16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V; Test Circuit 2
	±0.25	±2	nA max	
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.05		nA typ	V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V; Test Circuit 2
	±0.25	±2	nA max	
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.1		nA typ	V <sub>D</sub> = V <sub>S</sub> = ±15.5 V; Test Circuit 3
	±0.35	±3	nA max	
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.4	V min	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>	0.005		μA typ	
		±0.02	μA max	
C <sub>IN</sub> Digital Input Capacitance	9		pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>				
t <sub>ON</sub>	90		ns typ	V <sub>DD</sub> = +15 V, V <sub>SS</sub> = –15 V R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; V <sub>S</sub> = ±10 V; Test Circuit 4
		165	ns max	
t <sub>OFF</sub>	60		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; V <sub>S</sub> = ±10 V; Test Circuit 4
		130	ns max	
Break-Before-Make Time Delay, t <sub>D</sub> (ADG433 Only)	25		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; V <sub>S1</sub> = V <sub>S2</sub> = +10 V; Test Circuit 5
Charge Injection	5		pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 10 nF; Test Circuit 6
OFF Isolation	68		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Test Circuit 8
C <sub>S</sub> (OFF)	9		pF typ	f = 1 MHz
C <sub>D</sub> (OFF)	9		pF typ	f = 1 MHz
C <sub>D</sub> , C <sub>S</sub> (ON)	35		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I <sub>DD</sub>	0.0001		μA typ	V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = –16.5 V Digital Inputs = 0 V or 5 V
	0.1	0.2	μA max	
I <sub>SS</sub>	0.0001		μA typ	
	0.1	0.2	μA max	
I <sub>L</sub>	0.0001		μA typ	
	0.1	0.2	μA max	
Power Dissipation		7.7	μW max	

## NOTES

<sup>1</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**Single Supply** ( $V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range	0 V to V <sub>DD</sub>		V	0 < V <sub>D</sub> < 8.5 V, I <sub>S</sub> = −10 mA; V <sub>DD</sub> = 10.8 V
R <sub>ON</sub>	28		Ω typ	
	42	45	Ω max	
R <sub>ON</sub> vs. V <sub>D</sub> (V <sub>S</sub> )	20		% typ	
R <sub>ON</sub> Drift	0.5		%/°C typ	V <sub>D</sub> = 0 V, I <sub>S</sub> = −10 mA
R <sub>ON</sub> Match	5		% typ	
LEAKAGE CURRENTS				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.04		nA typ	V <sub>DD</sub> = 13.2 V V <sub>D</sub> = 12.2/1 V, V <sub>S</sub> = 1/12.2 V; Test Circuit 2
	±0.25	±2	nA max	
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.04		nA typ	V <sub>D</sub> = 12.2/1 V, V <sub>S</sub> = 1/12.2 V; Test Circuit 2
	±0.25	±2	nA max	
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.01		nA typ	V <sub>D</sub> = V <sub>S</sub> = 12.2 V/1 V; Test Circuit 3
	±0.3	±3	nA max	
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.4	V min	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>	0.005		μA typ	
		±0.01	μA max	
C <sub>IN</sub> Digital Input Capacitance	9		pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>				
t <sub>ON</sub>	165		ns typ	V <sub>DD</sub> = 12 V, V <sub>SS</sub> = 0 V R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; V <sub>S</sub> = 8 V; Test Circuit 4
		240	ns max	
t <sub>OFF</sub>	60		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; V <sub>S</sub> = 8 V; Test Circuit 4
		115	ns max	
Break-Before-Make Time Delay, t <sub>D</sub> (ADG433 Only)	25		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; V <sub>S1</sub> = V <sub>S2</sub> = 10 V; Test Circuit 5
Charge Injection	25		pC typ	
OFF Isolation	68		dB typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 10 nF; Test Circuit 6
Channel-to-Channel Crosstalk	85		dB typ	
C <sub>S</sub> (OFF)	9		pF typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Test Circuit 7
C <sub>D</sub> (OFF)	9		pF typ	
C <sub>D</sub> , C <sub>S</sub> (ON)	35		pF typ	
POWER REQUIREMENTS				
I <sub>DD</sub>	0.0001		μA typ	V <sub>DD</sub> = 13.2 V Digital Inputs = 0 V or 5 V
	0.03	0.1	μA max	
I <sub>L</sub>	0.0001		μA typ	V <sub>L</sub> = 5.25 V
	0.03	0.1	μA max	
Power Dissipation		1.9	μW max	

## NOTES

<sup>1</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Truth Table (ADG431/ADG432)

ADG431 In	ADG432 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG433)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

# ADG431/ADG432/ADG433

## ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted.)

V <sub>DD</sub> to V <sub>SS</sub>	44 V
V <sub>DD</sub> to GND	–0.3 V to +25 V
V <sub>SS</sub> to GND	+0.3 V to –25 V
V <sub>L</sub> to GND	–0.3 V to V <sub>DD</sub> + 0.3 V
Analog, Digital Inputs <sup>2</sup>	V <sub>SS</sub> – 2 V to V <sub>DD</sub> + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	100 mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C

Plastic Package, Power Dissipation	470 mW
θ <sub>JA</sub> , Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	600 mW
θ <sub>JA</sub> , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

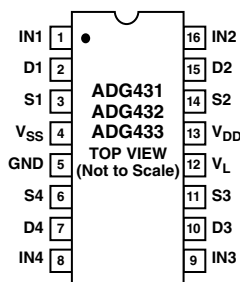
<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG431/ADG432/ADG433 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION (DIP/SOIC)



## ORDERING GUIDE

Model	Temperature Range	Package Option <sup>1</sup>
ADG431BN	–40°C to +85°C	N-16
ADG431BR	–40°C to +85°C	R-16A
ADG431ABR	–40°C to +85°C	R-16A <sup>2</sup>
ADG432BN	–40°C to +85°C	N-16
ADG432BR	–40°C to +85°C	R-16A
ADG432ABR	–40°C to +85°C	R-16A <sup>2</sup>
ADG433BN	–40°C to +85°C	N-16
ADG433BR	–40°C to +85°C	R-16A
ADG433ABR	–40°C to +85°C	R-16A <sup>2</sup>

## NOTES

<sup>1</sup>N = Plastic DIP; R = 0.15" Small Outline IC (SOIC).

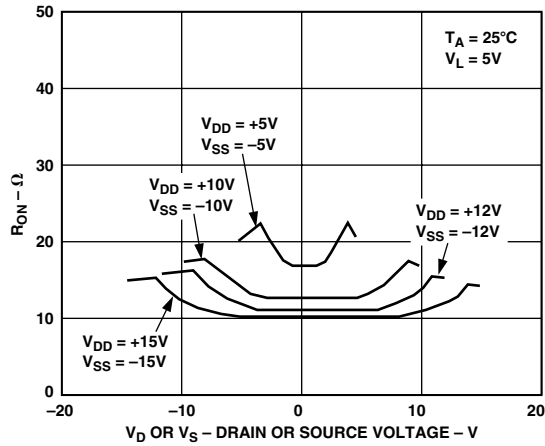
<sup>2</sup>Trench isolated, latch-up proof parts. See Trench Isolation section.

## TERMINOLOGY

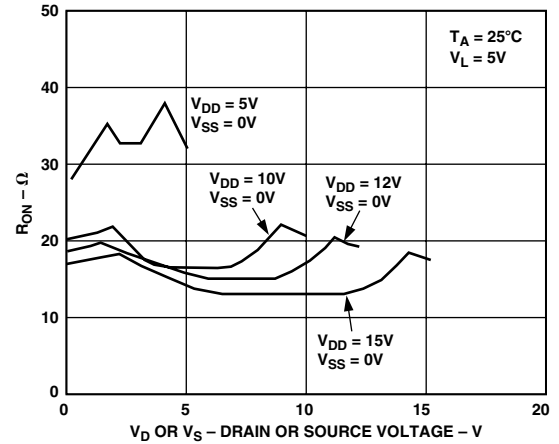
V <sub>DD</sub>	Most positive power supply potential.
V <sub>SS</sub>	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V <sub>L</sub>	Logic power supply (5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R <sub>ON</sub>	Ohmic resistance between D and S.
R <sub>ON</sub> vs. V <sub>D</sub> (V <sub>S</sub> )	The variation in R <sub>ON</sub> due to a change in the analog input voltage with a constant load current.
R <sub>ON</sub> Drift	Change in R <sub>ON</sub> vs. temperature.
R <sub>ON</sub> Match	Difference between the R <sub>ON</sub> of any two switches.
I <sub>S</sub> (OFF)	Source leakage current with the switch "OFF."
I <sub>D</sub> (OFF)	Drain leakage current with the switch "OFF."
I <sub>D</sub> , I <sub>S</sub> (ON)	Channel leakage current with the switch "ON."
V <sub>D</sub> (V <sub>S</sub> )	Analog voltage on terminals D, S.

C <sub>S</sub> (OFF)	"OFF" switch source capacitance.
C <sub>D</sub> (OFF)	"OFF" switch drain capacitance.
C <sub>D</sub> , C <sub>S</sub> (ON)	"ON" switch capacitance.
C <sub>IN</sub>	Input Capacitance to ground of a digital input.
t <sub>ON</sub>	Delay between applying the digital control input and the output switching on.
t <sub>OFF</sub>	Delay between applying the digital control input and the output switching off.
t <sub>D</sub>	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

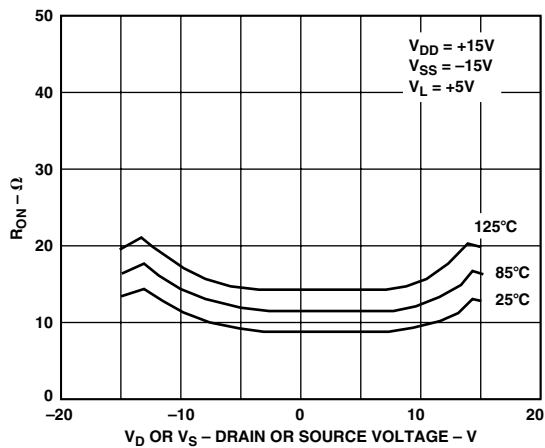
# Typical Performance Characteristics—ADG431/ADG432/ADG433



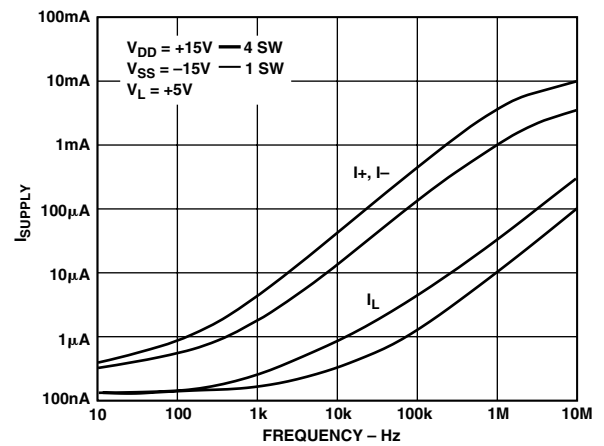
TPC 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) Dual Supplies



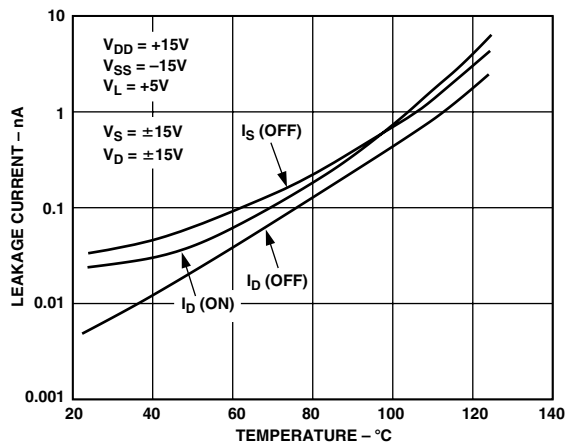
TPC 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supply



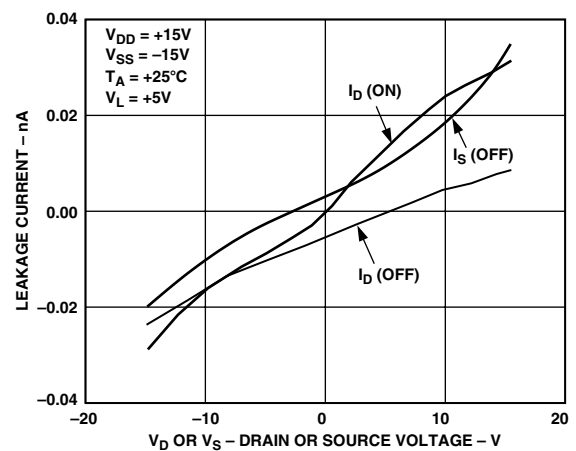
TPC 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures



TPC 5. Supply Current vs. Input Switching Frequency

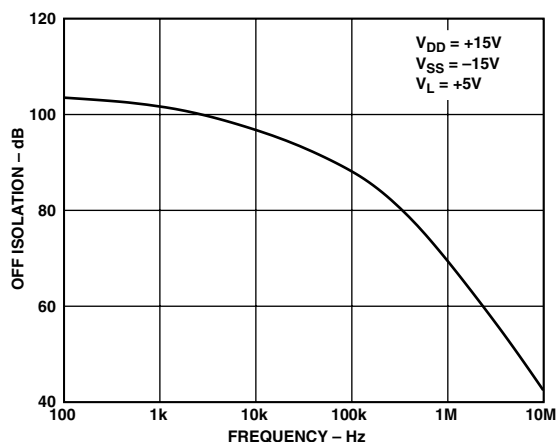


TPC 3. Leakage Currents as a Function of Temperature

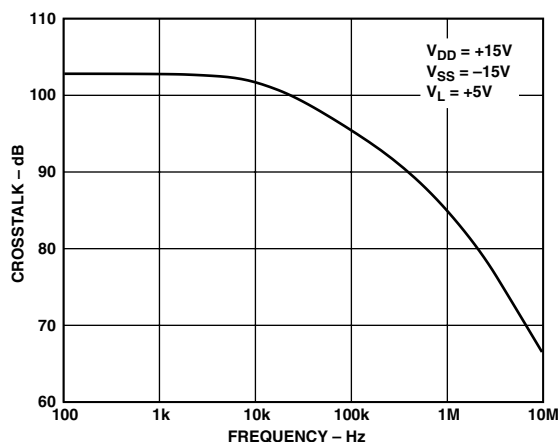


TPC 6. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

# ADG431/ADG432/ADG433



TPC 7. Off Isolation vs. Frequency



TPC 8. Crosstalk vs. Frequency

## TRENCH ISOLATION

In the ADG431A, ADG432A and ADG433A, an insulating oxide layer (trench) is placed between the NMOS and PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors from a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

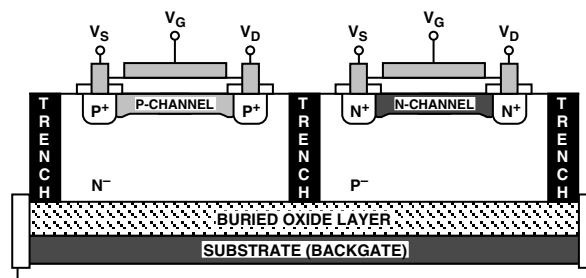


Figure 1. Trench Isolation

## APPLICATION

Figure 2 illustrates a precise, fast sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output  $V_{OUT}$  follows the input signal  $V_{IN}$ . In the hold mode, SW1 is opened and the signal is held by the hold capacitor  $C_H$ .

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG431/ADG432/ADG433 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically  $30 \mu V/\mu s$ .

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network  $R_C$  and  $C_C$ . This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the  $\pm 10 V$  input range. Both the acquisition and settling times are 850 ns.

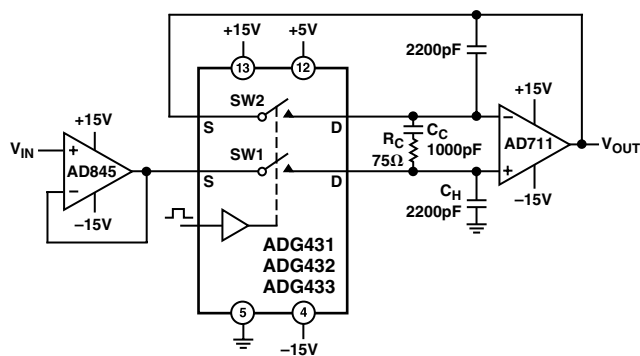
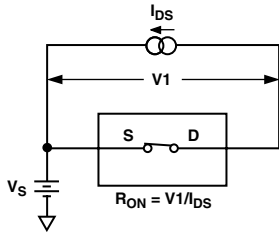
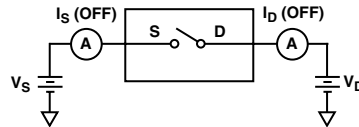


Figure 2. Fast, Accurate Sample-and-Hold

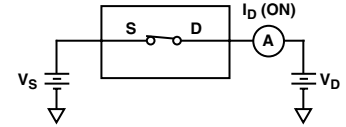
## Test Circuits



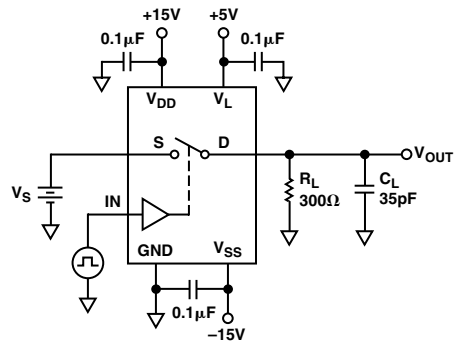
Test Circuit 1. On Resistance



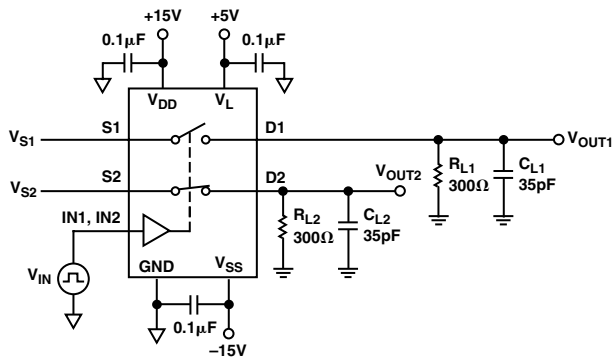
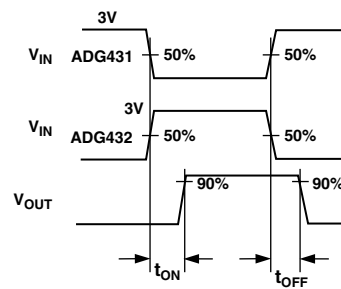
Test Circuit 2. Off Leakage



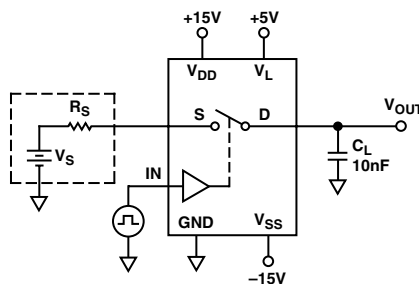
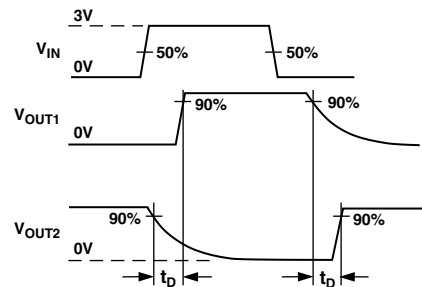
Test Circuit 3. On Leakage



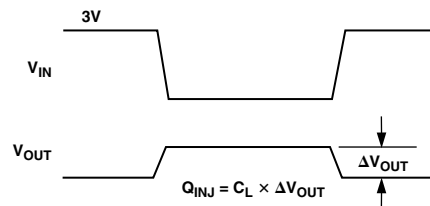
Test Circuit 4. Switching Times



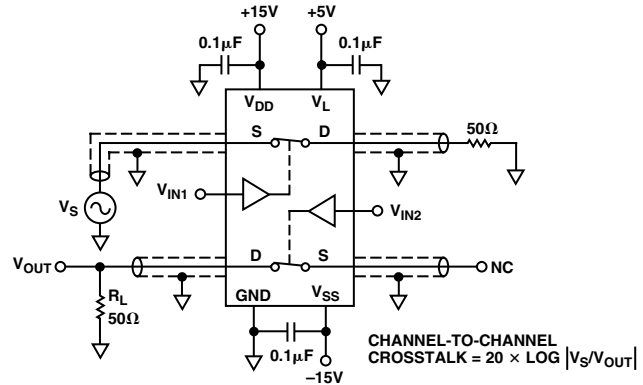
Test Circuit 5. Break-Before-Make Time Delay



Test Circuit 6. Charge Injection



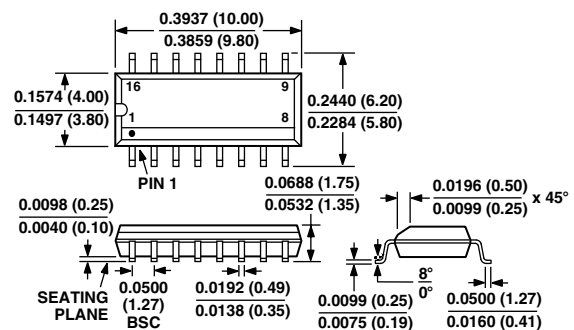
## ADG431/ADG432/ADG433—Revision History



### Test Circuit 8. Channel-to-Channel Crosstalk

Dimensions shown in inches and (mm).

**(N-16)**



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