ADG417* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1313: Configuring the AD5422 to Combine Output Current and Output Voltage to a Single Output Pin

Data Sheet

- ADG417: LC^{2}MOS Precision Mini-DIP Analog Switch Data Sheet

REFERENCE MATERIALS

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

DESIGN RESOURCES

- ADG417 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG417 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

This page is dynamically generated by Analog Devices, Inc., and inserted into this data sheet. A dynamic change to the content on this page will not trigger a change to either the revision number or the content of the product data sheet. This dynamic page may be frequently modified.

ADG417–SPECIFICATIONS

Dual Supply[1] (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/Comments
	+25°C	–40°C to +85°C	+25°C	–55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	25		25		Ω typ	$V_D = \pm 12.5$ V, $I_S = -10$ mA
	35	45	35	45	Ω max	$V_{DD} = +13.5$ V, $V_{SS} = -13.5$ V
LEAKAGE CURRENTS						$V_{DD} = +16.5$ V, $V_{SS} = -16.5$ V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	$V_D = \pm 15.5$ V, $V_S = \mp 15.5$ V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	$V_D = \pm 15.5$ V, $V_S = \mp 15.5$ V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	$V_S = V_D = \pm 15.5$ V;
	±0.4	±5	±0.4	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	µA typ	$V_{IN} = V_{INL}$ or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	100		100		ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF;
	160	200	145	200	ns max	$V_S = \pm 10$ V; Test Circuit 4
t_{OFF}	60		60		ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF;
	100	150	100	150	ns max	$V_S = \pm 10$ V; Test Circuit 4
Charge Injection	7		7		pC typ	$V_S = 0$ V, $R_L = 0\ \Omega$, $C_L = 10$ nF; Test Circuit 5
OFF Isolation	80		80		dB typ	$R_L = 50\ \Omega$, f = 1 MHz; Test Circuit 6
C_S (OFF)	6		6		pF typ	
C_D (OFF)	6		6		pF typ	
C_D, C_S (ON)	55		55		pF typ	
POWER REQUIREMENTS						$V_{DD} = +16.5$ V, $V_{SS} = -16.5$ V
I_{DD}	0.0001		0.0001		µA typ	$V_{IN} = 0$ V or 5 V
	1	2.5	1	2.5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	2.5	1	2.5	µA max	
I_L	0.0001		0.0001		µA typ	$V_L = +5.5$ V
	1	2.5	1	2.5	µA max	

NOTES

[1] Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2] Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply[1] (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = +3 V, +8.5 V, I_S = –10 mA
		60		70	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENT						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_S = V_D = 12.2 V/1 V;
	±0.4	±5	±0.4	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	180	250	180	250	ns max	R_L = 300 Ω, C_L = 35 pF;
						V_S = +8 V; Test Circuit 4
t_{OFF}	85	110	85	110	ns max	R_L = 300 Ω, C_L = 35 pF;
						V_S = +8 V; Test Circuit 4
Charge Injection	11		11		pC typ	V_S = 0 V, R_S = 0 Ω,
						C_L = 10 nF; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz;
						Test Circuit 6
C_S (OFF)	13		13		pF typ	
C_D (OFF)	13		13		pF typ	
C_D, C_S (ON)	65		65		pF typ	
POWER REQUIREMENTS						V_{DD} = +13.2 V
I_{DD}	0.0001		0.0001		µA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	µA max	
I_L	0.0001		0.0001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES

[1] Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

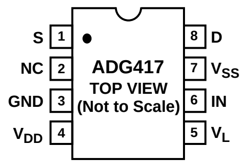
[2] Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Table I. Truth Table

Logic	Switch Condition
0	ON
1	OFF

PIN CONFIGURATION DIP/SOIC



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Options*
ADG417BN	–40°C to +85°C	N-8
ADG417BR	–40°C to +85°C	SO-8

*N = Plastic DIP, SO = 0.15" Small Outline IC (SOIC).

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	+44 V
V_{DD} to GND	–0.3 V to +25 V
V_{SS} to GND	+0.3 V to –25 V
V_L to GND	–0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2]	V_{SS} – 2 V to V_{DD} +2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)	
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Extended (T Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Plastic Package, Power Dissipation	400 mW
θ_{JA}, Thermal Impedance	100°C/W
Lead Temperature, Soldering (10 sec)	+260°C
SOIC Package, Power Dissipation	400 mW
θ_{JA}, Thermal Impedance	155°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec).	+215°C
Infrared (15 sec)	+220°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG417 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or an output.
D	Drain terminal. May be an input or an output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.
I_L	Logic supply current.

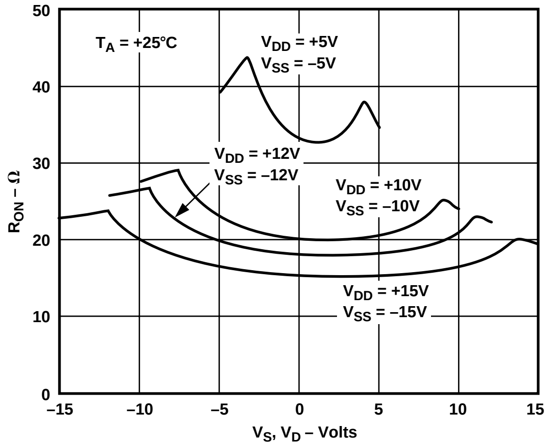


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

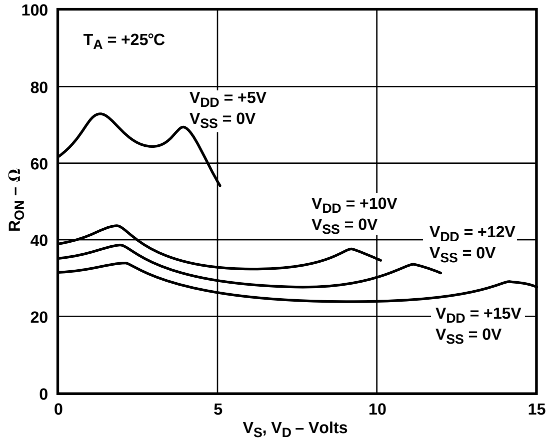


Figure 4. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

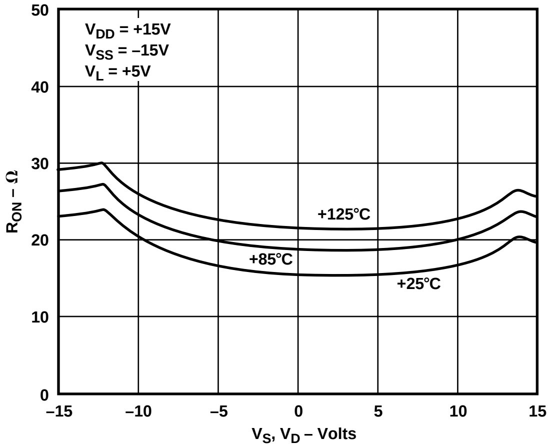


Figure 2. R_{ON} as a Function of V_D (V_S) for Different Temperatures

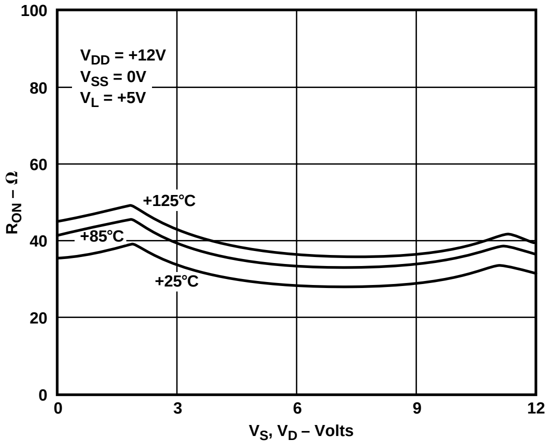


Figure 5. R_{ON} as a Function of V_D (V_S) for Different Temperatures

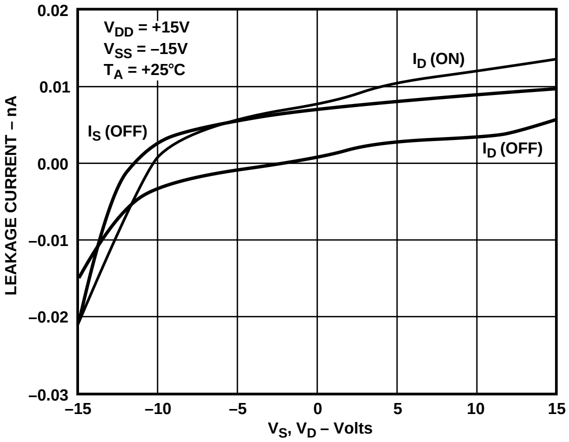


Figure 3. Leakage Currents as a Function of V_S (V_D)

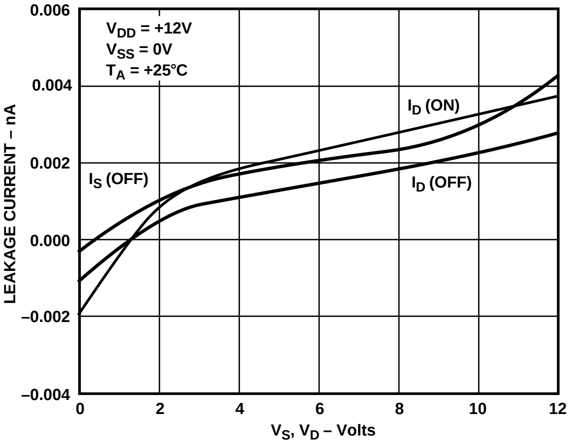


Figure 6. Leakage Currents as a Function of V_S (V_D)

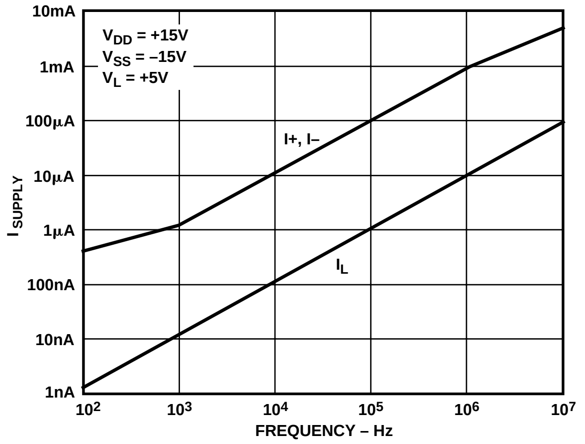


Figure 7. Supply Current vs. Input Switching Frequency

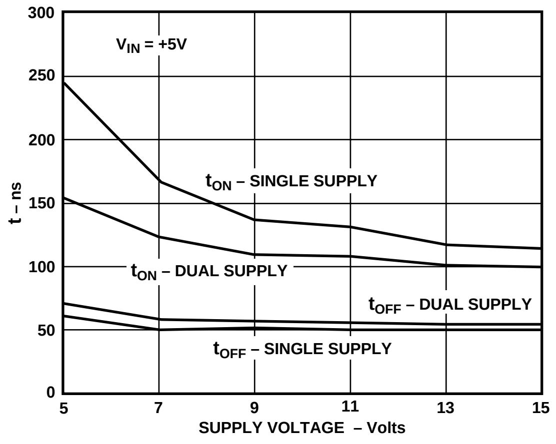
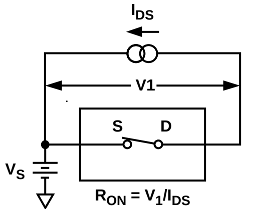
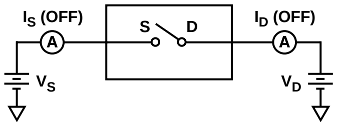


Figure 8. Switching Time vs. Power Supply

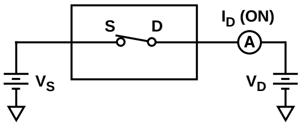
Test Circuits



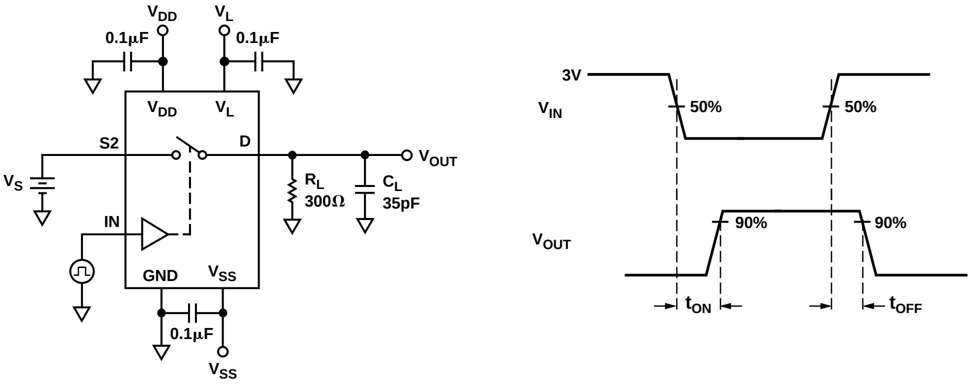
Test Circuit 1. On Resistance



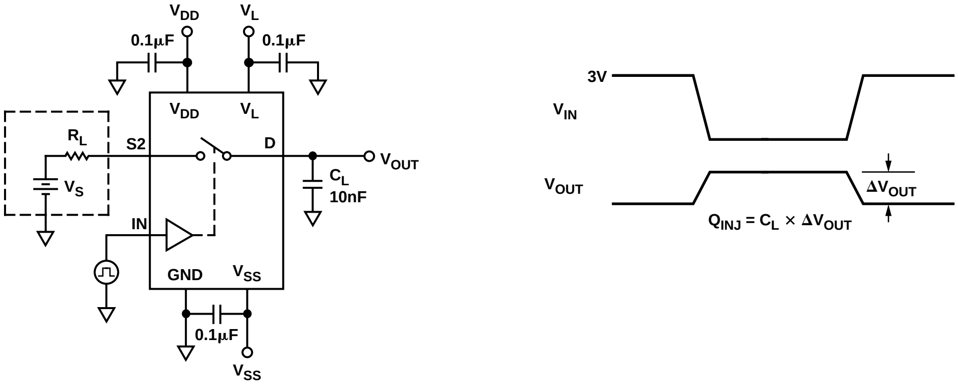
Test Circuit 2. Off Leakage



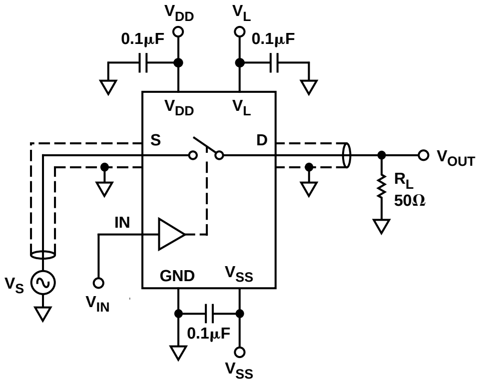
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times



Test Circuit 5. Charge Injection

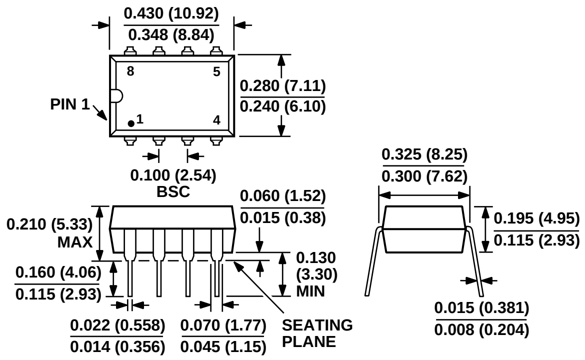


Test Circuit 6. Off Isolation

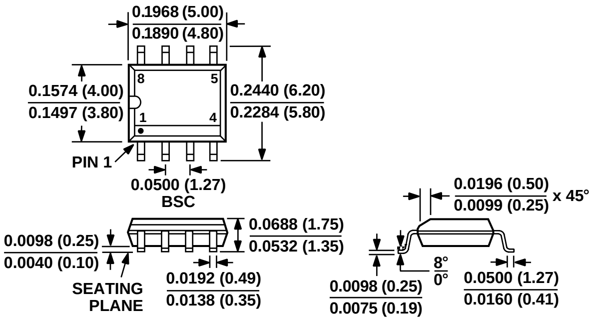
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead SOIC (SO-8)
(Narrow Body)



C1974a–0–9/98

PRINTED IN U.S.A.