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## REVISION HISTORY

### 03/08—Rev. D to Rev. E

|                                                              |           |
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| Updated Format.....                                          | Universal |
| Changes to Features.....                                     | 1         |
| Changes to General Description .....                         | 1         |
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### 11/04—Rev. C to Rev. D

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### 04/03—Rev. A to Rev. B

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### 06/02—Rev. 0 to Rev. A

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## SPECIFICATIONS

$V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $GND = 0 \text{ V}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

| Parameter <sup>1</sup>                                | Symbol                                           | Conditions <sup>2</sup>                                                       | B Version |                  |       | Unit |
|-------------------------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------|-----------|------------------|-------|------|
|                                                       |                                                  |                                                                               | Min       | Typ <sup>3</sup> | Max   |      |
| DC ELECTRICAL CHARACTERISTICS                         |                                                  |                                                                               |           |                  |       |      |
| Input High Voltage                                    | V <sub>INH</sub>                                 |                                                                               | 2.4       |                  |       | V    |
| Input Low Voltage                                     | V <sub>INL</sub>                                 |                                                                               | −0.3      |                  | +0.8  | V    |
| Input Leakage Current                                 | I <sub>I</sub>                                   | 0 ≤ V <sub>IN</sub> ≤ 5.5 V                                                   |           | ±0.01            | ±1    | μA   |
| Off State Leakage Current                             | I <sub>OZ</sub>                                  | 0 ≤ A, B ≤ V <sub>CC</sub>                                                    |           | ±0.01            | ±1    | μA   |
| On State Leakage Current                              | I <sub>OZ</sub>                                  | 0 ≤ A, B ≤ V <sub>CC</sub>                                                    |           | ±0.01            | ±1    | μA   |
| Maximum Pass Voltage <sup>4</sup>                     | V <sub>P</sub>                                   | V <sub>IN</sub> = V <sub>CC</sub> = 5 V, I <sub>O</sub> = −5 μA               | 3.9       | 4.2              | 4.4   | V    |
| CAPACITANCE <sup>4</sup>                              |                                                  |                                                                               |           |                  |       |      |
| A Port Off Capacitance                                | C <sub>A</sub> OFF                               | f = 1 MHz                                                                     |           | 7                |       | pF   |
| B Port Off Capacitance                                | C <sub>B</sub> OFF                               | f = 1 MHz                                                                     |           | 5                |       | pF   |
| A, B Port On Capacitance                              | C <sub>A</sub> , C <sub>B</sub> ON               | f = 1 MHz                                                                     |           | 11               |       | pF   |
| Control Input Capacitance                             | C <sub>IN</sub>                                  | f = 1 MHz                                                                     |           | 4                |       | pF   |
| SWITCHING CHARACTERISTICS <sup>4</sup>                |                                                  |                                                                               |           |                  |       |      |
| Propagation Delay A to B or B to A, t <sub>PD</sub>   | t <sub>PHL</sub> , t <sub>PLH</sub> <sup>5</sup> | V <sub>A</sub> = 0 V, C <sub>L</sub> = 50 pF                                  |           |                  | 0.10  | ns   |
| Propagation Delay Matching <sup>6</sup>               |                                                  | V <sub>A</sub> = 0 V, C <sub>L</sub> = 50 pF                                  |           | 0.0075           | 0.035 | ns   |
| Bus Enable Time $\overline{BE}$ to A or B             | t <sub>PZH</sub> , t <sub>PZL</sub>              | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                | 1         | 5                | 7.5   | ns   |
| Bus Disable Time $\overline{BE}$ to A or B            | t <sub>PHZ</sub> , t <sub>PLZ</sub>              | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                | 1         | 3.5              | 7     | ns   |
| Bus Select Time S to A or B                           |                                                  |                                                                               |           |                  |       |      |
| Enable                                                | t <sub>SEL_EN</sub>                              | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                |           | 8                | 12    | ns   |
| Disable                                               | t <sub>SEL_DIS</sub>                             | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                |           | 5                | 8     | ns   |
| Maximum Data Rate                                     |                                                  | V <sub>A</sub> = 2 V p-p                                                      |           | 933              |       | Mbps |
| DIGITAL SWITCH                                        |                                                  |                                                                               |           |                  |       |      |
| On Resistance                                         | R <sub>ON</sub>                                  | V <sub>A</sub> = 0 V                                                          |           |                  |       |      |
|                                                       |                                                  | I <sub>O</sub> = 48 mA, 15 mA, 8 mA, T <sub>A</sub> = 25°C                    |           | 2                | 4     | Ω    |
|                                                       |                                                  | I <sub>O</sub> = 48 mA, 15 mA, 8 mA                                           |           |                  | 5     | Ω    |
|                                                       |                                                  | V <sub>A</sub> = 2.4 V                                                        |           |                  |       |      |
|                                                       |                                                  | I <sub>O</sub> = 48 mA, 15 mA, 8 mA, T <sub>A</sub> = 25°C                    |           | 3                | 6     | Ω    |
|                                                       |                                                  | I <sub>O</sub> = 48 mA, 15 mA, 8 mA                                           |           |                  | 7     | Ω    |
| On-Resistance Matching                                | ΔR <sub>ON</sub>                                 | V <sub>A</sub> = 0 V, I <sub>O</sub> = 48 mA, 15 mA, 8 mA                     |           | 0.15             |       | Ω    |
| POWER REQUIREMENTS                                    |                                                  |                                                                               |           |                  |       |      |
| V <sub>CC</sub>                                       |                                                  |                                                                               | 3.0       |                  | 5.5   | V    |
| Quiescent Power Supply Current                        | I <sub>CC</sub>                                  | Digital inputs = 0 V or V <sub>CC</sub>                                       |           | 0.001            | 1     | μA   |
| Increase in I <sub>CC</sub> per Input <sup>4, 7</sup> | ΔI <sub>CC</sub>                                 | V <sub>CC</sub> = 5.5 V, one input at 3.0 V; others at V <sub>CC</sub> or GND |           |                  | 200   | μA   |

<sup>1</sup> Temperature range is: Version B:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> See Test Circuits section.

<sup>3</sup> All typical values are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

<sup>4</sup> Guaranteed by design, not subject to production test.

<sup>5</sup> The digital switch contributes no propagation delay other than the RC delay of the typical  $R_{ON}$  of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

<sup>6</sup> Propagation delay matching between channels is calculated from on-resistance matching of worst-case channel combinations and load capacitance.

<sup>7</sup> This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition.

# ADG3257

$V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $GND = 0 \text{ V}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

**Table 3.**

| Parameter <sup>1</sup>                                | Symbol                                           | Conditions <sup>2</sup>                                                       | B Version |                  |      | Unit |
|-------------------------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------|-----------|------------------|------|------|
|                                                       |                                                  |                                                                               | Min       | Typ <sup>3</sup> | Max  |      |
| DC ELECTRICAL CHARACTERISTICS                         |                                                  |                                                                               |           |                  |      |      |
| Input High Voltage                                    | V <sub>INH</sub>                                 |                                                                               | 2.0       |                  |      | V    |
| Input Low Voltage                                     | V <sub>INL</sub>                                 |                                                                               | −0.3      |                  | +0.8 | V    |
| Input Leakage Current                                 | I <sub>I</sub>                                   | 0 ≤ V <sub>IN</sub> ≤ 3.6 V                                                   |           | ±0.01            | ±1   | μA   |
| Off State Leakage Current                             | I <sub>OZ</sub>                                  | 0 ≤ A, B ≤ V <sub>CC</sub>                                                    |           | ±0.01            | ±1   | μA   |
| On State Leakage Current                              | I <sub>OZ</sub>                                  | 0 ≤ A, B ≤ V <sub>CC</sub>                                                    |           | ±0.01            | ±1   | μA   |
| Maximum Pass Voltage <sup>4</sup>                     | V <sub>P</sub>                                   | V <sub>IN</sub> = V <sub>CC</sub> = 3.3 V, I <sub>O</sub> = −5 μA             | 2.3       | 2.6              | 2.8  | V    |
| CAPACITANCE <sup>4</sup>                              |                                                  |                                                                               |           |                  |      |      |
| A Port Off Capacitance                                | C <sub>A</sub> OFF                               | f = 1 MHz                                                                     |           | 7                |      | pF   |
| B Port Off Capacitance                                | C <sub>B</sub> OFF                               | f = 1 MHz                                                                     |           | 5                |      | pF   |
| A, B Port On Capacitance                              | C <sub>A</sub> , C <sub>B</sub> ON               | f = 1 MHz                                                                     |           | 11               |      | pF   |
| Control Input Capacitance                             | C <sub>IN</sub>                                  | f = 1 MHz                                                                     |           | 4                |      | pF   |
| SWITCHING CHARACTERISTICS <sup>4</sup>                |                                                  |                                                                               |           |                  |      |      |
| Propagation Delay A to B or B to A, t <sub>PD</sub>   | t <sub>PHL</sub> , t <sub>PLH</sub> <sup>5</sup> | V <sub>A</sub> = 0 V, C <sub>L</sub> = 50 pF                                  |           |                  | 0.10 | ns   |
| Propagation Delay Matching <sup>6</sup>               |                                                  | V <sub>A</sub> = 0 V, C <sub>L</sub> = 50 pF                                  |           | 0.01             | 0.04 | ns   |
| Bus Enable Time $\overline{BE}$ to A or B             | t <sub>PZH</sub> , t <sub>PZL</sub>              | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                | 1         | 5.5              | 9    | ns   |
| Bus Disable Time $\overline{BE}$ to A or B            | t <sub>PHZ</sub> , t <sub>PLZ</sub>              | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                | 1         | 4.5              | 8.5  | ns   |
| Bus Select Time S to A or B                           |                                                  |                                                                               |           |                  |      |      |
| Enable                                                | t <sub>SEL_EN</sub>                              | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                |           | 8                | 12   | ns   |
| Disable                                               | t <sub>SEL_DIS</sub>                             | C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω                                |           | 6                | 9    | ns   |
| Maximum Data Rate                                     |                                                  | V <sub>A</sub> = 2 V p-p                                                      |           | 933              |      | Mbps |
| DIGITAL SWITCH                                        |                                                  |                                                                               |           |                  |      |      |
| On Resistance                                         | R <sub>ON</sub>                                  | V <sub>A</sub> = 0 V, I <sub>O</sub> = 15 mA, 8 mA, T <sub>A</sub> = 25°C     | 2         |                  | 4    | Ω    |
|                                                       |                                                  | V <sub>A</sub> = 0 V, I <sub>O</sub> = 15 mA, 8 mA                            |           |                  | 5    | Ω    |
|                                                       |                                                  | V <sub>A</sub> = 1 V, I <sub>O</sub> = 15 mA, 8 mA, T <sub>A</sub> = 25°C     | 4         |                  | 7    | Ω    |
|                                                       |                                                  | V <sub>A</sub> = 1 V, I <sub>O</sub> = 15 mA, 8 mA                            |           |                  | 8    | Ω    |
| On-Resistance Matching                                | ΔR <sub>ON</sub>                                 | V <sub>A</sub> = 0 V, I <sub>O</sub> = 15 mA, 8 mA                            |           | 0.2              |      | Ω    |
| POWER REQUIREMENTS                                    |                                                  |                                                                               |           |                  |      |      |
| V <sub>CC</sub>                                       |                                                  |                                                                               | 3.0       |                  | 5.5  | V    |
| Quiescent Power Supply Current                        | I <sub>CC</sub>                                  | Digital inputs = 0 V or V <sub>CC</sub>                                       |           | 0.001            | 1    | μA   |
| Increase in I <sub>CC</sub> per Input <sup>4, 7</sup> | ΔI <sub>CC</sub>                                 | V <sub>CC</sub> = 3.3 V, one input at 3.0 V; others at V <sub>CC</sub> or GND |           |                  | 200  | μA   |

<sup>1</sup> Temperature range is: Version B:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> See Test Circuits section.

<sup>3</sup> All typical values are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

<sup>4</sup> Guaranteed by design, not subject to production test.

<sup>5</sup> The digital switch contributes no propagation delay other than the RC delay of the typical  $R_{ON}$  of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

<sup>6</sup> Propagation delay matching between channels is calculated from on-resistance matching of worst-case channel combinations and load capacitance.

<sup>7</sup> This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

| Parameter                             | Rating           |
|---------------------------------------|------------------|
| $V_{CC}$ to GND                       | −0.3 V to +6 V   |
| Digital Inputs to GND                 | −0.3 V to +6 V   |
| DC Input Voltage                      | −0.3 V to +6 V   |
| DC Output Current                     | 100 mA           |
| Operating Temperature Range           |                  |
| Industrial (B Version)                | −40°C to +85°C   |
| Storage Temperature Range             | −65°C to +150°C  |
| Junction Temperature                  | 150°C            |
| QSOP Package                          |                  |
| $\theta_{JA}$ Thermal Impedance       | 149.97°C/W       |
| Lead Soldering                        |                  |
| Lead Temperature, Soldering (10 sec)  | 300°C            |
| IR Reflow, Peak Temperature (<20 sec) | 220°C            |
| Soldering (Pb-Free)                   |                  |
| Reflow, Peak Temperature              | 260(+0/−5)°C     |
| Time at Peak Temperature              | 20 sec to 40 sec |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG3257

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

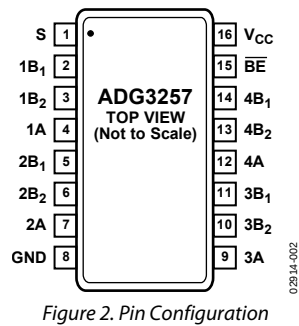


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No.                    | Mnemonic                                                                                                                                      | Description                 |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| 1                          | S                                                                                                                                             | Port Select.                |
| 2, 3, 5, 6, 10, 11, 13, 14 | 1B <sub>1</sub> , 1B <sub>2</sub> , 2B <sub>1</sub> , 2B <sub>2</sub> , 3B <sub>2</sub> , 3B <sub>1</sub> , 4B <sub>2</sub> , 4B <sub>1</sub> | Port B, Inputs or Outputs.  |
| 4, 7, 9, 12                | 1A, 2A, 3A, 4A                                                                                                                                | Port A, Inputs or Outputs.  |
| 8                          | GND                                                                                                                                           | Negative Power Supply.      |
| 15                         | $\overline{BE}$                                                                                                                               | Output Enable (Active Low). |
| 16                         | V <sub>CC</sub>                                                                                                                               | Positive Power Supply.      |

## TYPICAL PERFORMANCE CHARACTERISTICS

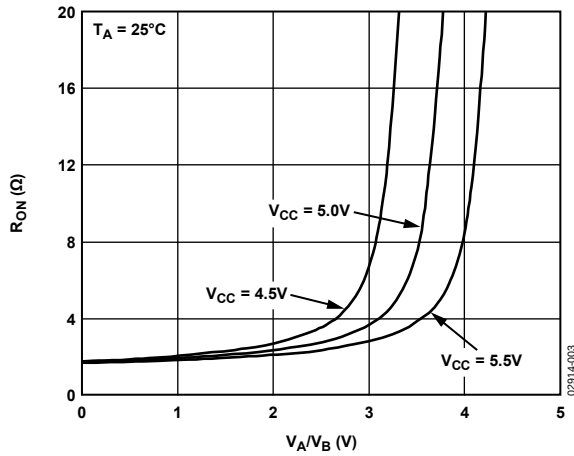


Figure 3. On Resistance vs. Input Voltage

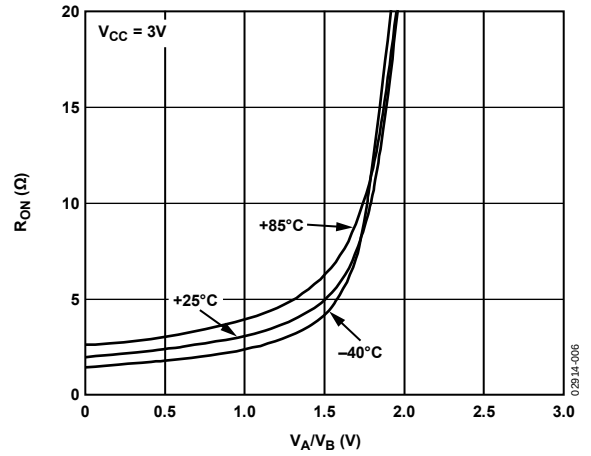


Figure 6. On Resistance vs. Input Voltage for Different Temperatures

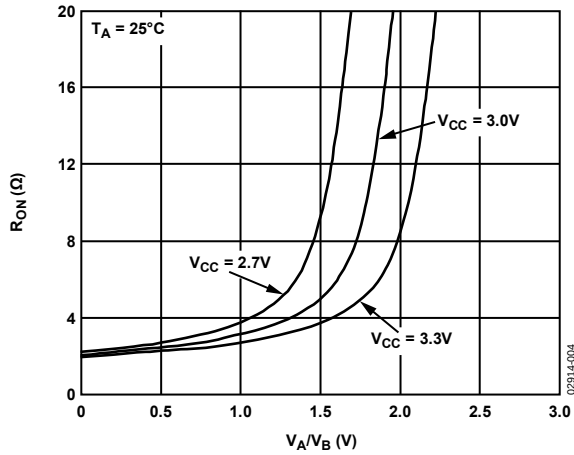


Figure 4. On Resistance vs. Input Voltage

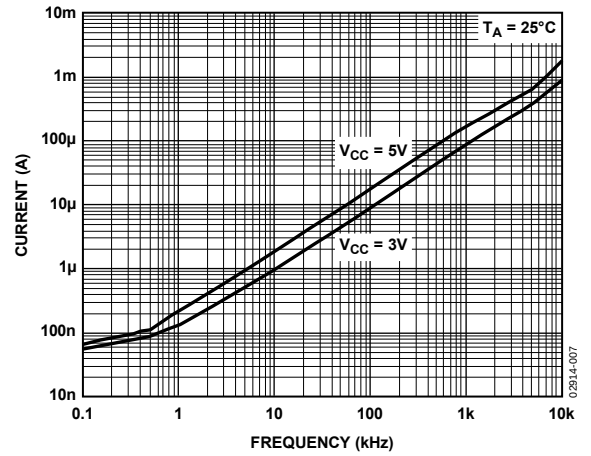


Figure 7.  $I_{CC}$  vs. Enable Frequency

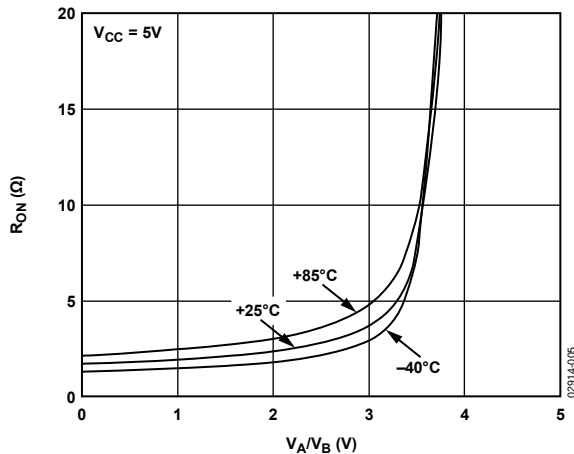


Figure 5. On Resistance vs. Input Voltage for Different Temperatures

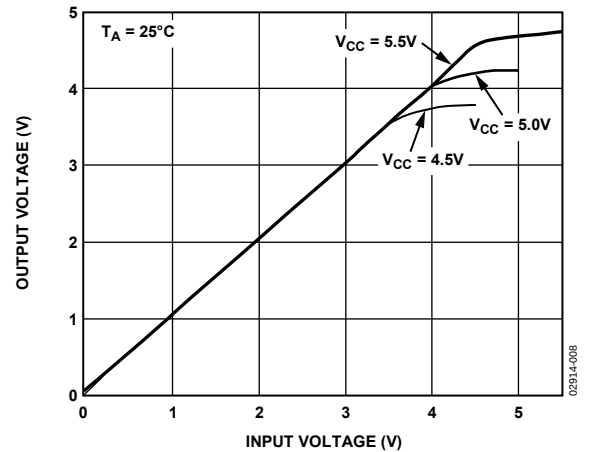


Figure 8. Maximum Pass Voltage

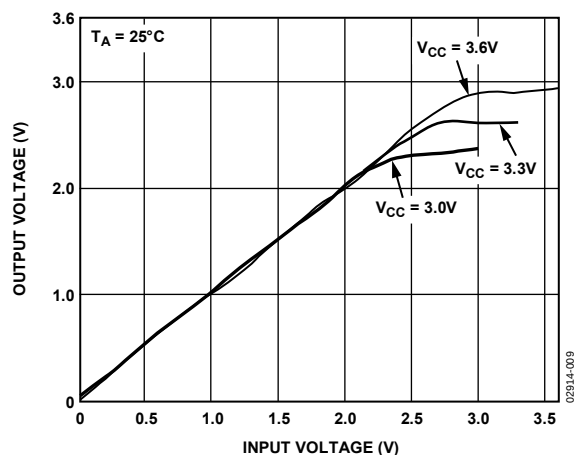


Figure 9. Maximum Pass Voltage

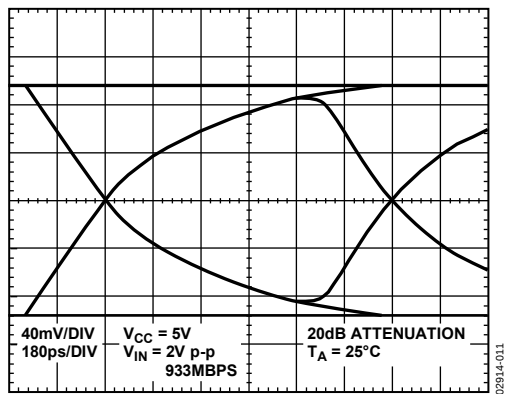


Figure 11. 933 Mbps Eye Diagram

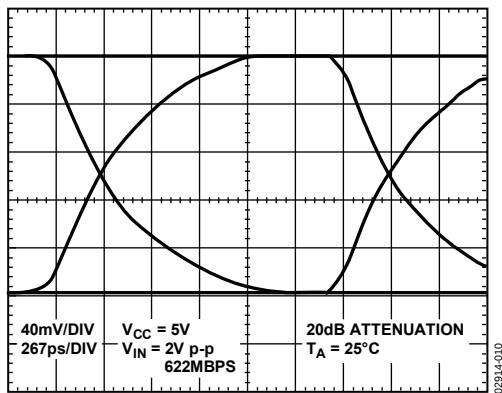
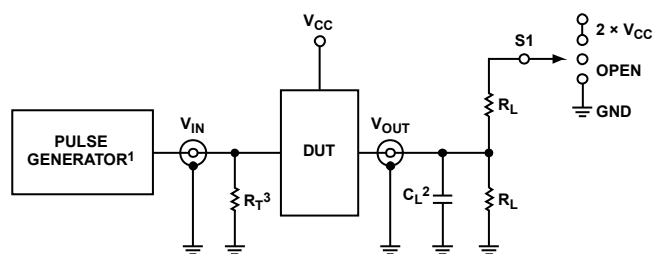


Figure 10. 622 Mbps Eye Diagram

# TEST CIRCUITS



<sup>1</sup>PULSE GENERATOR FOR ALL PULSES:  $t_F < 2.5\text{ns}$ ,  $t_R < 2.5\text{ns}$ .  
<sup>2</sup> $C_L$  = INCLUDES BOARD, STRAY, AND LOAD CAPACITANCES.  
<sup>3</sup> $R_T$  IS THE TERMINATION RESISTOR; SHOULD BE EQUAL TO  $Z_{OUT}$  OF THE PULSE GENERATOR.

Figure 12. Load Circuit

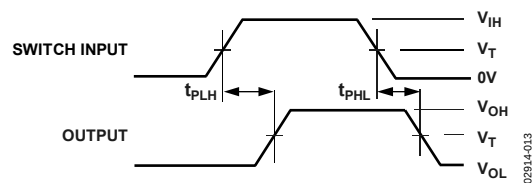


Figure 13. Propagation Delay

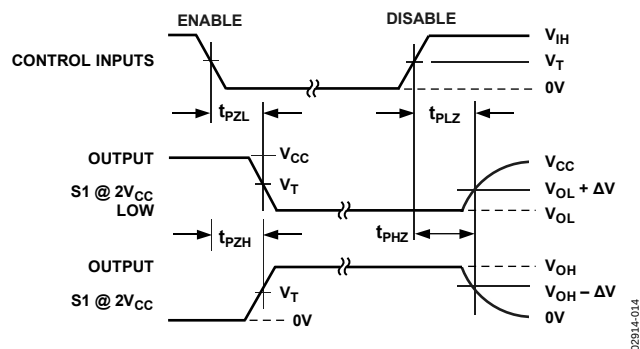


Figure 14. Select, Enable, and Disable Times

Table 6. Switch S1 Condition

| Test                  | S1                |
|-----------------------|-------------------|
| $t_{PLH}$ , $t_{PHL}$ | Open              |
| $t_{PLZ}$ , $t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}$ , $t_{PZH}$ | GND               |
| $t_{SEL}$             | Open              |

Table 7. Test Conditions

| Symbol     | $V_{CC} = 5\text{V} \pm 10\%$ | $V_{CC} = 3.3\text{V} \pm 10\%$ | Unit     |
|------------|-------------------------------|---------------------------------|----------|
| $R_L$      | 500                           | 500                             | $\Omega$ |
| $\Delta V$ | 300                           | 300                             | mV       |
| $C_L$      | 50                            | 50                              | pF       |

## APPLICATIONS INFORMATION

### MIXED VOLTAGE OPERATION, LEVEL TRANSLATION

Bus switches can be used to provide a solution for mixed voltage systems where interfacing bidirectionally between 5 V and 3.3 V devices is required. To interface between 5 V and 3.3 V buses, an external diode is placed in series with the 5 V power supply as shown in Figure 15.

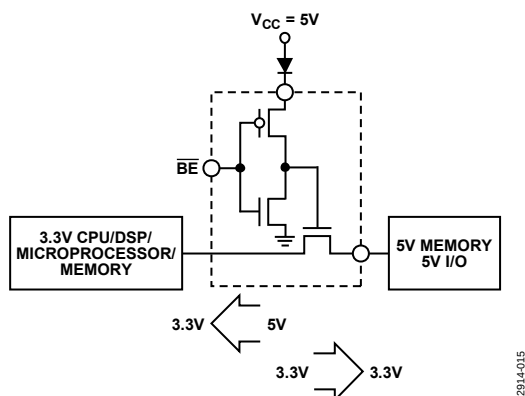


Figure 15. Level Translation Between 5 V and 3.3 V Devices

The diode drops the internal gate voltage down to 4.3 V. The bus switch limits the voltage present on the output to

$$V_{CC} - \text{External Diode Drop} = V_{TH}$$

Therefore, assuming a diode drop of 0.7 V and a  $V_{TH}$  of 1 V, the output voltage is limited to 3.3 V with a logic high.

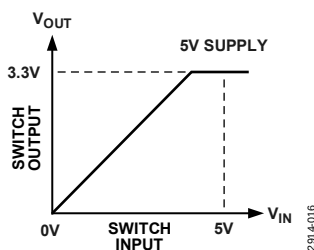


Figure 16. Input Voltage to Output Voltage

Similarly, the device could be used to translate bidirectionally between 3.3 V to 2.5 V systems. In this case, there is no need for an external diode. The internal  $V_{TH}$  drop is 1 V, so with a  $V_{CC} = 3.3$  V the bus switch limits the output voltage to

$$V_{CC} - 1 \text{ V} = 2.3 \text{ V}$$

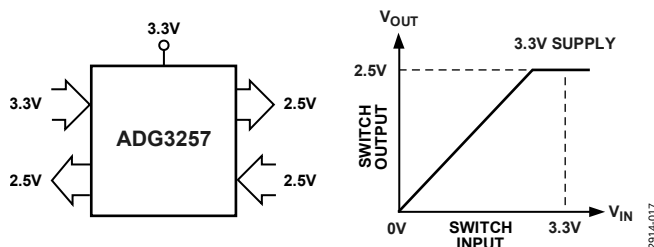


Figure 17. 3.3 V to 2.5 V Level Translation Using the ADG3257 Bus Switch

### MEMORY SWITCHING

This quad bus switch may be used to allow switching between different memory banks, thus allowing additional memory and decreasing capacitive loading. Figure 18 illustrates the ADG3257 in such an application.

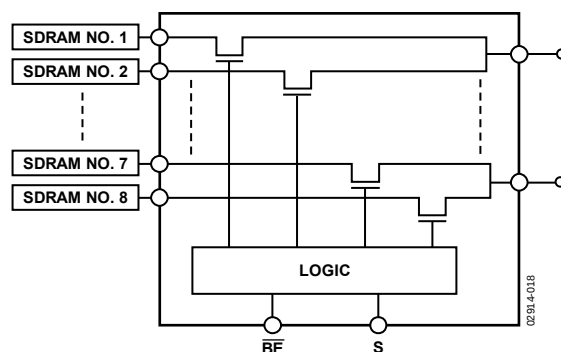
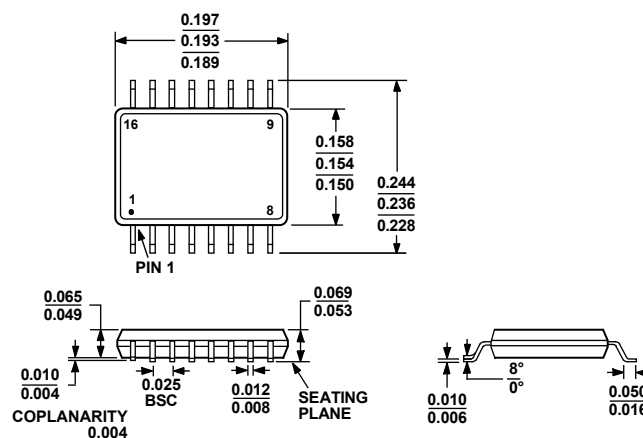


Figure 18. Allows Additional Memory Modules Without Added Drive or Delay

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

Figure 19. 16-Lead Shrink Small Outline Package [QSOP]  
(RQ-16)

Dimensions shown in inches

## ORDERING GUIDE

| Model                          | Temperature Range | Package Description                         | Package Option |
|--------------------------------|-------------------|---------------------------------------------|----------------|
| ADG3257BRQ                     | −40°C to +85°C    | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16          |
| ADG3257BRQ-REEL                | −40°C to +85°C    | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16          |
| ADG3257BRQ-REEL7               | −40°C to +85°C    | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16          |
| ADG3257BRQZ <sup>1</sup>       | −40°C to +85°C    | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16          |
| ADG3257BRQZ-REEL <sup>1</sup>  | −40°C to +85°C    | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16          |
| ADG3257BRQZ-REEL7 <sup>1</sup> | −40°C to +85°C    | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16          |

<sup>1</sup> Z = RoHS Compliant Part.

**ADG3257**

## NOTES