

# ADG3248\* Product Page Quick Links

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## Documentation

### Data Sheet

- ADG3248: 2.5 V/3.3 V, 2:1 Multiplexer/ Demultiplexer Bus Switch Data Sheet

## Reference Materials

### Product Selection Guide

- Switches and Multiplexers Product Selection Guide

### Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection

## Design Resources

- ADG3248 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

|                                 |           |
|---------------------------------|-----------|
| 10/07—Rev. 0 to Rev. A          |           |
| Updated Format.....             | Universal |
| Changes to Table 1.....         | 1         |
| Changes to Table 3,.....        | 4         |
| Changes to Ordering Guide ..... | 12        |

10/03—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 2.3 \text{ V}$  to  $3.6 \text{ V}$ ,  $GND = 0 \text{ V}$ , all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

Table 2.

| Parameter  | Symbol                              | Conditions   | B Version |                  |       | Unit   |
|--|-------------------------------------|--|-----------|------------------|-------|--------|
|  |                                     |  | Min       | Typ <sup>2</sup> | Max   |        |
| DC ELECTRICAL CHARACTERISTICS                                    |                                     |  |           |                  |       |        |
| Input High Voltage   | V <sub>INH</sub>                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2.0       |                  |       | V      |
|  | V <sub>INH</sub>                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7       |                  |       | V      |
| Input Low Voltage  | V <sub>INL</sub>                    | V <sub>CC</sub> = 2.7 V to 3.6 V   |           |                  | 0.8   | V      |
|  | V <sub>INL</sub>                    | V <sub>CC</sub> = 2.3 V to 2.7 V   |           |                  | 0.7   | V      |
| Input Leakage Current  | I <sub>I</sub>                      |  |           | ±0.01            | ±1    | μA     |
| Off State Leakage Current  | I <sub>OZ</sub>                     | 0 ≤ A, B ≤ V <sub>CC</sub>   |           | ±0.01            | ±1    | μA     |
| On State Leakage Current   | I <sub>OL</sub>                     | 0 ≤ A, B ≤ V <sub>CC</sub>   |           | ±0.01            | ±1    | μA     |
| Maximum Pass Voltage   | V <sub>P</sub>                      | V <sub>A</sub> /V <sub>B</sub> = V <sub>CC</sub> = 3.3 V, I <sub>O</sub> = −5 μA | 2.0       | 2.5              | 2.9   | V      |
|  |                                     | V <sub>A</sub> /V <sub>B</sub> = V <sub>CC</sub> = 2.5 V, I <sub>O</sub> = −5 μA | 1.5       | 1.8              | 2.1   | V      |
| CAPACITANCE <sup>3</sup>   |                                     |  |           |                  |       |        |
| A Port Off Capacitance   | C <sub>A</sub> Off                  | f = 1 MHz  |           | 3.5              |       | pF     |
| B Port Off Capacitance   | C <sub>B</sub> Off                  | f = 1 MHz  |           | 4.5              |       | pF     |
| A, B Port On Capacitance   | C <sub>A</sub> , C <sub>B</sub> On  | f = 1 MHz  |           | 8.5              |       | pF     |
| Control Input Capacitance  | C <sub>IN</sub>                     | f = 1 MHz  |           | 4                |       | pF     |
| SWITCHING CHARACTERISTICS <sup>3</sup>                           |                                     |  |           |                  |       |        |
| Propagation Delay A to B or B to A, t <sub>PD</sub> <sup>4</sup> | t <sub>PHL</sub> , t <sub>PLH</sub> | C <sub>L</sub> = 50 pF, V <sub>CC</sub> = 3 V                                    |           |                  | 0.225 | ns     |
| Propagation Delay Matching <sup>5</sup>                          |                                     |  |           |                  | 5     | ps     |
| Transition Time  | t <sub>TRANS</sub>                  | R <sub>L</sub> = 510 Ω, C <sub>L</sub> = 50 pF                                   |           | 16               | 29    | ns     |
| Break-Before-Make Time   | t <sub>BBM</sub>                    | R <sub>L</sub> = 510 Ω, C <sub>L</sub> = 50 pF                                   | 5         | 10               |       | ns     |
| Maximum Data Rate  |                                     | V <sub>CC</sub> = 3.3 V; V <sub>A</sub> /V <sub>B</sub> = 2 V                    |           | 1.244            |       | Gbps   |
| Channel Jitter   |                                     | V <sub>CC</sub> = 3.3 V; V <sub>A</sub> /V <sub>B</sub> = 2 V                    |           | 45               |       | ps p-p |
| DIGITAL SWITCH   |                                     |  |           |                  |       |        |
| On Resistance  | R <sub>ON</sub>                     | V <sub>CC</sub> = 3 V, V <sub>A</sub> = 0 V, I <sub>BA</sub> = 8 mA              |           | 4.5              | 8     | Ω      |
|  |                                     | V <sub>CC</sub> = 3 V, V <sub>A</sub> = 1.7 V, I <sub>BA</sub> = 8 mA            |           | 12               | 28    | Ω      |
|  |                                     | V <sub>CC</sub> = 2.3 V, V <sub>A</sub> = 0 V, I <sub>BA</sub> = 8 mA            |           | 5                | 9     | Ω      |
|  |                                     | V <sub>CC</sub> = 2.3 V, V <sub>A</sub> = 1 V, I <sub>BA</sub> = 8 mA            |           | 9                | 18    | Ω      |
| On-Resistance Matching   | ΔR <sub>ON</sub>                    | V <sub>CC</sub> = 3 V, V <sub>A</sub> = 0 V, I <sub>A</sub> = 8 mA               |           | 0.1              | 0.5   | Ω      |
| POWER REQUIREMENTS   |                                     |  |           |                  |       |        |
| V <sub>CC</sub>  |                                     |  | 2.3       |                  | 3.6   | V      |
| Quiescent Power Supply Current                                   | I <sub>CC</sub>                     | Digital inputs = 0 V or V <sub>CC</sub>  |           | 0.01             | 1     | μA     |

<sup>1</sup> Temperature range is as follows for B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> Typical values are at  $25^\circ\text{C}$ , unless otherwise stated.

<sup>3</sup> Guaranteed by design, not subject to production test.

<sup>4</sup> The digital switch contributes no propagation delay other than the resistance-capacitance (RC) delay of the typical  $R_{ON}$  of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

<sup>5</sup> Propagation delay matching between channels is calculated from the on-resistance matching and load capacitance of  $50 \text{ pF}$ .

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

| Parameter                            | Rating                                    |
|--------------------------------------|---|
| $V_{CC}$ to GND                      | $-0.5\text{ V to }+4.6\text{ V}$          |
| Digital Inputs to GND                | $-0.5\text{ V to }+4.6\text{ V}$          |
| DC Input Voltage                     | $-0.5\text{ V to }+4.6\text{ V}$          |
| DC Output Current                    | 25 mA per channel                         |
| Operating Temperature Range          |   |
| Industrial (B Version)               | $-40^\circ\text{C to }+85^\circ\text{C}$  |
| Storage Temperature Range            | $-65^\circ\text{C to }+150^\circ\text{C}$ |
| Junction Temperature                 | $150^\circ\text{C}$                       |
| $\theta_{JA}$ Thermal Impedance      | $332^\circ\text{C/W}$                     |
| Lead Soldering                       |   |
| Lead Temperature, Soldering (10 sec) | $300^\circ\text{C}$                       |
| IR Reflow, Peak Temperature          | $220^\circ\text{C}$                       |
| Pb-Free Soldering                    |   |
| Reflow, Peak Temperature             | $260(+0/-5)^\circ\text{C}$                |
| Time at Peak Temperature             | 20 sec to 40 sec                          |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

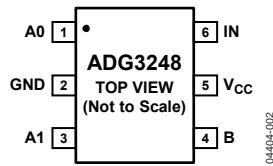


Figure 2. 6-Lead SC70

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic        | Description                    |
|---------|-----------------|--------------------------------|
| 1       | A0              | Port A0, Input or Output.      |
| 2       | GND             | Ground Reference.              |
| 3       | A1              | Port A1, Input or Output.      |
| 4       | B               | Port B, Input or Output.       |
| 5       | V <sub>CC</sub> | Positive Power Supply Voltage. |
| 6       | IN              | Channel Select.                |

# TYPICAL PERFORMANCE CHARACTERISTICS

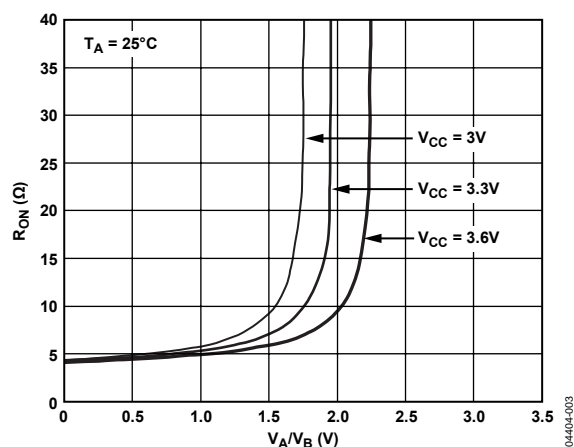


Figure 3. On Resistance vs. Input Voltage

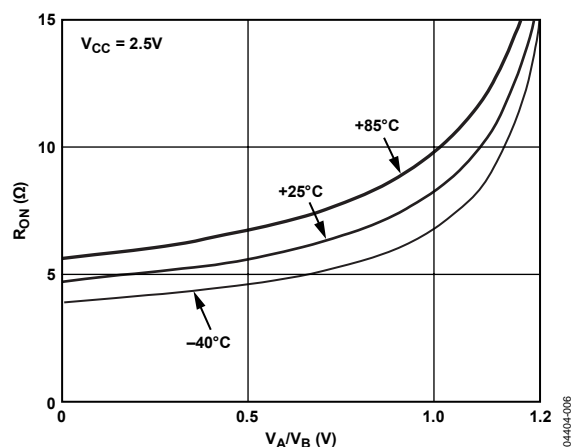


Figure 6. On Resistance vs. Input Voltage for Different Temperatures

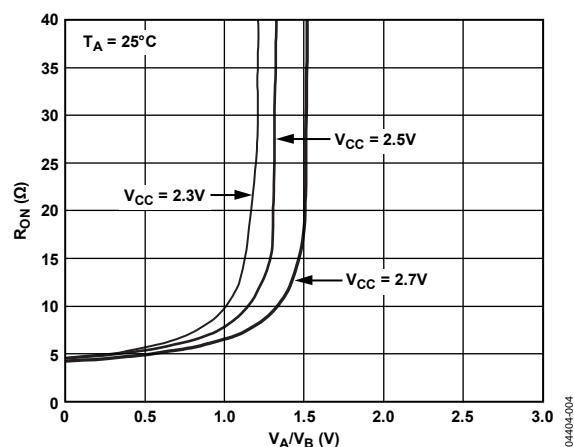


Figure 4. On Resistance vs. Input Voltage

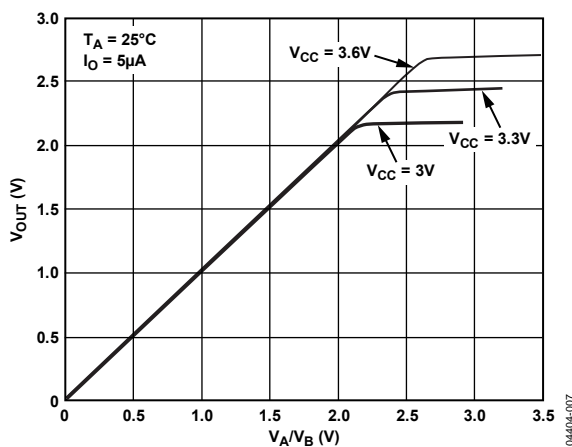


Figure 7. Pass Voltage vs.  $V_{CC}$

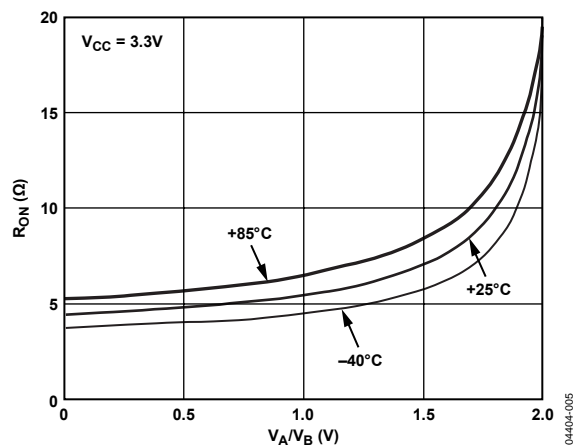


Figure 5. On Resistance vs. Input Voltage for Different Temperatures

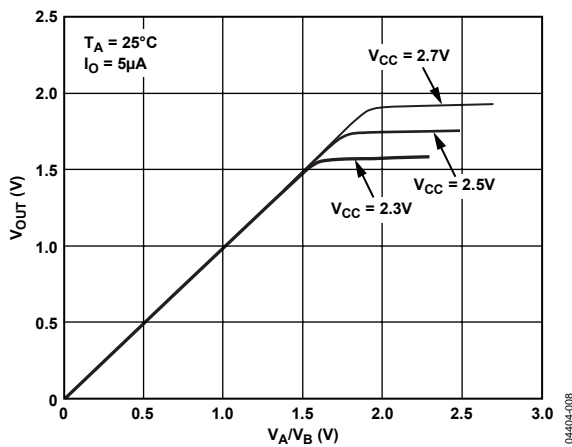


Figure 8. Pass Voltage vs.  $V_{CC}$

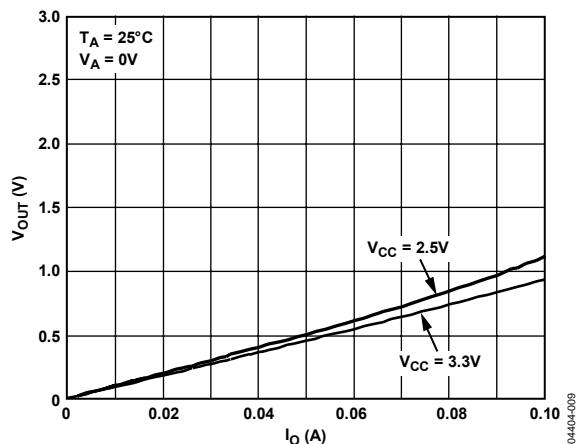


Figure 9. Output Low Characteristic

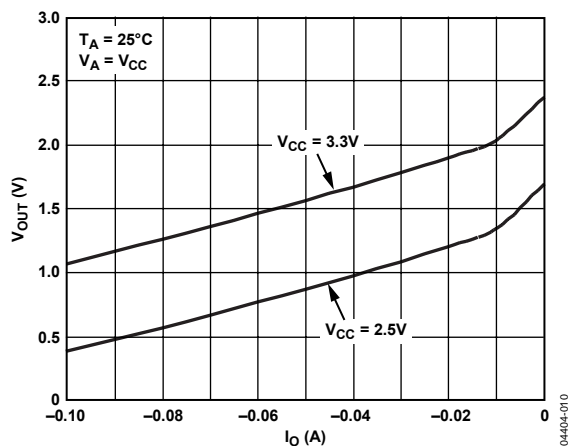


Figure 10. Output High Characteristic

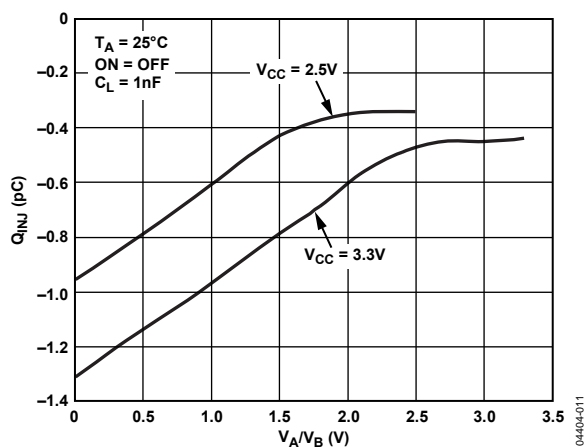


Figure 11. Charge Injection vs. Input Voltage

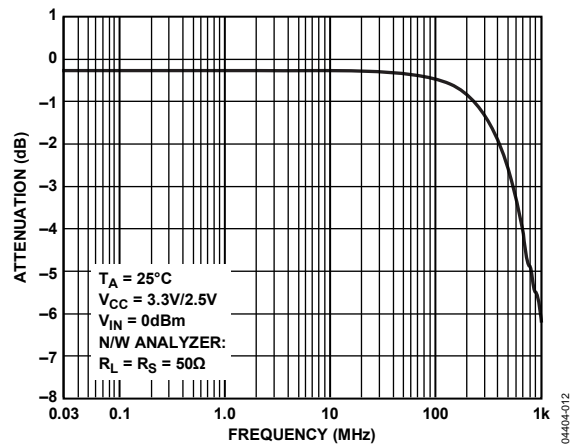


Figure 12. Bandwidth vs. Frequency

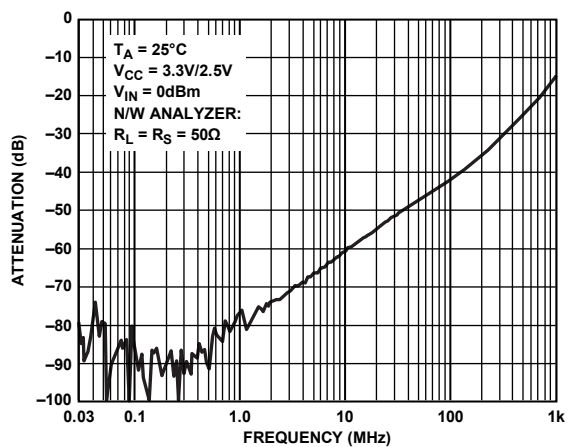


Figure 13. Crosstalk vs. Frequency

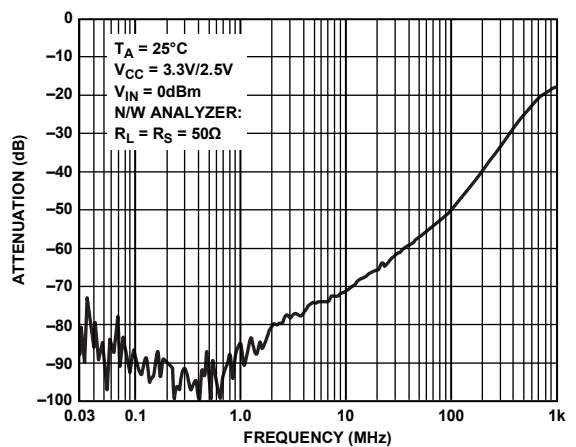


Figure 14. Off Isolation vs. Frequency

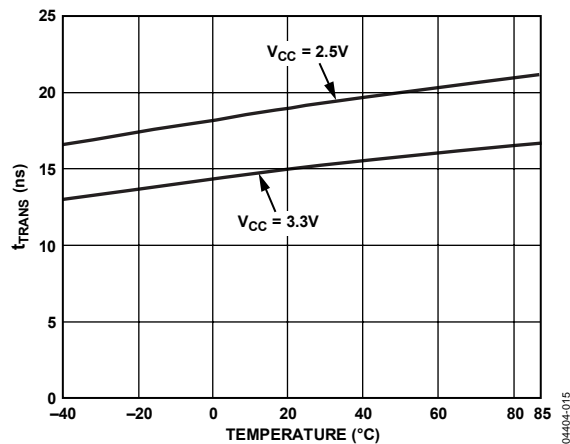


Figure 15. Transition Time vs. Temperature

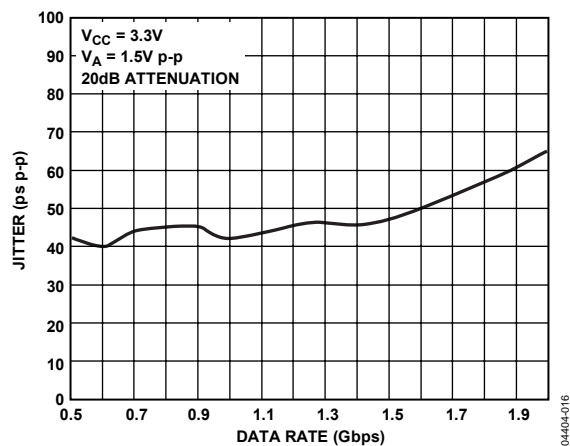


Figure 16. Jitter vs. Data Rate; PRBS 31

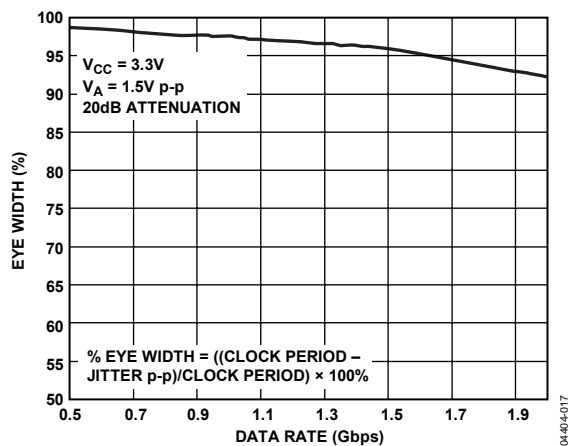


Figure 17. Eye Width vs. Data Rate; PRBS 31

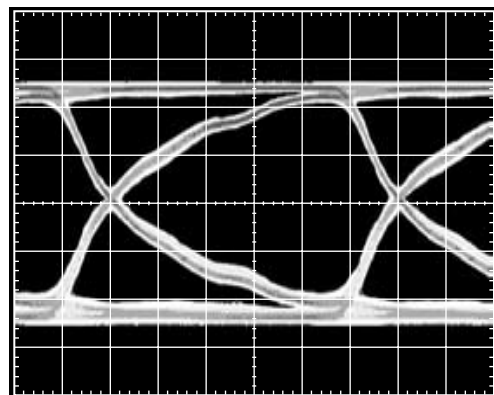


Figure 18. Eye Pattern; 1.244 Gbps,  $V_{CC} = 3.3 V$ , PRBS 31

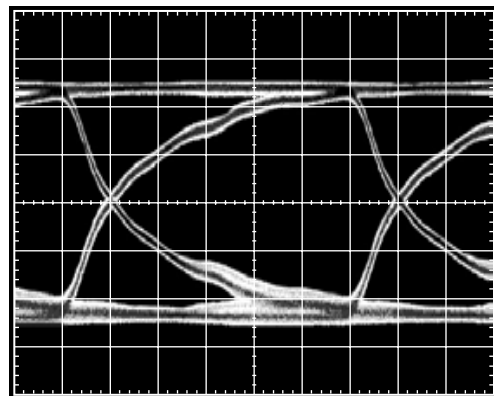


Figure 19. Eye Pattern; 1 Gbps,  $V_{CC} = 2.5 V$ , PRBS 31



## TERMINOLOGY

**V<sub>CC</sub>**

Positive power supply voltage.

**GND**

Ground (0 V) reference.

**V<sub>INH</sub>**

Minimum input voltage for Logic 1.

**V<sub>INL</sub>**

Maximum input voltage for Logic 0.

**I<sub>I</sub>**

Input leakage current at the control inputs.

**I<sub>OZ</sub>**

Off state leakage current. I<sub>OZ</sub> is the maximum leakage current at the switch pin in the off state.

**I<sub>OL</sub>**

On state leakage current. I<sub>OL</sub> is the maximum leakage current at the switch pin in the on state.

**V<sub>P</sub>**

Maximum pass voltage. V<sub>P</sub> relates to the clamped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.

**R<sub>ON</sub>**

Ohmic resistance offered by a switch in the on state. R<sub>ON</sub> is measured at a given voltage by forcing a specified amount of current through the switch.

**ΔR<sub>ON</sub>**

On resistance match between any two channels, that is, R<sub>ON max</sub> – R<sub>ON min</sub>.

**C<sub>X Off</sub>**

Off switch capacitance.

**C<sub>X On</sub>**

On switch capacitance.

**C<sub>IN</sub>**

Control input capacitance. C<sub>IN</sub> consists of I<sub>N</sub>.

**I<sub>CC</sub>**

Quiescent power supply current. I<sub>CC</sub> represents the leakage current between the V<sub>CC</sub> and ground pins and is measured when all control inputs are at a logic high or logic low level and the switches are off.

**t<sub>PLH</sub>, t<sub>PHL</sub>**

Data propagation delay through the switch in the on state. Propagation delay is related to the RC time constant R<sub>ON</sub> × C<sub>L</sub>, where C<sub>L</sub> is the load capacitance.

**t<sub>BBM</sub>**

On or off time measured between the 90% points of both switches when switching from one to another.

**t<sub>TRANS</sub>**

Time taken to switch from one channel to the other, measured from 50% of the in signal to 90% of the out signal.

**Maximum Data Rate**

Maximum rate at which data can be passed through the switch.

**Channel Jitter**

Peak-to-peak value of the sum of the deterministic and random jitter of the switch channel.

## BUS SWITCH APPLICATIONS

### MIXED VOLTAGE OPERATION, LEVEL TRANSLATION

Bus switches can provide an ideal solution for interfacing between mixed voltage systems. The ADG3248 is suitable for applications in which voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 2.5 V to 1.8 V or bidirectionally from 3.3 V directly to 2.5 V.

Figure 20 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs; therefore, placing the ADG3248 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

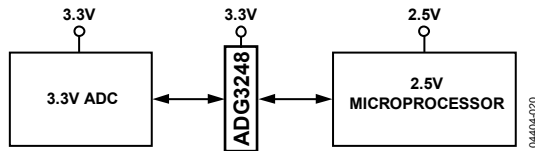


Figure 20. Level Translation Between a 3.3 V ADC and a 2.5 V Microprocessor

#### 3.3 V to 2.5 V Translation

When  $V_{CC}$  is 3.3 V and the input signal range is 0 V to  $V_{CC}$ , the maximum output signal is clamped to within a voltage threshold below the  $V_{CC}$  supply.

In this case, the output is limited to 2.5 V, as shown in Figure 22. This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

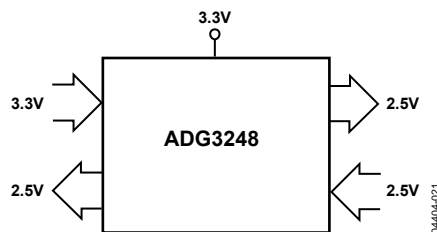


Figure 21. 3.3 V to 2.5 V Voltage Translation

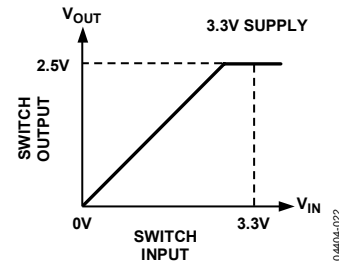


Figure 22. 3.3 V to 2.5 V Voltage Translation

#### 2.5 V to 1.8 V Translation

When  $V_{CC}$  is 2.5 V and the input signal range is 0 V to  $V_{CC}$ , the maximum output signal is, as before, clamped to within a voltage threshold below the  $V_{CC}$  supply. In this case, the output is limited to approximately 1.8 V, as shown in Figure 24.

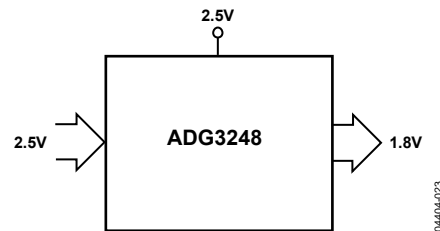


Figure 23. 2.5 V to 1.8 V Voltage Translation

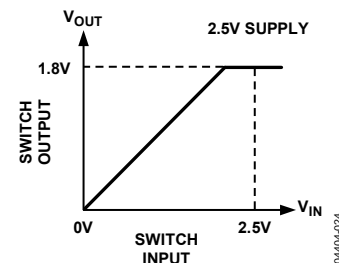


Figure 24. 2.5 V to 1.8 V Voltage Translation

## ANALOG SWITCHING

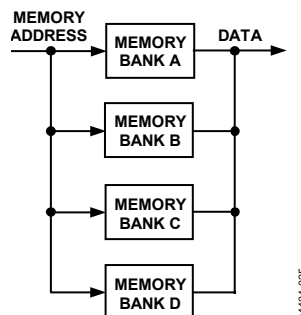
Bus switches can be used in many analog switching applications, for example, video graphics. Bus switches can have lower on resistance, smaller on and off channel capacitance, and thus better frequency performance than their analog counterparts. The bus switch channel itself, consisting solely of an NMOS switch, limits the operating voltage (see Figure 3 for a typical plot) but, in many cases, this does not present an issue.

## MULTIPLEXING

Many systems, such as docking stations and memory banks, have a large number of common bus signals. Common problems faced by designers of these systems include

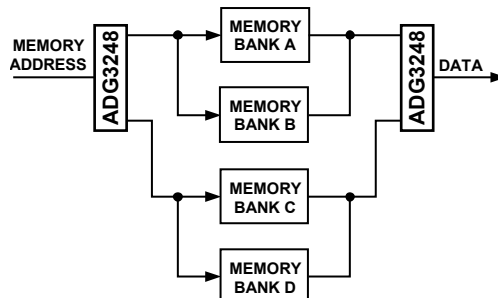
- Large delays caused by capacitive loading of the bus
- Noise due to simultaneous switching of the address and data bus signals

Figure 25 shows an array of memory banks in which each address and data signal is loaded by the sum of the individual loads. If a bus switch is used as shown in Figure 26, the output load on the memory address and data bits is halved. The speed at which data from the selected bank can flow is much improved because the capacitance loading is halved and the switches introduce negligible propagation delay. Bus noise is also reduced.



04404-025

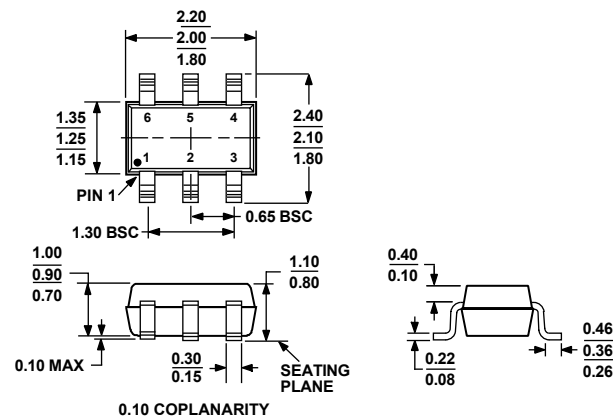
Figure 25. All Memory Banks Are Permanently Connected to the Bus



04404-026

Figure 26. ADG3248 Used to Reduce Both Access Time and Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AB  
Figure 27. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]  
(KS-6)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model                          | Temperature Range | Package Description  | Package Option | Branding |
|--------------------------------|-------------------|--|----------------|----------|
| ADG3248BKS-R2                  | −40°C to +85°C    | 6-Lead Thin Shrink Small Outline Transistor Package (SC70) | KS-6           | SMA      |
| ADG3248BKS-REEL                | −40°C to +85°C    | 6-Lead Thin Shrink Small Outline Transistor Package (SC70) | KS-6           | SMA      |
| ADG3248BKS-REEL7               | −40°C to +85°C    | 6-Lead Thin Shrink Small Outline Transistor Package (SC70) | KS-6           | SMA      |
| ADG3248BKSZ-REEL7 <sup>1</sup> | −40°C to +85°C    | 6-Lead Thin Shrink Small Outline Transistor Package (SC70) | KS-6           | S1W      |

<sup>1</sup> Z = RoHS Compliant Part.