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REVISION HISTORY

10/12—Rev. B to Rev. C

|                                                            |           |
|------------------------------------------------------------|-----------|
| Updated Format.....                                        | Universal |
| Added Pin Descriptions, Table 3 .....                      | 5         |
| Moved Table 4 .....                                        | 5         |
| Changes to Figure 5, Figure 6, Figure 8, and Figure 9..... | 6         |
| Updated Outline Dimensions .....                           | 13        |
| Changes to Ordering Guide .....                            | 14        |

9/02—Rev. A to Rev. B

## SPECIFICATIONS

$V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $V_L = 5\text{ V}$ , unless otherwise noted.

Table 1.

| Parameter                                            | 25°C |     |     | –40°C to +85°C |     |     | Unit | Test Conditions/Comments                                                            |
|------------------------------------------------------|------|-----|-----|----------------|-----|-----|------|-------------------------------------------------------------------------------------|
|                                                      | Min  | Typ | Max | Min            | Typ | Max |      |                                                                                     |
| ANALOG SWITCH                                        |      |     |     |                |     |     |      |                                                                                     |
| Analog Signal Range                                  |      | ±15 |     |                | ±15 |     | V    | –10 V ≤ V <sub>S</sub> ≤ +10 V, I <sub>DS</sub> = 1 mA, see Figure 21               |
| R <sub>ON</sub>                                      |      |     | 115 |                |     | 175 | Ω    |                                                                                     |
| R <sub>ON</sub> vs. V <sub>D</sub> (V <sub>S</sub> ) |      | 20  |     |                |     |     | %    |                                                                                     |
| R <sub>ON</sub> Drift                                |      | 0.5 |     |                |     |     | %/°C |                                                                                     |
| R <sub>ON</sub> Match                                |      | 5   |     |                |     |     | %    |                                                                                     |
| V <sub>S</sub> = 0 V, I <sub>DS</sub> = 1 mA         |      |     |     |                |     |     |      |                                                                                     |
| LEAKAGE CURRENTS                                     |      |     |     |                |     |     |      |                                                                                     |
| I <sub>S</sub> (Off)                                 |      | 0.5 |     |                |     |     | nA   | V <sub>D</sub> = ±14 V; V <sub>S</sub> = ∓ 14 V; see Figure 22                      |
| Off Input Leakage                                    |      |     | 5   |                |     | 100 | nA   |                                                                                     |
| I <sub>D</sub> (Off)                                 |      | 0.5 |     |                |     |     | nA   | V <sub>D</sub> = ±14 V; V <sub>S</sub> = ∓ 14 V; see Figure 22                      |
| Off Output Leakage                                   |      |     | 5   |                |     | 100 | nA   |                                                                                     |
| I <sub>D</sub> (On)                                  |      | 0.5 |     |                |     |     | nA   | V <sub>D</sub> = V <sub>S</sub> = ±14 V; see Figure 23                              |
| On Channel Leakage                                   |      |     | 5   |                |     | 200 | nA   |                                                                                     |
| DIGITAL CONTROL                                      |      |     |     |                |     |     |      |                                                                                     |
| V <sub>INH</sub> , Input High Voltage                |      |     |     | 2.4            |     |     | V    | TTL compatibility is independent of V <sub>L</sub>                                  |
| V <sub>INL</sub> , Input Low Voltage                 |      |     |     |                |     | 0.8 | V    |                                                                                     |
| I <sub>NL</sub> or I <sub>NH</sub>                   |      |     |     |                |     | 1   | μA   |                                                                                     |
| C <sub>IN</sub> , Digital Input Capacitance          |      | 5   |     |                |     |     | pF   |                                                                                     |
| DYNAMIC CHARACTERISTICS                              |      |     |     |                |     |     |      |                                                                                     |
| t <sub>OPEN</sub> <sup>1</sup>                       |      | 30  |     |                |     |     | ns   | See Figure 24                                                                       |
| t <sub>ON</sub> <sup>1</sup>                         |      |     | 600 |                |     |     | ns   | See Figure 25                                                                       |
| t <sub>OFF</sub> <sup>1</sup>                        |      |     | 450 |                |     |     | ns   | See Figure 25                                                                       |
| Off Isolation                                        |      | 80  |     |                |     |     | dB   | V <sub>S</sub> = 10 V (p-p); f = 100 kHz;<br>R <sub>L</sub> = 75 Ω; see Figure 26   |
| Channel-to-Channel Crosstalk                         |      | 80  |     |                |     |     | dB   | See Figure 27                                                                       |
| C <sub>S</sub> (Off)                                 |      | 5   |     |                |     |     | pF   | R <sub>S</sub> = 0 Ω; C <sub>L</sub> = 1000 pF; V <sub>S</sub> = 0 V; see Figure 28 |
| C <sub>D</sub> (Off)                                 |      | 5   |     |                |     |     | pF   |                                                                                     |
| C <sub>S</sub> , C <sub>D</sub> (On)                 |      | 16  |     |                |     |     | pF   |                                                                                     |
| Q <sub>INJ</sub> , Charge Injection                  |      | 20  |     |                |     |     | pC   |                                                                                     |
|                                                      |      |     |     |                |     |     |      |                                                                                     |
| POWER SUPPLY                                         |      |     |     |                |     |     |      |                                                                                     |
| I <sub>DD</sub>                                      |      | 0.6 |     |                |     |     | mA   | Digital inputs = V <sub>INL</sub> or V <sub>INH</sub>                               |
| I <sub>DD</sub>                                      |      |     | 1   |                |     |     | mA   |                                                                                     |
| I <sub>SS</sub>                                      |      | 0.1 |     |                |     |     | mA   |                                                                                     |
| I <sub>SS</sub>                                      |      |     | 0.2 |                |     |     | mA   |                                                                                     |
| I <sub>L</sub>                                       |      |     | 0.9 |                |     |     | mA   |                                                                                     |

<sup>1</sup> Sample tested at 25°C to ensure compliance.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise stated.

Table 2.

| Parameter                            | Rating                                                                                  |
|--------------------------------------|-----------------------------------------------------------------------------------------|
| $V_{DD}$ to $V_{SS}$                 | 44 V                                                                                    |
| $V_{DD}$ to GND                      | 25 V                                                                                    |
| $V_{SS}$ to GND                      | -25 V                                                                                   |
| $V_L$ to GND                         | -0.3 V, 25 V                                                                            |
| Analog Inputs <sup>1</sup>           |                                                                                         |
| Voltage at S, D                      | $V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$                                    |
| Continuous Current, S or D           | 30 mA                                                                                   |
| Pulsed Current S or D                |                                                                                         |
| 1 ms Duration, 10% Duty Cycle        | 70 mA                                                                                   |
| Digital Inputs <sup>1</sup>          |                                                                                         |
| Voltage at IN                        | $V_{SS} - 2 \text{ V}$ to $V_{DD} + 2 \text{ V}$ or<br>20 mA, Whichever<br>Occurs First |
| Power Dissipation (Any Package)      |                                                                                         |
| Up to $+75^\circ\text{C}$            | 470 mW                                                                                  |
| Derates above $+75^\circ\text{C}$ by | 6 mW/ $^\circ\text{C}$                                                                  |
| Operating Temperature                | $-40^\circ\text{C}$ to $+85^\circ\text{C}$                                              |
| Storage Temperature Range            | $-65^\circ\text{C}$ to $+150^\circ\text{C}$                                             |
| Lead Temperature (Soldering 10 sec)  | $+300^\circ\text{C}$                                                                    |

<sup>1</sup> Overvoltage at IN, S, or D will be clamped by diodes. Current should be limited to the Maximum Rating listed in Table 2.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

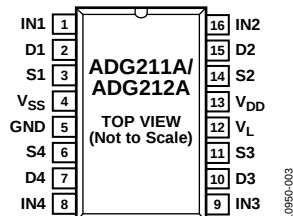
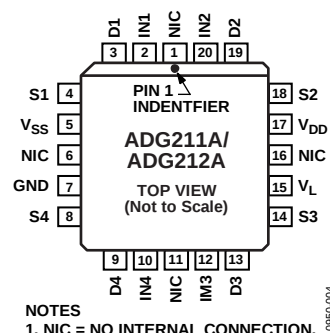


Figure 3. PDIP, SOIC Pin Configuration



NOTES  
1. NIC = NO INTERNAL CONNECTION.

Figure 4. PLCC Pin Configuration

Table 3. Pin Function Descriptions

| Pin No.    |              | Mnemonic        | Description                                 |
|------------|--------------|-----------------|---------------------------------------------|
| PDIP, SOIC | PLCC         |                 |                                             |
| 1          | 2            | IN1             | Logic Control Input.                        |
| 2          | 3            | D1              | Drain Terminal. Can be an input or output.  |
| 3          | 4            | S1              | Source Terminal. Can be an input or output. |
| 4          | 5            | V <sub>SS</sub> | Most Negative Power Supply Potential.       |
| 5          | 7            | GND             | Ground (0 V) Reference.                     |
| 6          | 8            | S4              | Source Terminal. Can be an input or output. |
| 7          | 9            | D4              | Drain Terminal. Can be an input or output.  |
| 8          | 10           | IN4             | Logic Control Input.                        |
| 9          | 12           | IN3             | Logic Control Input.                        |
| 10         | 13           | D3              | Drain Terminal. Can be an input or output.  |
| 11         | 14           | S3              | Source Terminal. Can be an input or output. |
| 12         | 15           | V <sub>L</sub>  | Logic Supply Voltage.                       |
| 13         | 17           | V <sub>DD</sub> | Most Positive Power Supply Potential.       |
| 14         | 18           | S2              | Source Terminal. Can be an input or output. |
| 15         | 19           | D2              | Drain Terminal. Can be an input or output.  |
| 16         | 20           | IN2             | Logic Control Input.                        |
|            | 1, 6, 11, 16 | NIC             | No Internal Connection.                     |

Table 4. Truth Table

| ADG211A In | ADG212A In | Switch Condition |
|------------|------------|------------------|
| 0          | 1          | On               |
| 1          | 0          | Off              |

## TYPICAL PERFORMANCE CHARACTERISTICS

The switches can comfortably operate anywhere in the 10 V to 15 V single or dual supply range, with only a slight degradation in performance. The following graphs show the relevant performance curves. The test circuits and test conditions are given in a following section, Test Circuits.

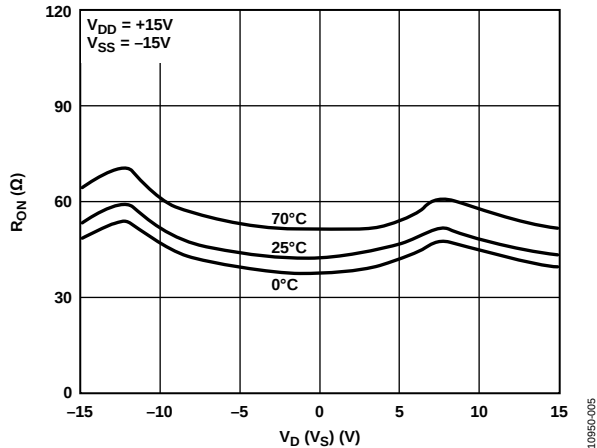


Figure 5.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ), Dual  $\pm 15$  V Supplies

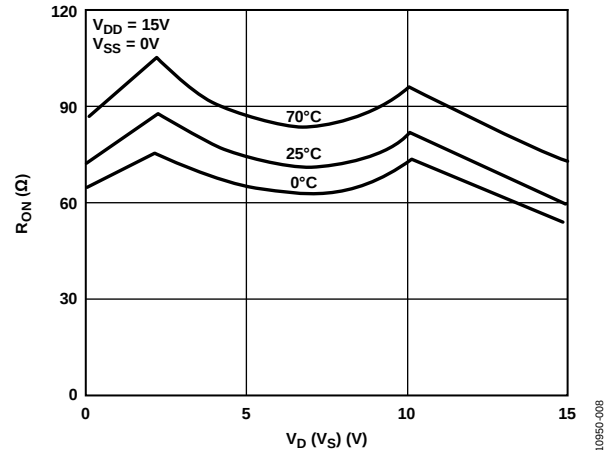


Figure 8.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ), Single +15 V Supply

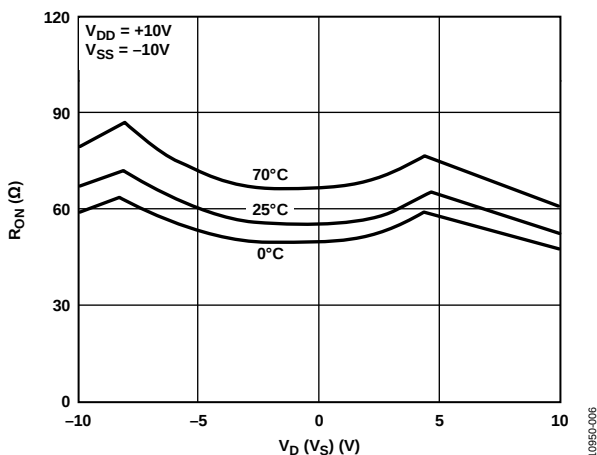


Figure 6.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ), Dual  $\pm 10$  V Supplies

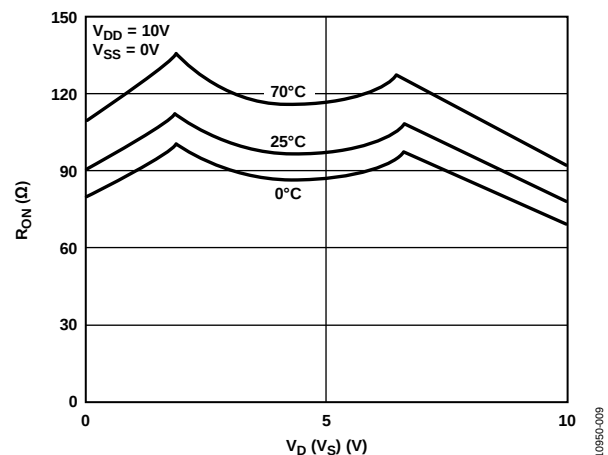


Figure 9.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ), Single +10 V Supply

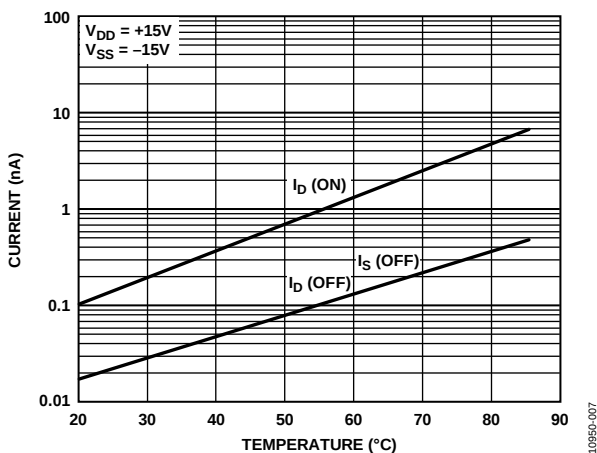


Figure 7. Leakage Current as a Function of Temperature  
(Note That Leakage Current Reduces as the Supply Voltages Reduce)

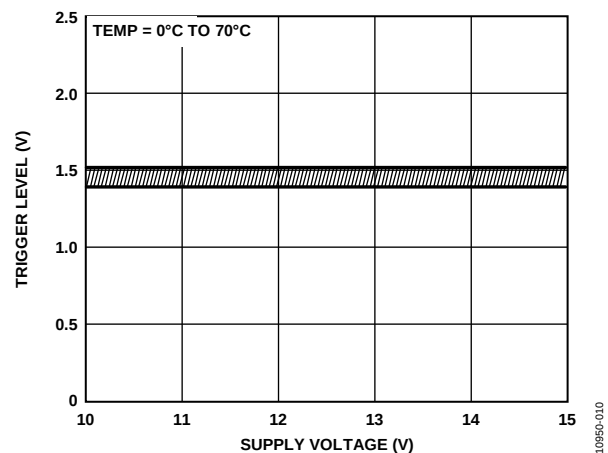


Figure 10. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply Voltage

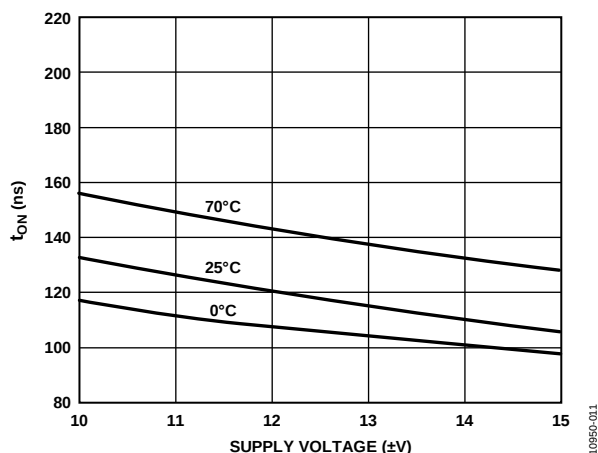
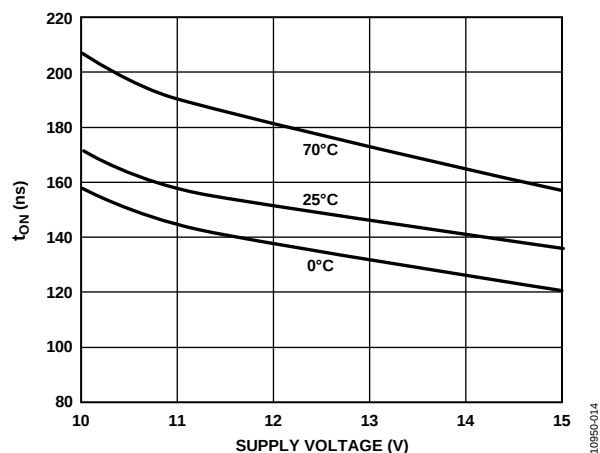
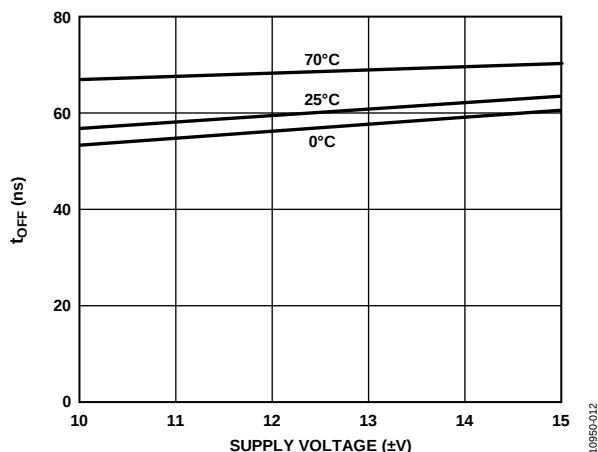
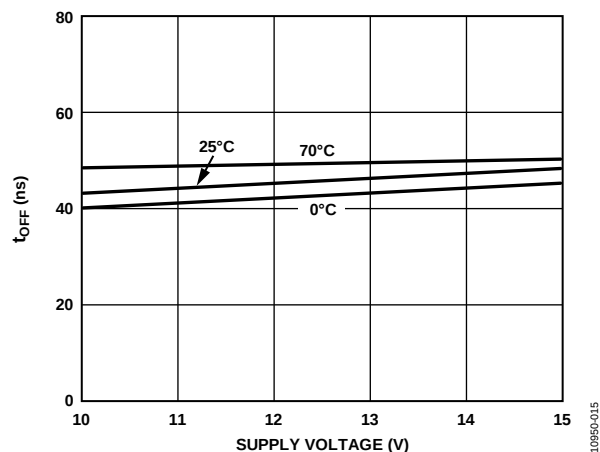
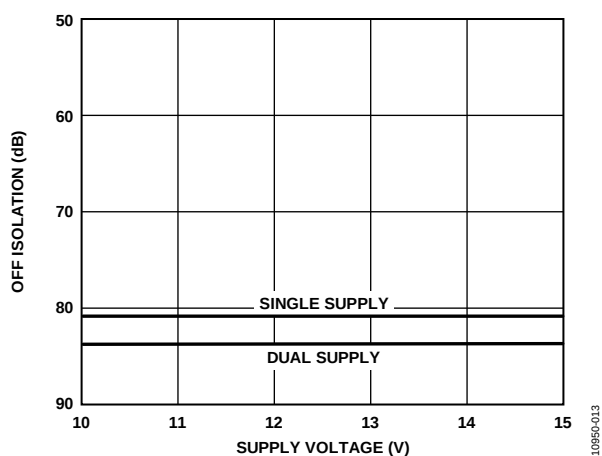
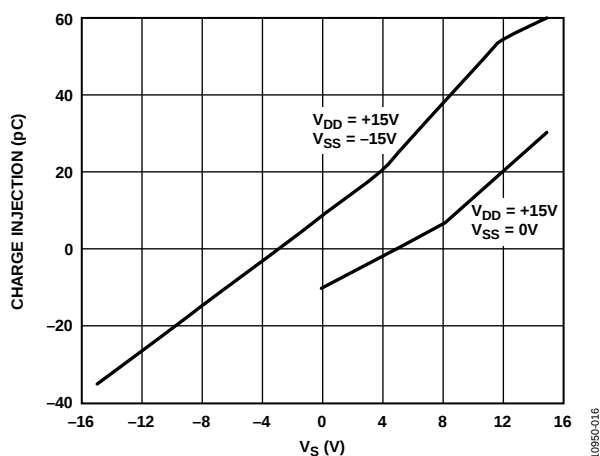
Figure 11. t<sub>ON</sub> vs. Supply Voltage (Dual Supply)Figure 14. t<sub>ON</sub> vs. Supply Voltage (Single Supply)Figure 12. t<sub>OFF</sub> vs. Supply Voltage (Dual Supply)Figure 15. t<sub>OFF</sub> vs. Supply Voltage (Single Supply)

Figure 13. Off Isolation and Channel-to-Channel Crosstalk vs. Supply Voltage

Figure 16. Charge Injection vs. Source Voltage (V<sub>S</sub>) for Dual and Single 15 V Supplies

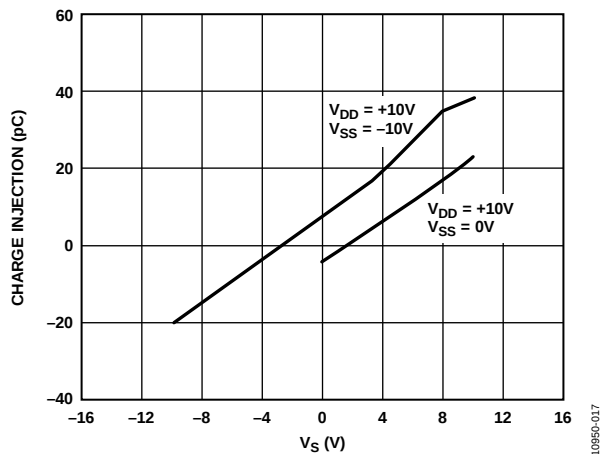


Figure 17. Charge Injection vs. Source Voltage for Dual and Single 10 V Supplies

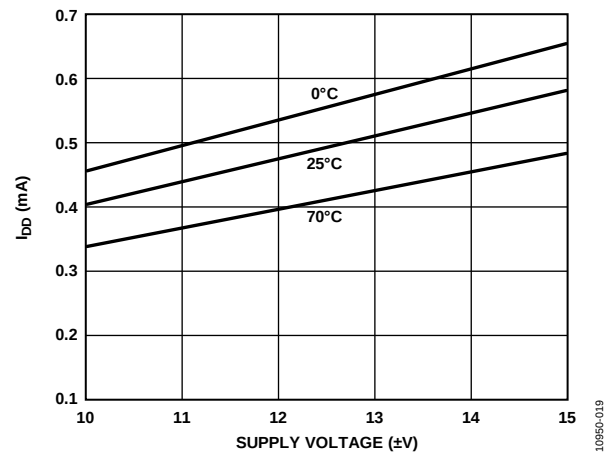


Figure 19.  $I_{DD}$  vs. Supply Voltage, (Dual Supply)

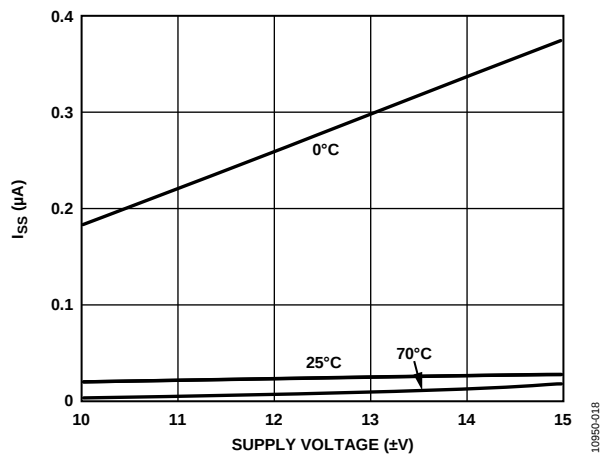


Figure 18.  $I_{SS}$  vs. Supply Voltage (Dual Supply)

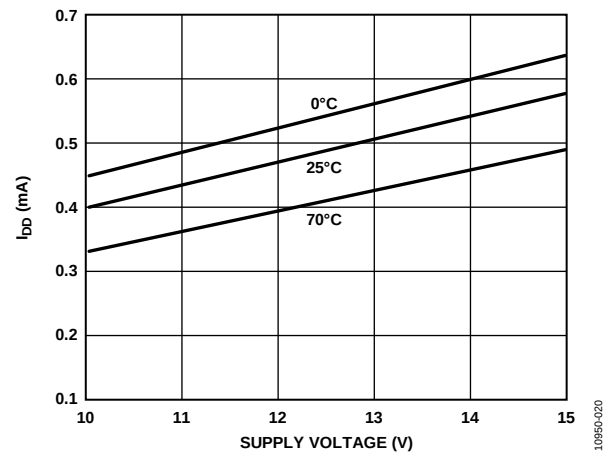


Figure 20.  $I_{DD}$  vs. Supply Voltage (Single Supply)

## TERMINOLOGY

 **$R_{ON}$** 

Ohmic resistance between the out and S terminals.

 **$R_{ON}$  Match**

Difference between the  $R_{ON}$  of any two channels.

 **$I_S$  (Off)**

Source terminal leakage current when the switch is off.

 **$I_D$  (Off)**

Drain terminal leakage current when the switch is off.

 **$I_D$  (On)**

Leakage current that flows from the closed switch into the body.

 **$V_D$  ( $V_S$ )**

Analog voltage on the D, S terminals.

 **$C_S$  (Off)**

Switch input capacitance off condition.

 **$C_D$  (Off)**

Switch output capacitance off condition.

 **$C_{IN}$** 

Digital input capacitance.

 **$C_D$ ,  $C_S$  (On)**

Input or output capacitance when the switch is on.

 **$t_{ON}$** 

Delay time between the 50% and 90% points of the digital input and switch on condition.

 **$t_{OFF}$** 

Delay time between the 50% and 90% points of the digital input and switch off condition.

 **$t_{OPEN}$** 

Off time measured between 50% points of both switches, which are connected as a multiplexer when switching from one address state to another.

 **$V_{INL}$** 

Maximum input voltage for a logic low.

 **$V_{INH}$** 

Minimum input voltage for a logic high.

 **$I_{INL}$  ( $I_{INH}$ )**

Input current of the digital input.

 **$V_{DD}$** 

Most positive voltage supply.

 **$V_{SS}$** 

Most negative voltage supply.

 **$V_L$** 

Logic supply voltage.

 **$I_{DD}$** 

Positive supply current.

 **$I_{SS}$** 

Negative supply current.

## TEST CIRCUITS

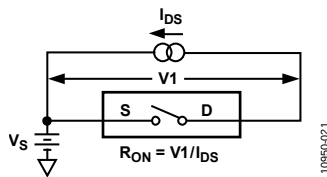


Figure 21.

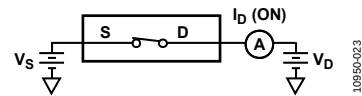


Figure 23.

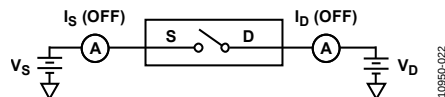


Figure 22.

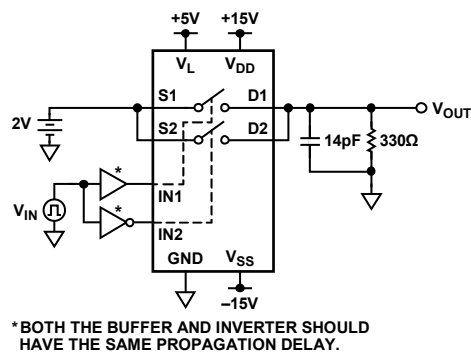


Figure 24.

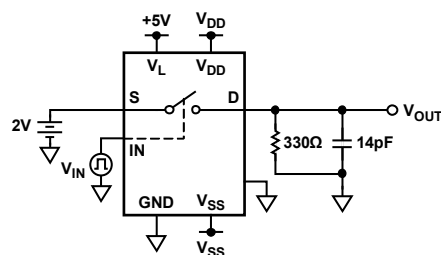
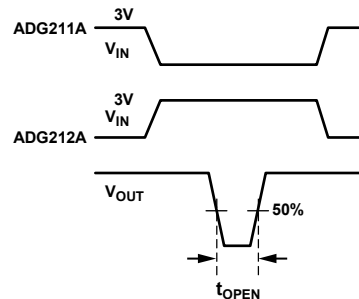
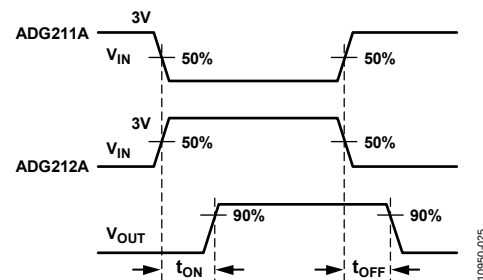


Figure 25.



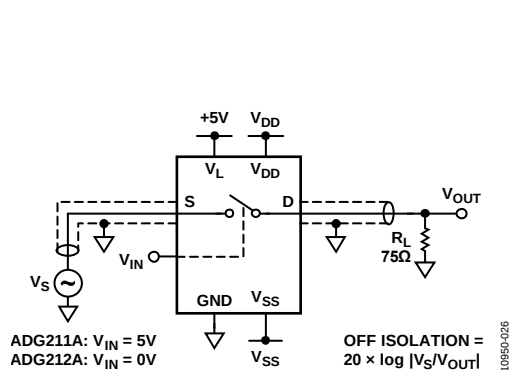


Figure 26. Off Isolation

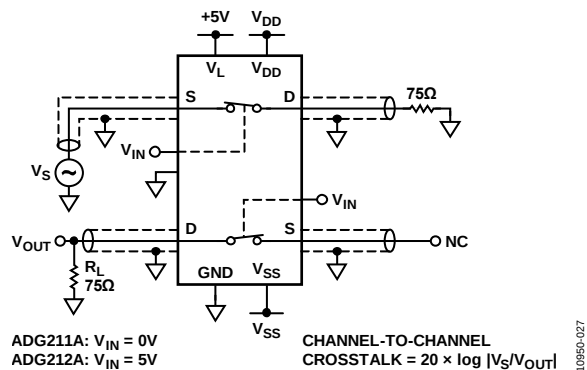


Figure 27. Channel-to-Channel Crosstalk

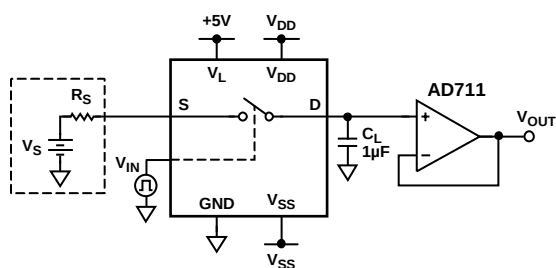
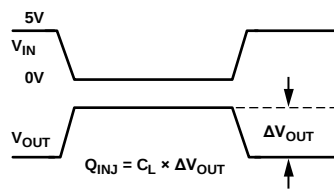
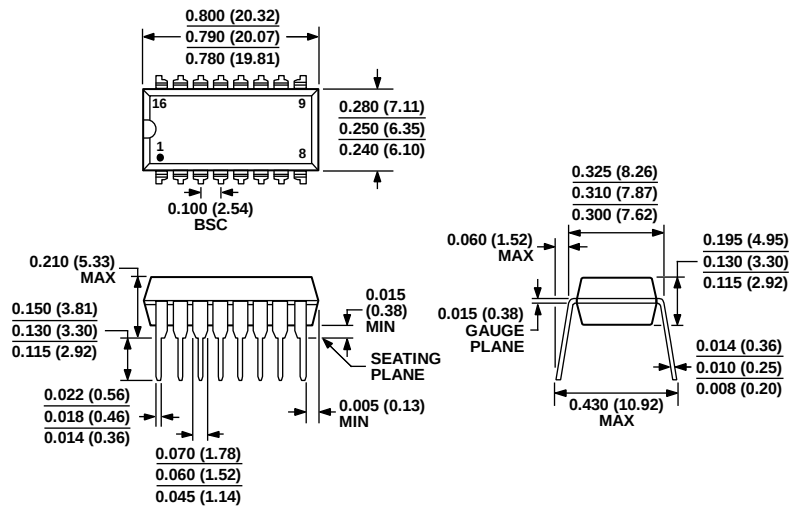


Figure 28. Charge Injection



## OUTLINE DIMENSIONS

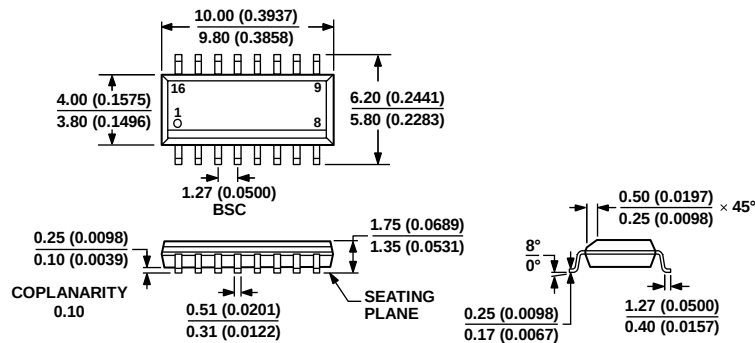


COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 29. 16-Lead Plastic Dual In-Line Package [PDIP]  
Narrow Body  
(N-16)

Dimensions shown in inches and (millimeters)

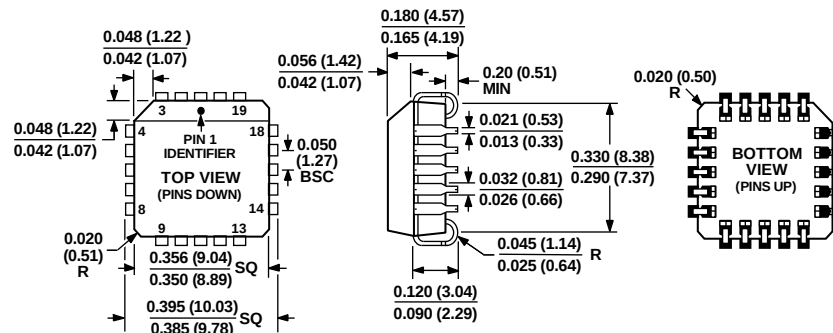


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 30. 16-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-047-AA  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 20-Lead Plastic Leaded Chip Carrier [PLCC]  
(P-20)

Dimensions shown in inches and (millimeters)

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---------------------|----------------|
| ADG211AKN          | -40°C to +85°C    | 16-Lead PDIP        | N-16           |
| ADG211AKNZ         | -40°C to +85°C    | 16-Lead PDIP        | N-16           |
| ADG211AKPZ         | -40°C to +85°C    | 20-Lead PLCC        | P-20           |
| ADG211AKR          | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |
| ADG211AKRZ         | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |
| ADG211AKRZ-REEL    | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |
| ADG211AKRZ-REEL7   | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |
| ADG212AKNZ         | -40°C to +85°C    | 16-Lead PDIP        | N-16           |
| ADG212AKPZ         | -40°C to +85°C    | 20-Lead PLCC        | P-20           |
| ADG212AKPZ-REEL    | -40°C to +85°C    | 20-Lead PLCC        | P-20           |
| ADG212AKR          | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |
| ADG212AKRZ         | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |
| ADG212AKRZ-REEL    | -40°C to +85°C    | 16-Lead SOIC_N      | R-16           |

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

## NOTES

**NOTES**