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REVISION HISTORY

9/13—Rev. 0 to Rev. A

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1/11—Revision 0: Initial Version

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SPECIFICATIONS

VDD1 = VDD2 = 3.3 V ± 10%, GND = 0 V; dBm referred to 50 Ω; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. The operating temperature range is −40°C to +105°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
Input Frequency	4		18	GHz	
RF Input Sensitivity	−10		+10	dBm	4 GHz to 18 GHz
Output Power	−10	−5		dBm	Single-ended output connected into 50 Ω load
	−7	−2		dBm	Differential outputs connected into 100 Ω differential load
Output Voltage Swing	200	330		mV p-p	Peak-to-peak voltage swing on each single-ended output, connected into 50 Ω load
	400	660		mV p-p	Peak-to-peak voltage swing on differential output, connected into 100 Ω differential load
		1000		mV p-p	Peak-to-peak voltage swing on each single-ended output, no load condition
Phase Noise		−147		dBc/Hz	Input frequency (f_{IN}) = 12 GHz, offset = 100 kHz
Reverse Leakage		−60		dBm	RF input power (P_{IN}) = 0 dBm, RF_{OUT} = 4 GHz
Second Harmonic Content		−28		dBc	
Third Harmonic Content		−12		dBc	
Fourth Harmonic Content		−37		dBc	
Fifth Harmonic Content		−19		dBc	
CE INPUT					
Input High Voltage, V_{IH}	2.2			V	
Input Low Voltage, V_{IL}			0.3	V	
POWER SUPPLIES					
Voltage Supply	3.0	3.3	3.6	V	
I_{DD} (I_{DD1} + I_{DD2})					
Active		30	60	mA	CE is high
Power-Down		17	30	mA	CE is low

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDDx to GND	−0.3 V to +3.9 V
RFIN	10 dBm
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	27.3°C/W
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of 2 kV, human body model (HBM) and is ESD sensitive. Implement proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

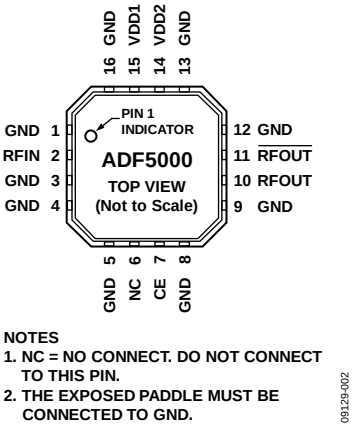

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 5, 8, 9, 12, 13, 16	GND	RF Ground. Tie all ground pins together.
2	RFIN	Single-Ended 50 Ω Input to the RF Prescaler. This pin is ac-coupled internally via a 3 pF capacitor.
6	NC	No Connect. Do not connect to this pin.
7	CE	Chip Enable. This pin is active high. When CE is brought low, the part enters power-down mode. If this functionality is not required, the pin can be left unconnected because it is pulled up internally through a weak pull-up resistor.
10	RFOUT	Divided-Down Output of the Prescaler. This pin has an internal 100 Ω load resistor tied to VDD2 and an ac coupling capacitor of 1 pF.
11	$\overline{\text{RFOUT}}$	Complementary Divided Down Output of the Prescaler. This pin has an internal 100 Ω load resistor tied to VDD2 and an ac coupling capacitor of 1 pF.
14	VDD2	Voltage Supply for the Output Stage. Decouple this pin to ground with a 0.1 µF capacitor in parallel with a 10 pF capacitor. VDD2 can be tied directly to VDD1.
15	VDD1	Voltage Supply for the Input Stage and Divider Block. Decouple this pin to ground with a 0.1 µF capacitor in parallel with a 10 pF capacitor.
	EPAD	The LFCSP has an exposed paddle that must be connected to GND.

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TYPICAL PERFORMANCE CHARACTERISTICS

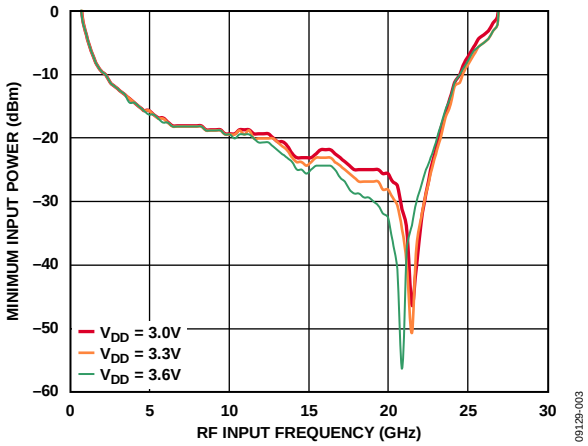

Figure 3. RF Input Sensitivity

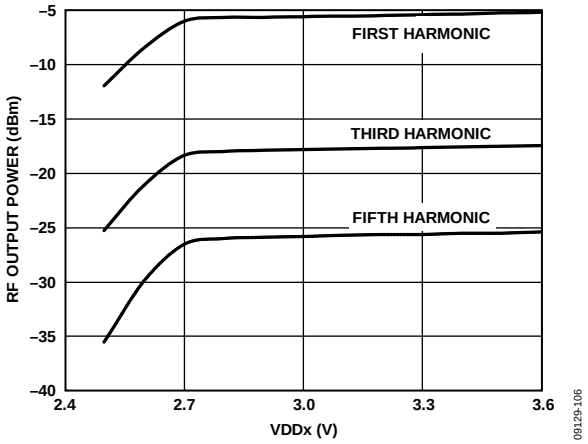

Figure 6. RF Output Harmonic Content vs. VDDx

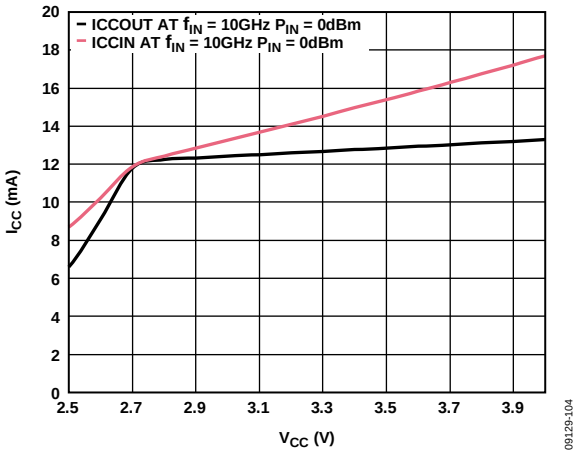

Figure 4. I_{DD1} and I_{DD2} vs. VDDx, f_{IN} = 10 GHz, P_{IN} = 0 dBm

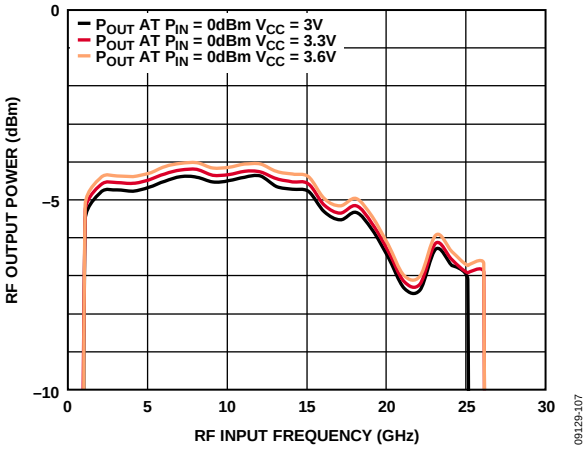

Figure 7. RF Output Power vs. RF Input Frequency, f_{IN} = 10 GHz, V_{DD} = 3.3 V

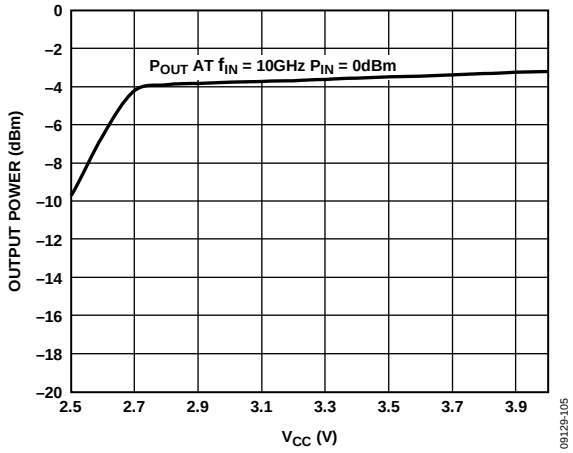

Figure 5. RF Output Power (Single-Ended) vs. VDDx, f_{IN} = 10 GHz, P_{IN} = 0 dBm

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EVALUATION BOARD PCB

The evaluation board has four connectors as shown in Figure 8. The RF input connector (J4) is a high frequency precision SMA connector from Emerson. This connector is mechanically compatible with SMA, 3.5 mm, and 2.92 mm cables.

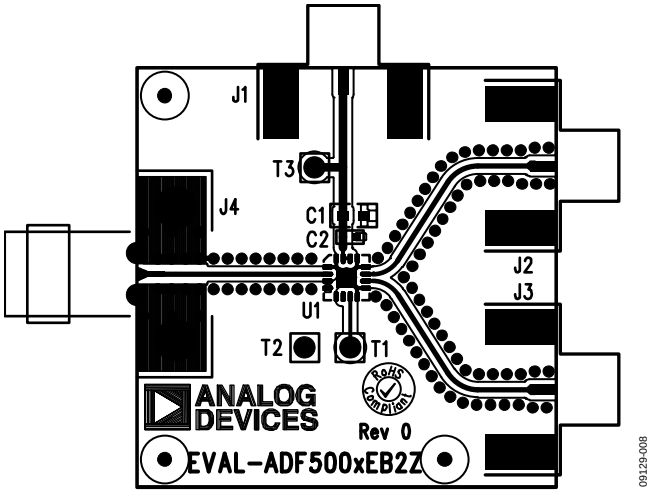

Figure 8. Evaluation Board Silkscreen—Top View

The evaluation board is powered from a single 3.0 V to 3.6 V supply, which should be connected to the J1 SMA connector. The power supply can also be connected using the T3 (VDDx) and T2 (GND) test points.

The differential RF outputs are brought out on the J2 and J3 SMA connectors. If only one of the outputs is being used, the unused output should be correctly terminated using a 50 Ω SMA termination.

The chip enable (CE) pin can be controlled using the T1 test point. If this function is not required, the test point can be left unconnected.

PCB MATERIAL STACK-UP

The evaluation board is built using Rogers RO4003C material (0.008 inch). RF track widths are 0.015 inch to achieve a controlled 50 Ω characteristic impedance. The complete printed circuit board (PCB) stack-up is shown in Figure 9.

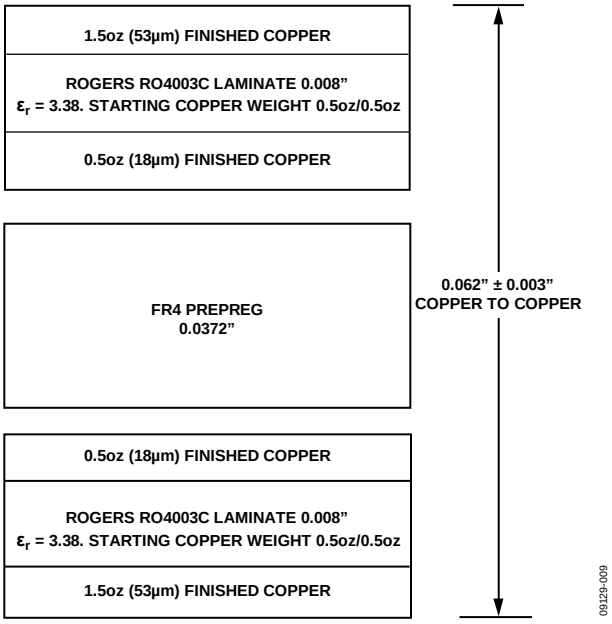

Figure 9. Evaluation Board PCB Layer Stack-Up

BILL OF MATERIALS

Table 4.

Qty.	Reference Designator	Description	Supplier	Part Number
1	C1	0.1 µF, 0603 capacitor	Murata	GRM188R71H104KA93D
1	C2	10 pF, 0402 capacitor	Murata	GRM1555C1H100JZ01D
3	J1, J2, J3	SMA RF connector	Emerson	142-0701-851
1	J4	SMA RF connector	Emerson	142-0761-801
3	T1, T2, T3	Test points	Vero	20-2137
1	U1	ADF5000 RF prescaler	Analog Devices, Inc.	ADF5000BCPZ

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APPLICATION CIRCUIT

The ADF5000 can be connected either single-ended or differentially to any of the Analog Devices PLL family of ICs. It is recommended that a differential connection be used for best performance and to achieve maximum power transfer. The application circuit shown in Figure 10 shows the ADF5000 used as the RF prescaler in a microwave 12 GHz PLL loop. The ADF5000 divides the 12 GHz RF signal down to 6 GHz, which is input differentially into the ADF4156 PLL. An active filter topology, using the OP184 op amp, is used to provide the wide tuning ranges typically required by microwave VCOs.

The positive input pin of the OP184 is biased at half the ADF4156 charge pump supply (V_P). This can be easily achieved using a simple resistor divider, ensuring sufficient decoupling close to the +IN A pin of the OP184. This configuration, in turn, allows the use of a single positive supply for the op amp. Alternatively, to optimize performance by ensuring a clean bias voltage, a low noise regulator such as the ADP150 can be used to power the resistor divider network or the +IN A pin directly.

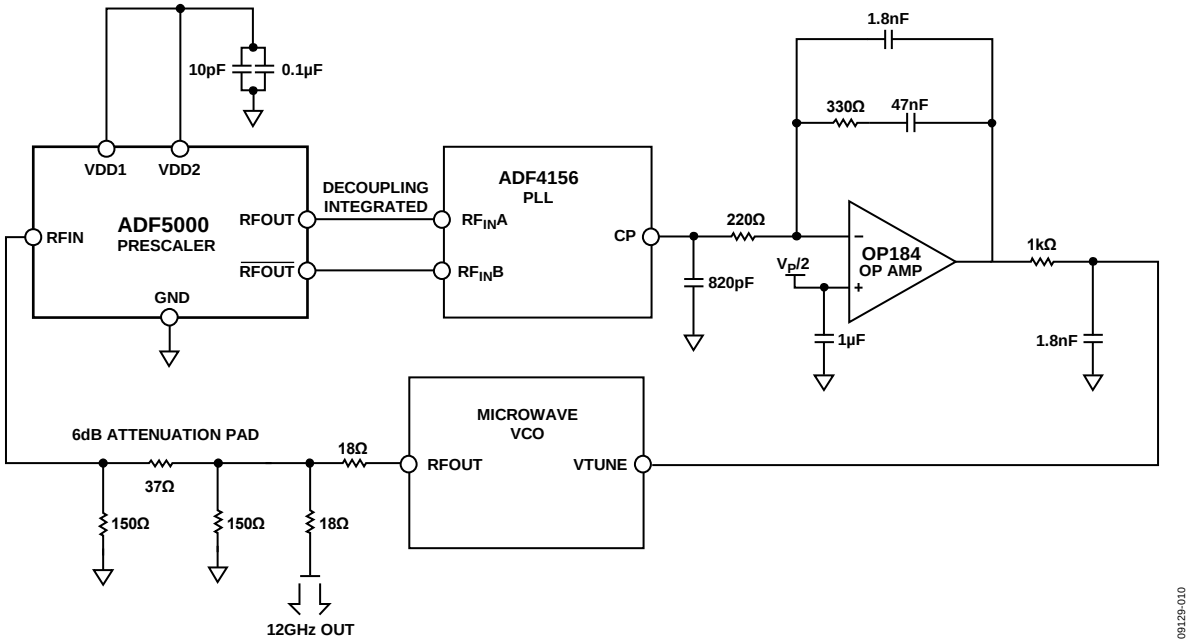

Figure 10. ADF5000 Used as the RF Prescaler in a Microwave 12 GHz PLL Loop

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OUTLINE DIMENSIONS

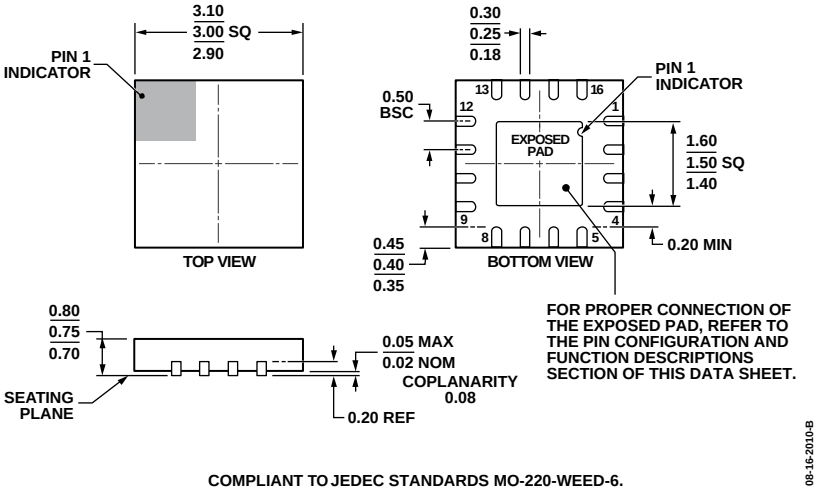

Figure 11. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-18)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADF5000BCPZ	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-18	Q1T
ADF5000BCPZ-RL7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7″Tape and Reel	CP-16-18	Q1T
EVAL-ADF5000EB2Z		Evaluation Board		

[1] Z = RoHS Compliant Part.

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