TABLE OF CONTENTS

Features ... 1
Applications ... 1
Pin Configuration ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 7
Thermal Resistance ... 7
ESD Caution ... 7
Pin Configuration and Function Descriptions ... 8
Typical Performance Characteristics ... 9
Theory of Operation ... 19
Architecture ... 19
Gain Selection ... 19
Reference Terminal ... 20
Input Voltage Range ... 20
Layout ... 20
Input Bias Current Return Path ... 21
Input Protection ... 22
Radio Frequency Interference (RFI) ... 22
Applications Information ... 23
Differential Drive ... 23
Precision Strain Gage ... 24
Driving an ADC ... 24
Outline Dimensions ... 25
Ordering Guide ... 25

REVISION HISTORY

10/2019—Rev. C to Rev. D

Changes to Table 4 ... 7

9/2012—Rev. B to Rev. C

Changes to CMRR, Voltage Offset, Input Offset Current, and Gain Error Parameters, Table 2 ... 3
Changes to CMRR, Voltage Offset, and Input Offset Current Parameters, Table 2 ... 5

3/2011—Rev. A to Rev. B

Added AD8235/AD8236 to Table 1 ... 1
Changes to Endnote 1, Table 2 ... 4
Change Endnote 2 Placement in Total Noise Equation, Table 3 ... 5
Added G > 1 BRZ, BRMZ Max Parameter ... 6
Changes to Endnote 1, Table 3 ... 6
Changes to Figure 18 ... 11
Changes to Figure 37 ... 14
Changes to Figure 42 ... 15
Updated Outline Dimensions ... 25

7/2009—Rev. 0 to Rev. A

Added BRZ and BRM Models ... Universal
Changes to Features Section ... 1
Changes to Table 1 ... 1
Changes to General Description Section ... 1
Changes to Gain vs. Temperature Parameter, Output Parameter, and Operating Range Parameter, Table 2 ... 4
Changes to Common-Mode Rejection Ratio (CMRR) Parameter and to Input Offset, V_{OSO}, Average Temperature Coefficient Parameter, Table 3 ... 5
Changes to Gain vs. Temperature Parameter, Table 3 ... 6
Changes to Gain Selection Section ... 19
Changes to Reference Terminal Section and Input Voltage Range Section ... 20
Changes to Ordering Guide ... 25

1/2009—Revision 0: Initial Version

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SPECIFICATIONS

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 2.

Parameter	Conditions	ARZ, ARMZ Min	ARZ, ARMZ Typ	ARZ, ARMZ Max	BRZ, BRMZ Min	BRZ, BRMZ Typ	BRZ, BRMZ Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = −10 V to +10 V							
CMRR, DC to 60 Hz								
G = 1		86			90			dB
G = 10		106			106			dB
G = 100		120			120			dB
G = 1000		120			120			dB
CMRR at 5 kHz								
G = 1		80			80			dB
G = 10		90			90			dB
G = 100		90			90			dB
G = 1000		100			100			dB
NOISE	Total noise: $e_N = \sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Voltage Noise	1 kHz							
Input Voltage Noise, e_{NI}			22	24		22	24	nV/√Hz
Output Voltage Noise, e_{NO}			120	125		120	125	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2		µV p-p
G = 10			0.5			0.5		µV p-p
G = 100 to 1000			0.4			0.4		µV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	Total offset voltage: $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V			100			50	µV
Average Temperature Coefficient	T_A = −40°C to +125°C		0.5	2		0.5	1	µV/°C
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V			600			400	µV
Average Temperature Coefficient	T_A = −40°C to +125°C		2	10		1	5	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V							
G = 1		100			100			dB
G = 10		115			115			dB
G = 100		120			120			dB
G = 1000		120			120			dB
INPUT CURRENT								
Input Bias Current[1]	T_A = +25°C	5	20	27	5	20	27	nA
	T_A = +125°C	5	15	25	5	15	25	nA
	T_A = −40°C	5	30	35	5	30	35	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		70			70		pA/°C
Input Offset Current	T_A = +25°C			1			0.5	nA
	T_A = +125°C			1.5			0.5	nA
	T_A = −40°C			2			0.5	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		5			5		pA/°C
REFERENCE INPUT								
R_{IN}			100			100		kΩ
I_{IN}			7			7		µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%
DYNAMIC RESPONSE								
Small-Signal −3 dB Bandwidth								
G = 1			1500			1500		kHz
G = 10			160			160		kHz
G = 100			20			20		kHz
G = 1000			2			2		kHz

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Parameter	Conditions	ARZ, ARMZ Min	ARZ, ARMZ Typ	ARZ, ARMZ Max	BRZ, BRMZ Min	BRZ, BRMZ Typ	BRZ, BRMZ Max	Unit
Settling Time 0.01%	10 V step							
G = 1			25			25		µs
G = 10			15			15		µs
G = 100			40			40		µs
G = 1000			350			350		µs
Slew Rate	G = 1		0.4			0.4		V/µs
	G = 5 to 100		0.6			0.6		V/µs
GAIN	G = 1 + (49.4 kΩ/R_G)							
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} ±10 V							
G = 1				0.015			0.01	%
G = 5 to 1000				0.15			0.1	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1 to 10	R_L ≥ 2 kΩ			10			10	ppm
G = 100	R_L ≥ 2 kΩ			75			75	ppm
G = 1000	R_L ≥ 2 kΩ			750			750	ppm
Gain vs. Temperature[2]								
G = 1	T_A = −40°C to +85°C			5			1	ppm/°C
	T_A = 85°C to 125°C			5			2	ppm/°C
G > 1	T_A = −40°C to +125°C			−100			−100	ppm/°C
INPUT	V_S = ±1.35 V to +36 V							
Input Impedance								
Differential			0.8||2			0.8||2		GΩ||pF
Common Mode			0.4||2			0.4||2		GΩ||pF
Input Operating Voltage Range[3]	T_A = +25°C	$-V_S$ − 0.1		$+V_S$ − 0.8	$-V_S$ − 0.1		$+V_S$ − 0.8	V
	T_A = +125°C	$-V_S$ − 0.05		$+V_S$ − 0.6	$-V_S$ − 0.05		$+V_S$ − 0.6	V
	T_A = −40°C	$-V_S$ − 0.15		$+V_S$ − 0.9	$-V_S$ − 0.15		$+V_S$ − 0.9	V
Input Overvoltage Range	T_A = −40°C to +125°C	$+V_S$ − 40		$-V_S$ + 40	$+V_S$ − 40		$-V_S$ + 40	V
OUTPUT								
Output Swing								
R_L = 2 kΩ to Ground								
	T_A = +25°C	$-V_S$ + 0.4		$+V_S$ − 0.7	$-V_S$ + 0.4		$+V_S$ − 0.7	V
	T_A = +125°C	$-V_S$ + 0.4		$+V_S$ − 1.0	$-V_S$ + 0.4		$+V_S$ − 1.0	V
	T_A = −40°C	$-V_S$ + 1.2		$+V_S$ − 1.1	$-V_S$ + 1.2		$+V_S$ − 1.1	V
R_L = 10 kΩ to Ground								
	T_A = +25°C	$-V_S$ + 0.2		$+V_S$ − 0.2	$-V_S$ + 0.2		$+V_S$ − 0.2	V
	T_A = +125°C	$-V_S$ + 0.3		$+V_S$ − 0.3	$-V_S$ + 0.3		$+V_S$ − 0.3	V
	T_A = −40°C	$-V_S$ + 0.2		$+V_S$ − 0.2	$-V_S$ + 0.2		$+V_S$ − 0.2	V
R_L = 100 kΩ to Ground								
	T_A = −40°C to +125°C	$-V_S$ + 0.1		$+V_S$ − 0.1	$-V_S$ + 0.1		$+V_S$ − 0.1	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Dual-supply operation	±1.35		±18	±1.35		±18	V
Quiescent Current	T_A = +25°C		350	425		350	425	µA
	T_A = −40°C		250	325		250	325	µA
	T_A = +85°C		450	525		450	525	µA
	T_A = +125°C		525	600		525	600	µA
TEMPERATURE RANGE		−40		+125	−40		+125	°C

[1] The input stage uses pnp transistors; therefore, input bias current always flows out of the part.
[2] The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
[3] Input voltage range of the AD8226 input stage. The input range depends on the common-mode voltage, the differential voltage, the gain, and the reference voltage. See the Input Voltage Range section for more information.

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$+V_S$ = 2.7 V, $-V_S$ = 0 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 3.

Parameter	Conditions	ARZ, ARMZ Min	ARZ, ARMZ Typ	ARZ, ARMZ Max	BRZ, BRMZ Min	BRZ, BRMZ Typ	BRZ, BRMZ Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = 0 V to 1.7 V							
CMRR, DC to 60 Hz								
G = 1		86			90			dB
G = 10		106			106			dB
G = 100		120			120			dB
G = 1000		120			120			dB
CMRR at 5 kHz								
G = 1		80			80			dB
G = 10		90			90			dB
G = 100		90			90			dB
G = 1000		100			100			dB
NOISE	Total noise: $e_N = \sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Voltage Noise	1 kHz							
Input Voltage Noise, e_{NI}			22	24		22	24	nV/√Hz
Output Voltage Noise, e_{NO}			120	125		120	125	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			2.0			2.0		µV p-p
G = 10			0.5			0.5		µV p-p
G = 100 to 1000			0.4			0.4		µV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	Total offset voltage: $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}				100			50	µV
Average Temperature Coefficient	T_A = −40°C to +125°C		0.5	2		0.5	1	µV/°C
Output Offset, V_{OSO}				600			400	µV
Average Temperature Coefficient	T_A = −40°C to +125°C		2	10		1	5	µV/°C
Offset RTI vs. Supply (PSR)	V_S = 0 V to 1.7 V							
G = 1		100			100			dB
G = 10		115			115			dB
G = 100		120			120			dB
G = 1000		120			120			dB
INPUT CURRENT								
Input Bias Current[1]	T_A = +25°C	5	20	27	5	20	27	nA
	T_A = +125°C	5	15	25	5	15	25	nA
	T_A = −40°C	5	30	35	5	30	35	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		70			70		pA/°C
Input Offset Current	T_A = +25°C			1			0.5	nA
	T_A = +125°C			1.5			0.5	nA
	T_A = −40°C			1			0.1	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		5			5		pA/°C
REFERENCE INPUT								
R_{IN}			100			100		kΩ
I_{IN}			7			7		µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%
DYNAMIC RESPONSE								
Small-Signal −3 dB Bandwidth								
G = 1			1500			1500		kHz
G = 10			160			160		kHz
G = 100			20			20		kHz
G = 1000			2			2		kHz

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Parameter	Conditions	ARZ, ARMZ Min	ARZ, ARMZ Typ	ARZ, ARMZ Max	BRZ, BRMZ Min	BRZ, BRMZ Typ	BRZ, BRMZ Max	Unit
Settling Time 0.01%	2 V step							
G = 1			6			6		µs
G = 10			6			6		µs
G = 100			35			35		µs
G = 1000			350			350		µs
Slew Rate	G = 1		0.4			0.4		V/µs
	G = 5 to 100		0.6			0.6		V/µs
GAIN	G = 1 + (49.4 kΩ/R_G)							
Gain Range		1		1000	1		1000	V/V
Gain Error								
G = 1	V_{OUT} = 0.8 V to 1.8 V			0.04			0.01%	%
G = 5 to 1000	V_{OUT} = 0.2 V to 2.5 V			0.3			0.1%	%
Gain vs. Temperature[2]								
G = 1	T_A = −40°C to +85°C			5			1	ppm/°C
	T_A = +85°C to +125°C			5			2	ppm/°C
G > 1	T_A = −40°C to +125°C			−100			−100	ppm/°C
INPUT	$-V_S$ = 0 V, $+V_S$ = 2.7 V to 36 V							
Input Impedance								
Differential			0.8‖2			0.8‖2		GΩ‖pF
Common Mode			0.4‖2			0.4‖2		GΩ‖pF
Input Operating Voltage Range[3]	T_A = +25°C	−0.1		$+V_S$ − 0.7	−0.1		$+V_S$ − 0.7	V
	T_A = −40°C	−0.15		$+V_S$ − 0.9	−0.15		$+V_S$ − 0.9	V
	T_A = +125°C	−0.05		$+V_S$ − 0.6	−0.05		$+V_S$ − 0.6	V
Input Overvoltage Range	T_A = −40°C to +125°C	$+V_S$ − 40		$-V_S$ + 40	$+V_S$ − 40		$-V_S$ + 40	
OUTPUT								
Output Swing	R_L = 10 kΩ to 1.35 V, T_A = −40°C to +125°C	0.1		$+V_S$ − 0.1	0.1		$+V_S$ − 0.1	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Single-supply operation	2.2		36	2.2		36	V
Quiescent Current	T_A = +25°C, $-V_S$ = 0 V, $+V_S$ = 2.7 V		325	400		325	400	µA
	T_A = −40°C, $-V_S$ = 0 V, $+V_S$ = 2.7 V		250	325		250	325	µA
	T_A = +85°C, $-V_S$ = 0 V, $+V_S$ = 2.7 V		425	500		425	500	µA
	T_A = +125°C, $-V_S$ = 0 V, $+V_S$ = 2.7 V		475	550		475	550	µA
TEMPERATURE RANGE		−40		+125	−40		+125	°C

[1] Input stage uses pnp transistors; therefore, input bias current always flows out of the part.
[2] The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
[3] Input voltage range of the AD8226 input stage. The input range depends on the common-mode voltage, the differential voltage, the gain, and the reference voltage. See the Input Voltage Range section for more information.

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ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current	Indefinite
Maximum Voltage at −IN or +IN	$-V_S$ + 40 V
Minimum Voltage at −IN or +IN	$+V_S$ − 40 V
REF Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +125°C
Maximum Junction Temperature	140°C
ESD	
Human Body Model	1 kV
Charge Device Model	1.5 kV
Machine Model	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 5. Thermal Resistance

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	135	°C/W
8-Lead SOIC, 4-Layer JEDEC Board	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

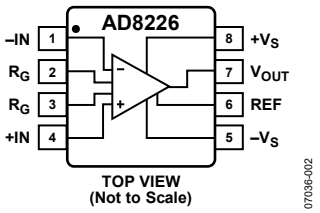

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input.
2, 3	R_G	Gain-Setting Pins. Place a gain resistor between these two pins.
4	+IN	Positive Input.
5	$-V_S$	Negative Supply.
6	REF	Reference. This pin must be driven by low impedance.
7	V_{OUT}	Output.
8	$+V_S$	Positive Supply.

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TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, V_S = ±15 V, R_L = 10 kΩ, unless otherwise noted.

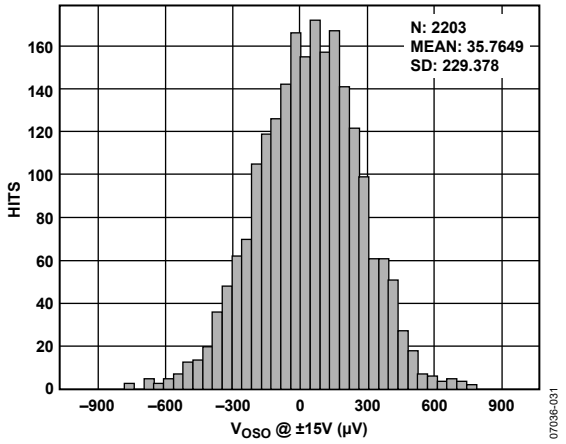

Figure 3. Typical Distribution of Output Offset Voltage

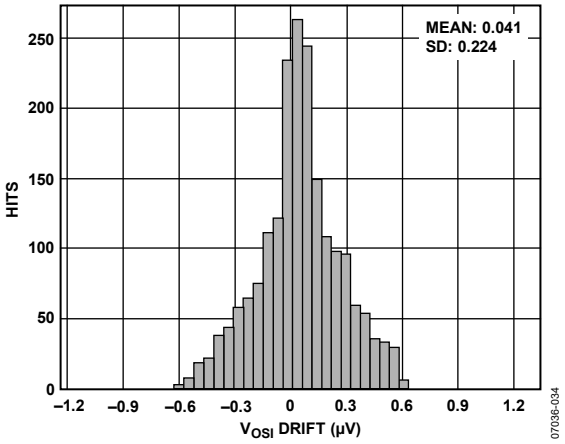

Figure 6. Typical Distribution of Input Offset Voltage Drift, G = 100

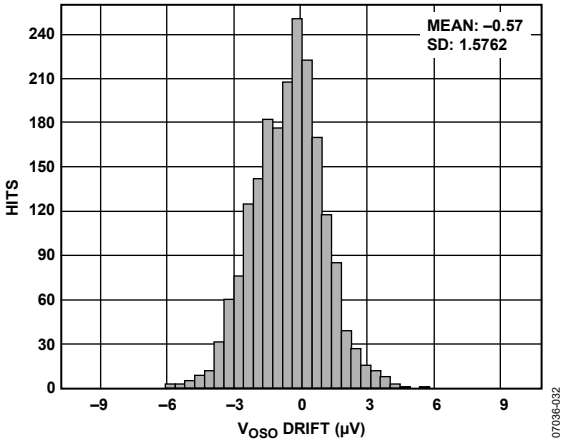

Figure 4. Typical Distribution of Output Offset Voltage Drift

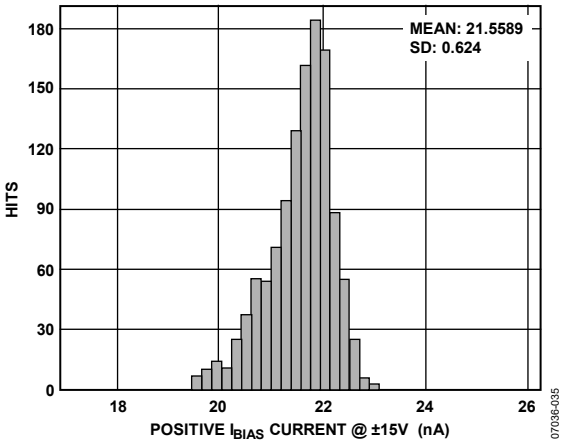

Figure 7. Typical Distribution of Input Bias Current

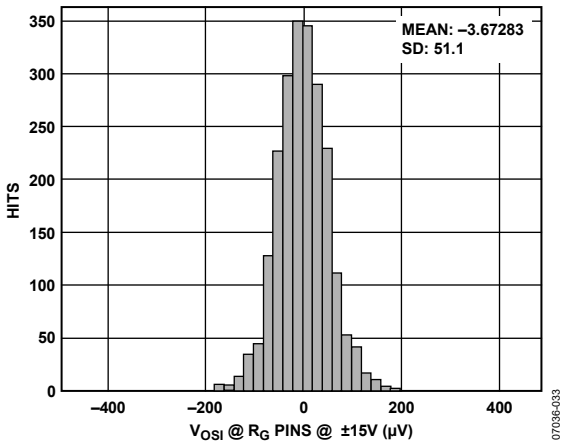

Figure 5. Typical Distribution of Input Offset Voltage

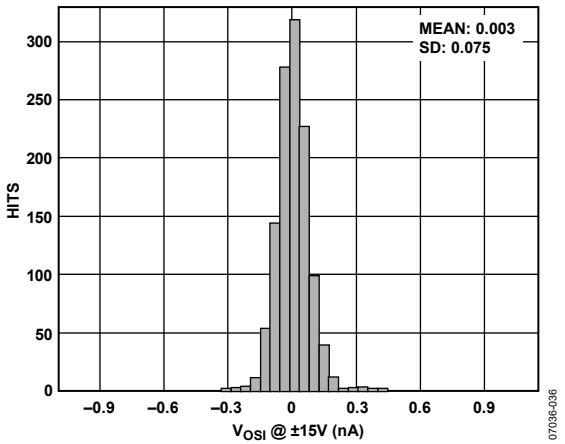

Figure 8. Typical Distribution of Input Offset Current

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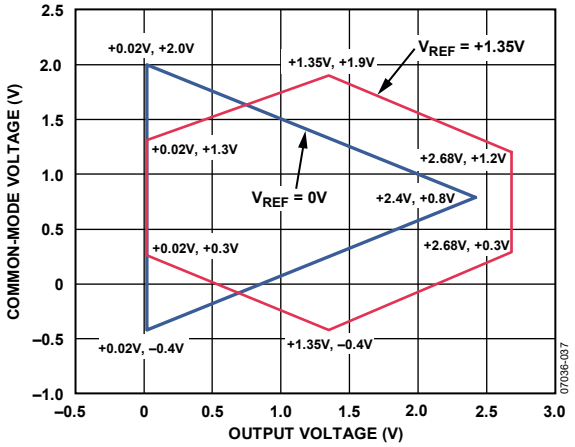

Figure 9. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = +2.7 V, G = 1

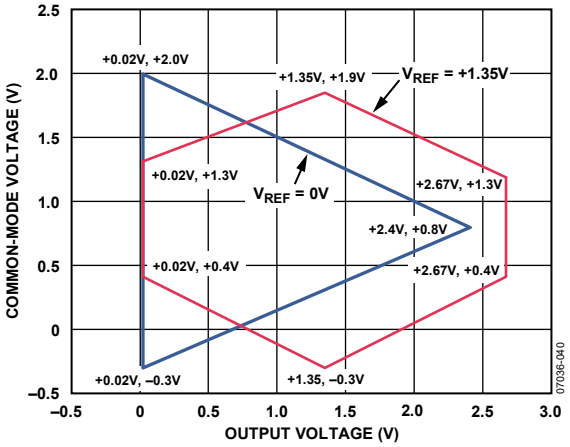

Figure 12. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = +2.7 V, G = 100

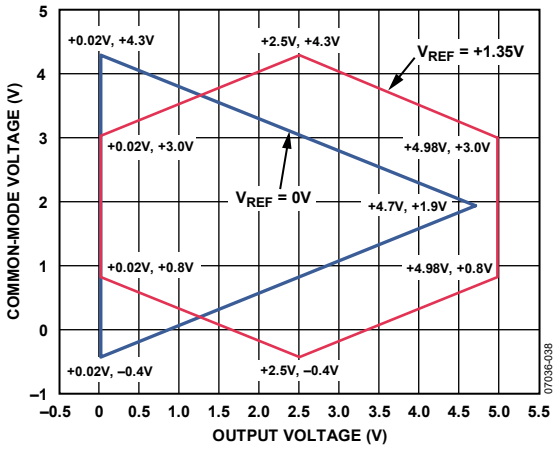

Figure 10. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = +5 V, G = 1

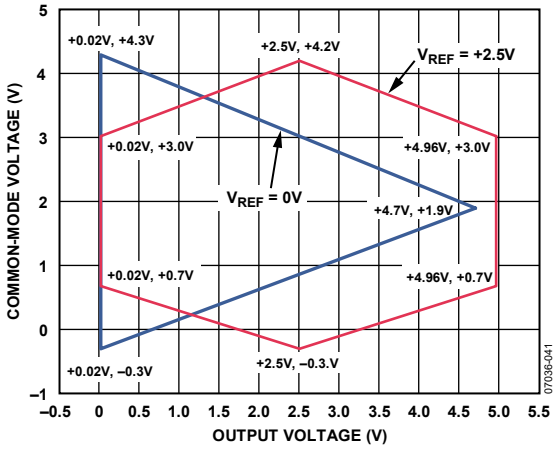

Figure 13. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = +5 V, G = 100

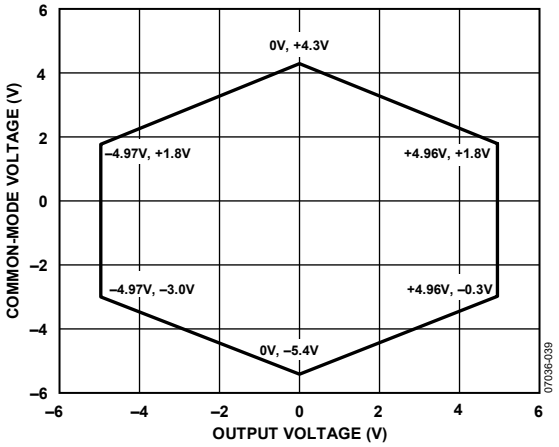

Figure 11. Input Common-Mode Voltage vs. Output Voltage, Dual Supplies, V_S = ±5 V, G = 1

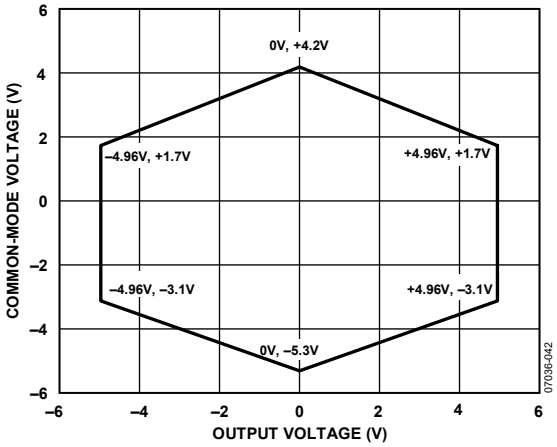

Figure 14. Input Common-Mode Voltage vs. Output Voltage, Dual Supplies, V_S = ±5 V, G = 100

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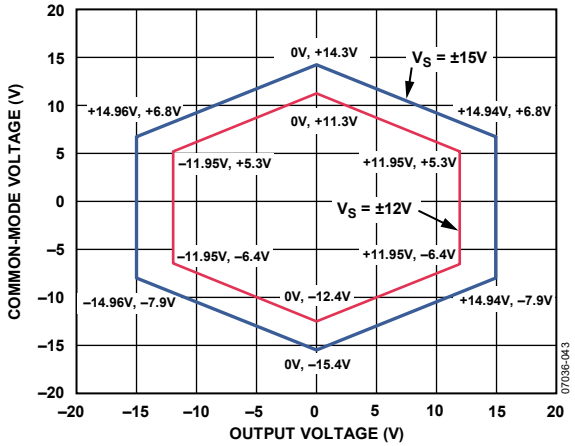

Figure 15. Input Common-Mode Voltage vs. Output Voltage, Dual Supplies, V_S = ±15 V, G = 1

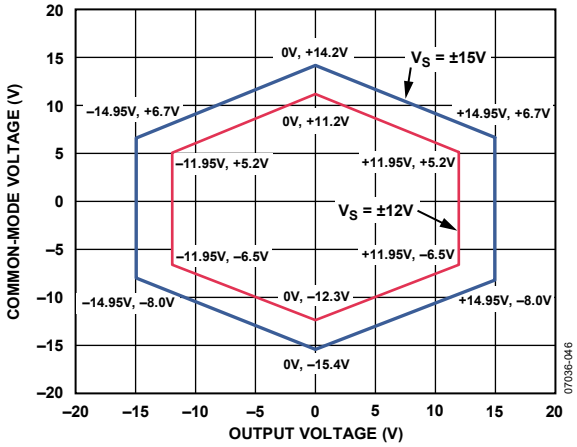

Figure 18. Input Common-Mode Voltage vs. Output Voltage, Dual Supplies, V_S = ±15 V, G = 100

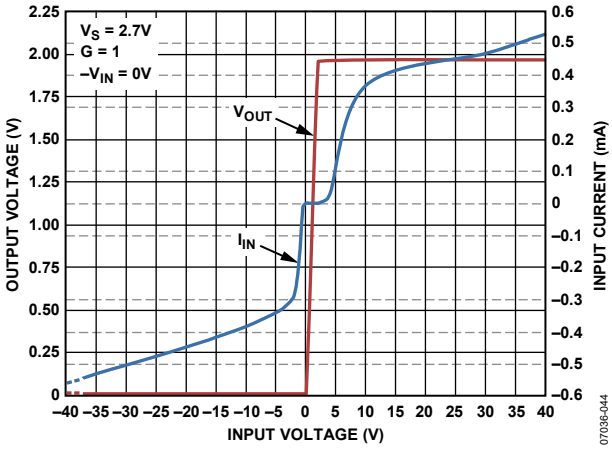

Figure 16. Input Overvoltage Performance, G = 1, V_S = 2.7 V

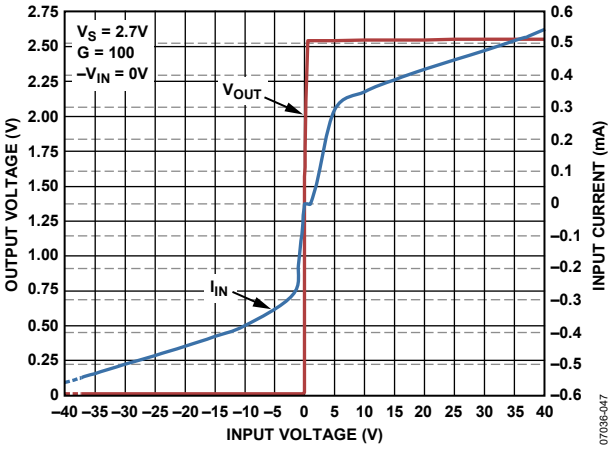

Figure 19. Input Overvoltage Performance, G = 100, V_S = 2.7 V

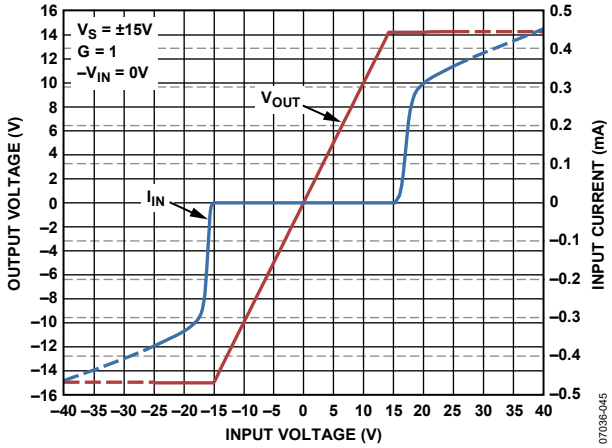

Figure 17. Input Overvoltage Performance, G = 1, V_S = ±15 V

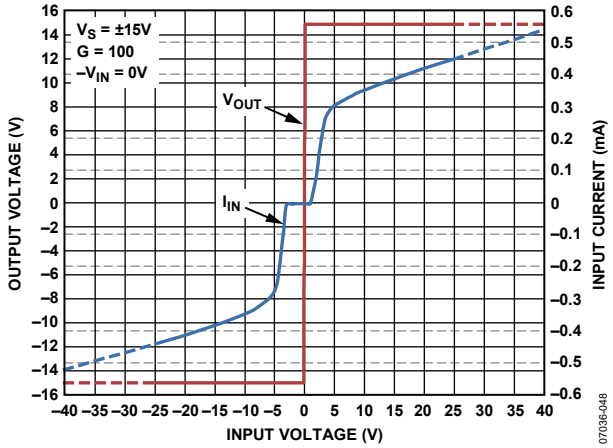

Figure 20. Input Overvoltage Performance, G = 100, V_S = ±15 V

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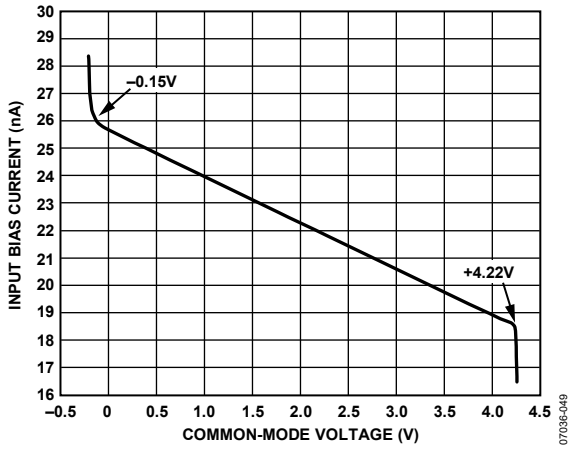

Figure 21. Input Bias Current vs. Common-Mode Voltage, V_S = +5 V

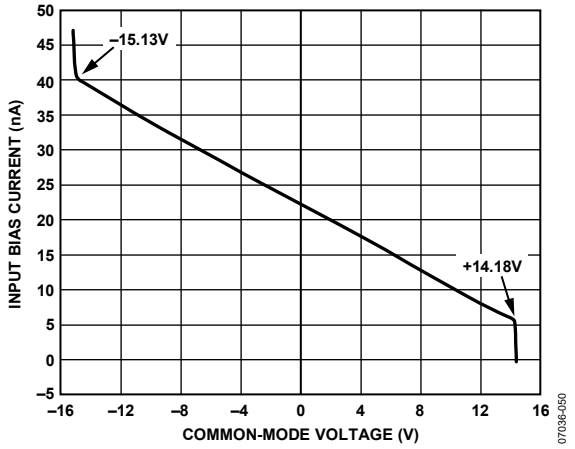

Figure 22. Input Bias Current vs. Common-Mode Voltage, V_S = ±15 V

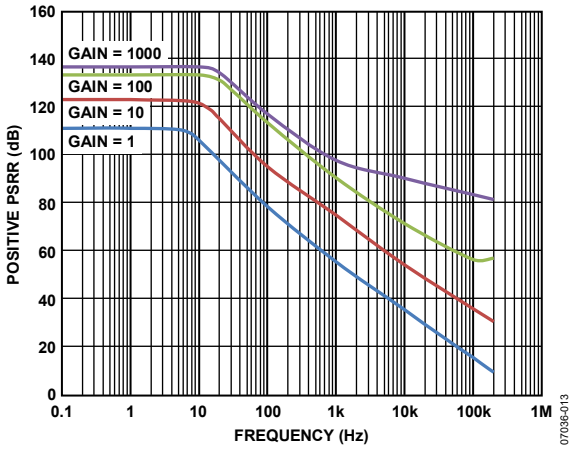

Figure 23. Positive PSRR vs. Frequency, RTI

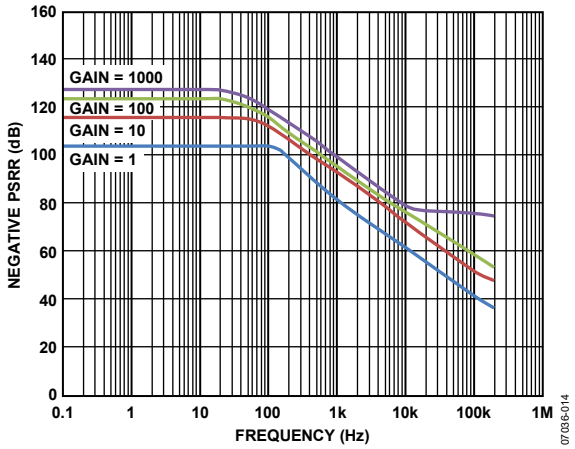

Figure 24. Negative PSRR vs. Frequency

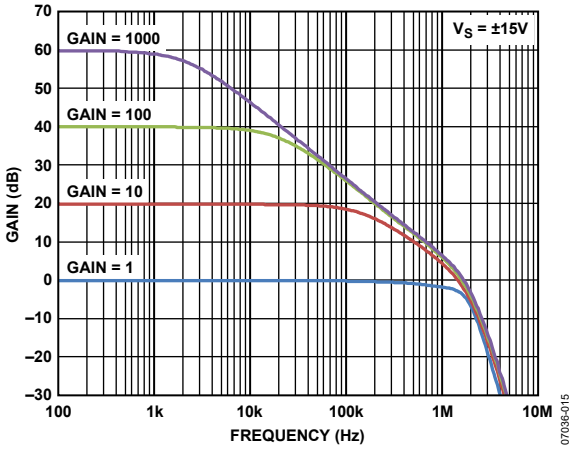

Figure 25. Gain vs. Frequency, V_S = ±15 V

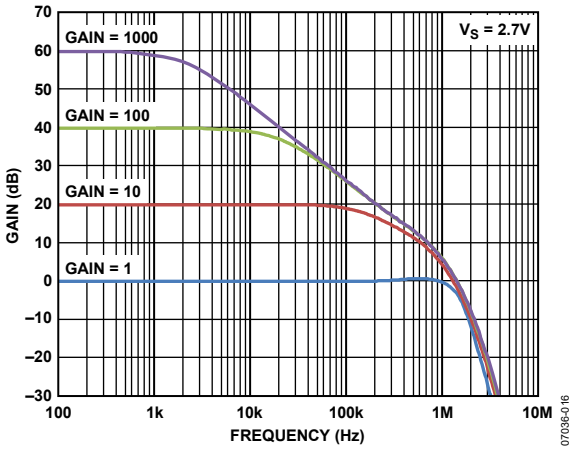

Figure 26. Gain vs. Frequency, 2.7 V Single Supply

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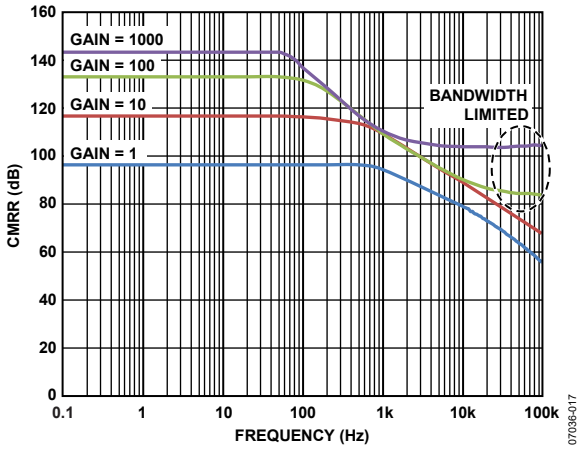

Figure 27. CMRR vs. Frequency, RTI

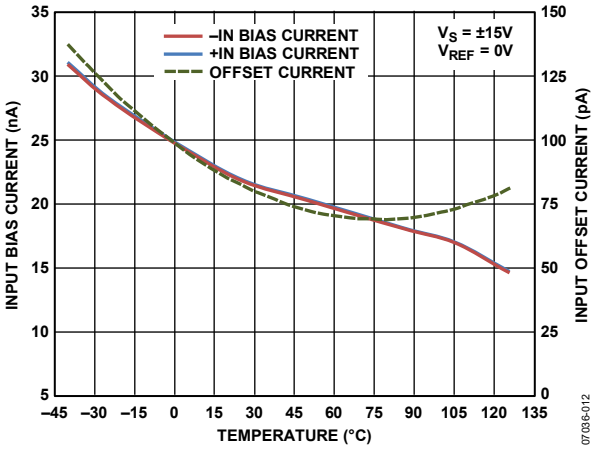

Figure 30. Input Bias Current and Input Offset Current vs. Temperature

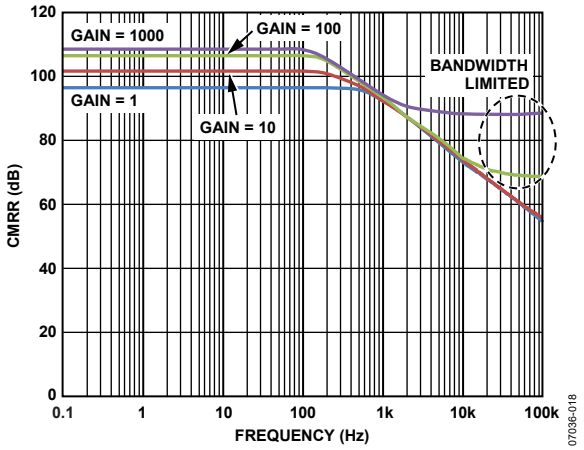

Figure 28. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance

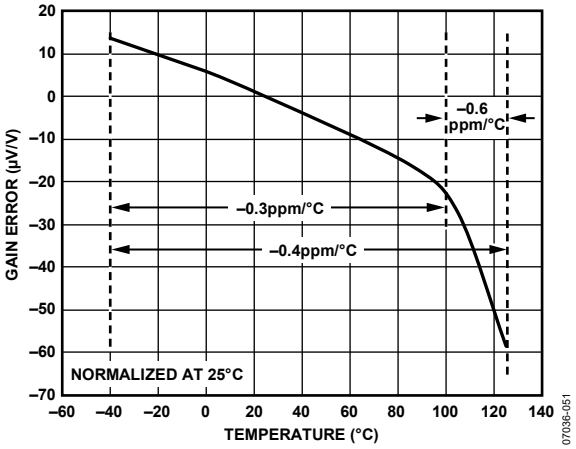

Figure 31. Gain Error vs. Temperature, G = 1

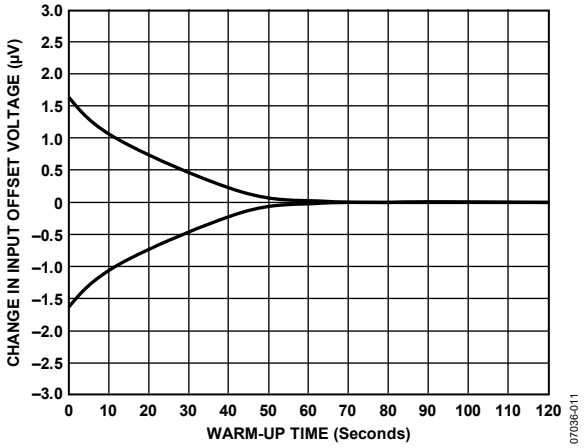

Figure 29. Change in Input Offset Voltage vs. Warm-Up Time

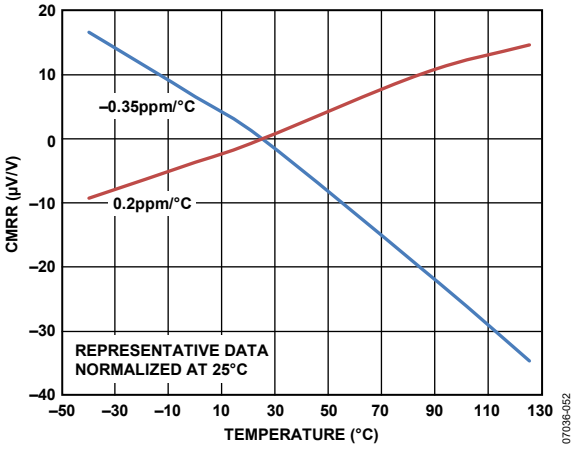

Figure 32. CMRR vs. Temperature, G = 1

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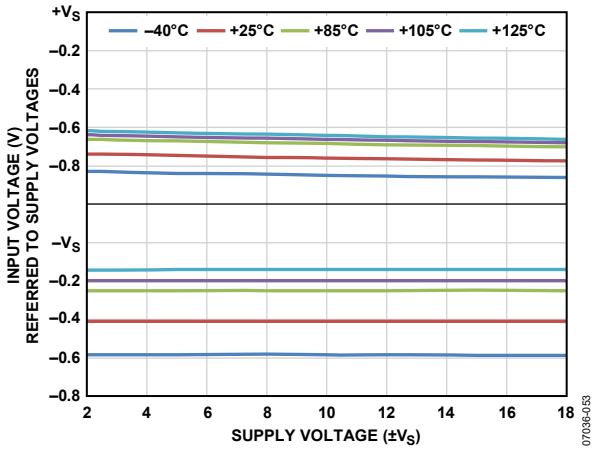

Figure 33. Input Voltage Limit vs. Supply Voltage

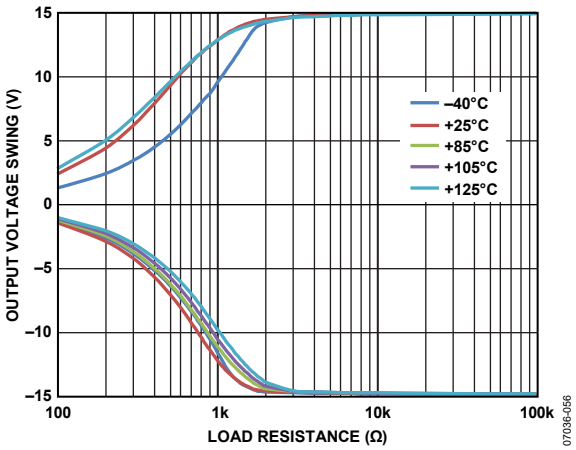

Figure 36. Output Voltage Swing vs. Load Resistance

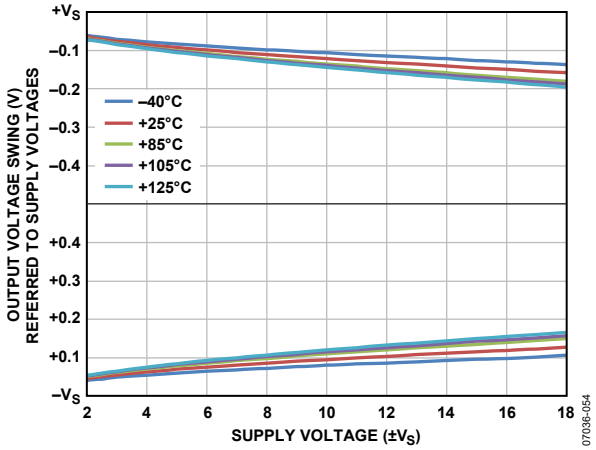

Figure 34. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

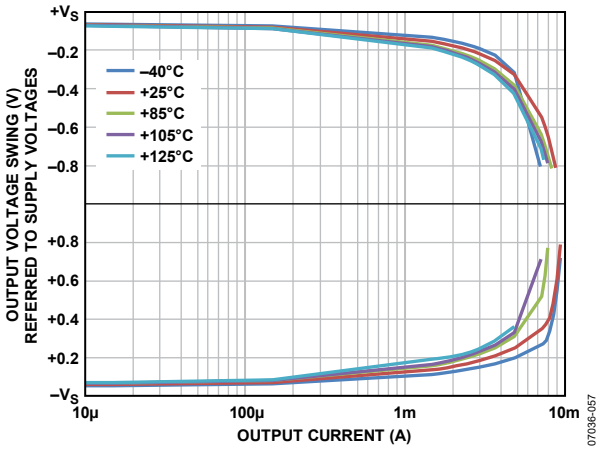

Figure 37. Output Voltage Swing vs. Output Current, G = 1

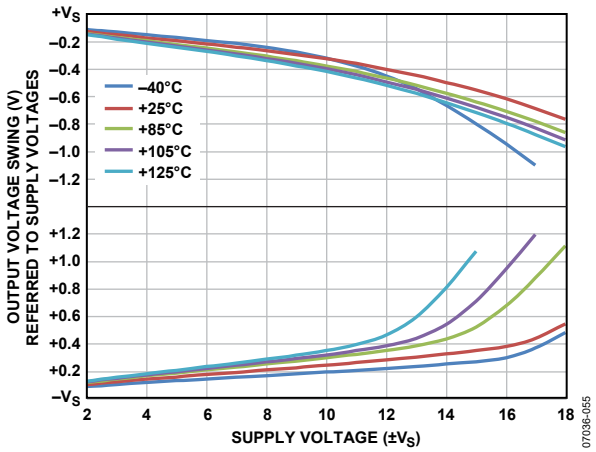

Figure 35. Output Voltage Swing vs. Supply Voltage, R_L = 2 kΩ

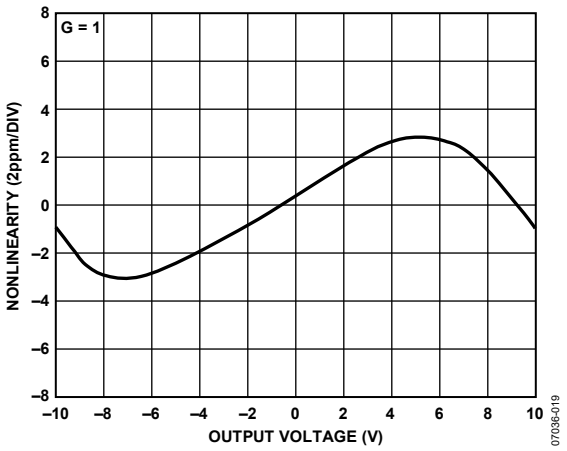

Figure 38. Gain Nonlinearity, G = 1, $R_L \geq$ 2 kΩ

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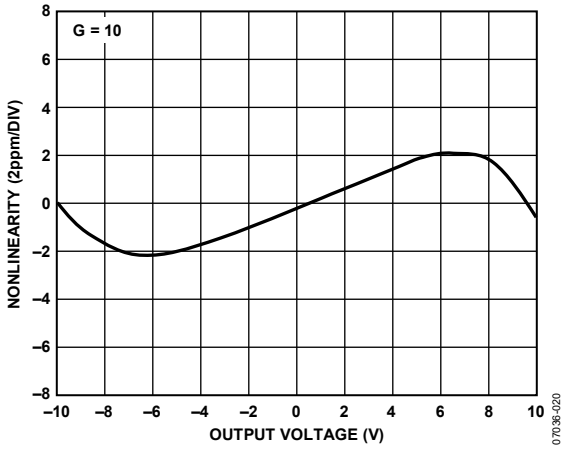

Figure 39. Gain Nonlinearity, G = 10, $R_L \geq 2$ kΩ

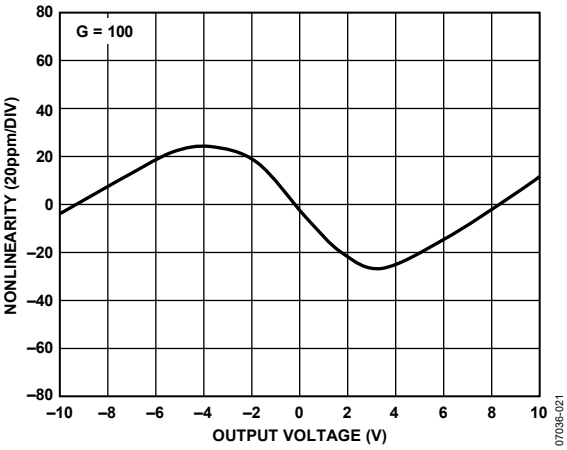

Figure 40. Gain Nonlinearity, G = 100, $R_L \geq 2$ kΩ

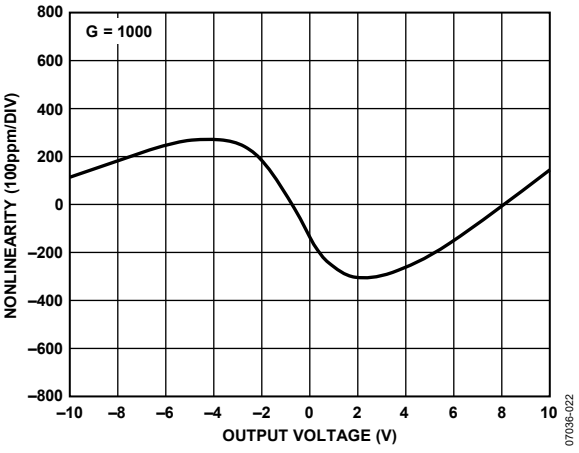

Figure 41. Gain Nonlinearity, G = 1000, $R_L \geq 2$ kΩ

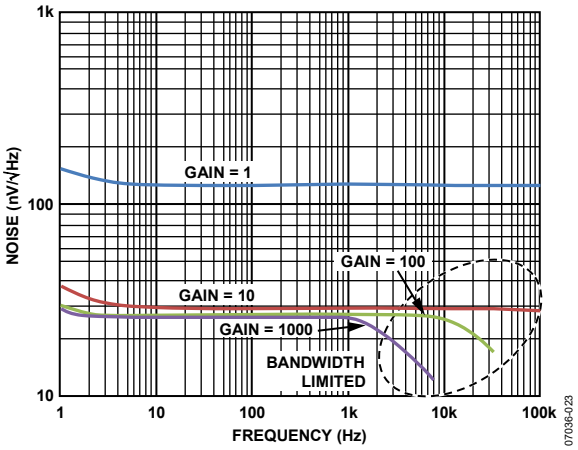

Figure 42. Voltage Noise Spectral Density vs. Frequency

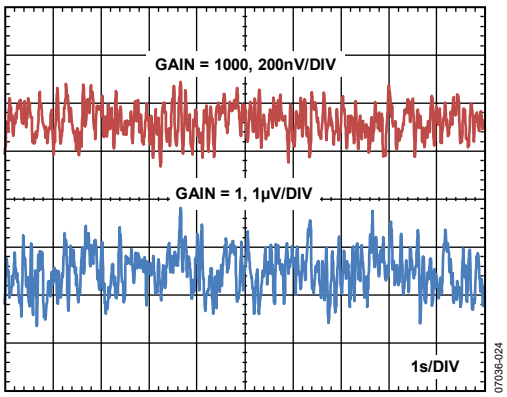

Figure 43. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1, G = 1000

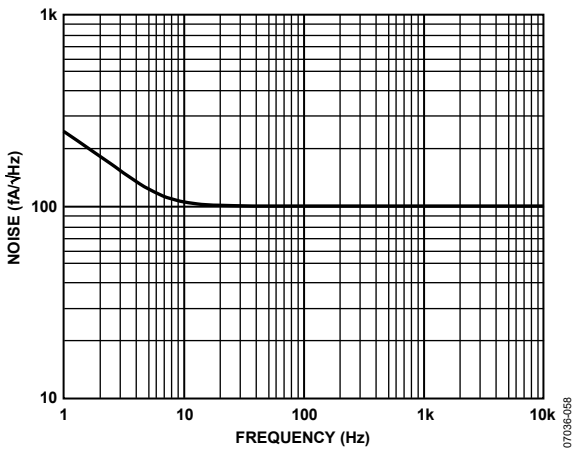

Figure 44. Current Noise Spectral Density vs. Frequency

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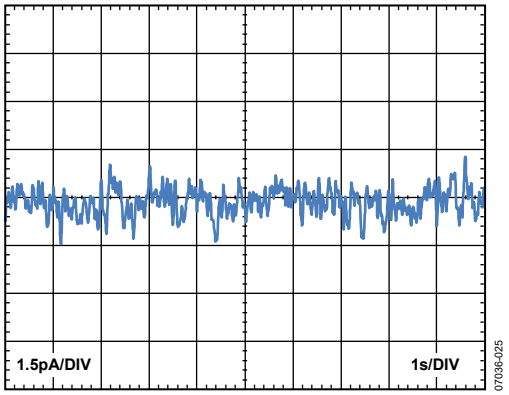

Figure 45. 0.1 Hz to 10 Hz Current Noise

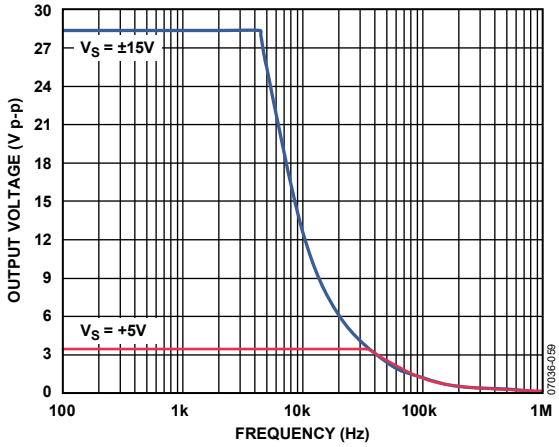

Figure 46. Large-Signal Frequency Response

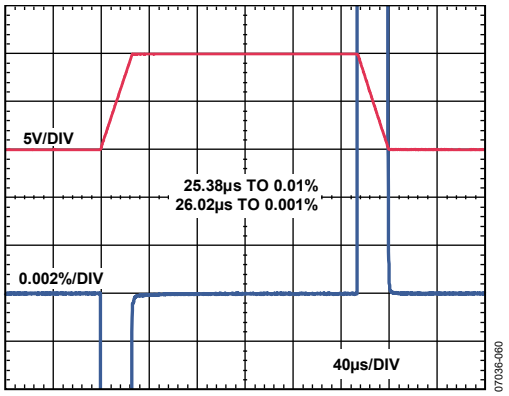

Figure 47. Large-Signal Pulse Response and Settling Time, $G = 1$, 10 V Step, $V_S = \pm 15$ V

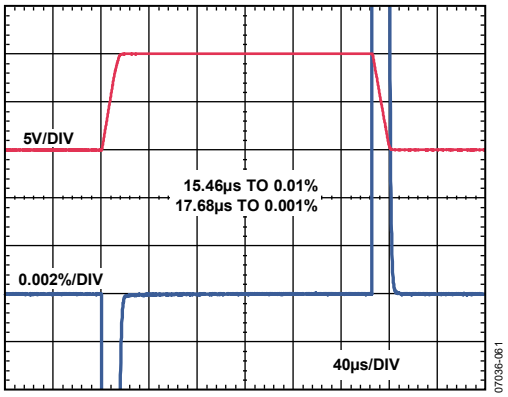

Figure 48. Large-Signal Pulse Response and Settling Time, $G = 10$, 10 V Step, $V_S = \pm 15$ V

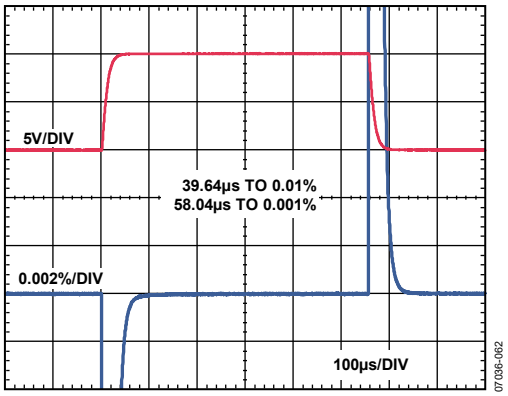

Figure 49. Large-Signal Pulse Response and Settling Time, $G = 100$, 10 V Step, $V_S = \pm 15$ V

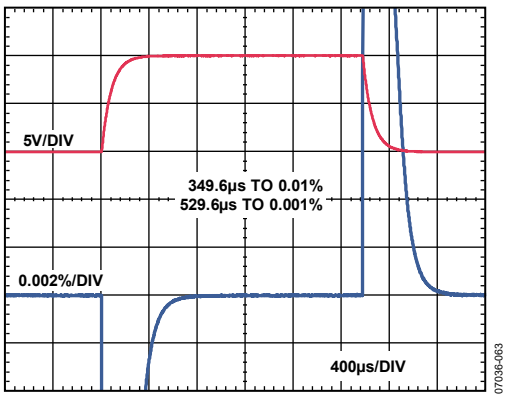

Figure 50. Large-Signal Pulse Response and Settling Time, $G = 1000$, 10 V Step, $V_S = \pm 15$ V

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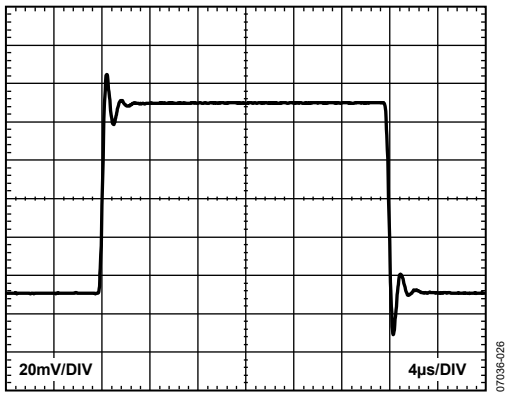

Figure 51. Small-Signal Response, G = 1, R_L = 10 kΩ, C_L = 100 pF

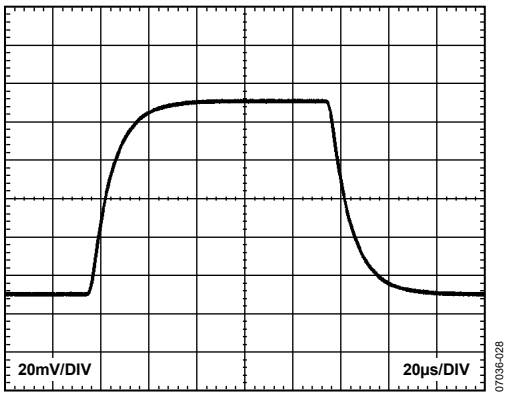

Figure 53. Small-Signal Response, G = 100, R_L = 10 kΩ, C_L = 100 pF

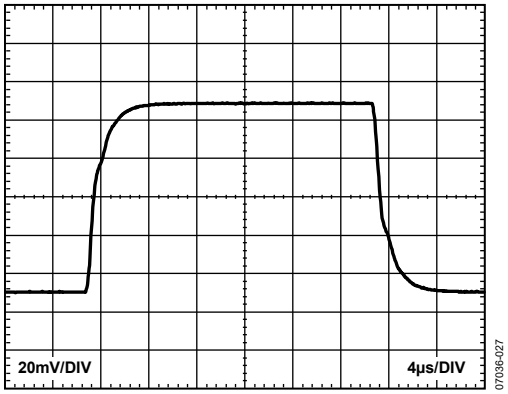

Figure 52. Small-Signal Response, G = 10, R_L = 10 kΩ, C_L = 100 pF

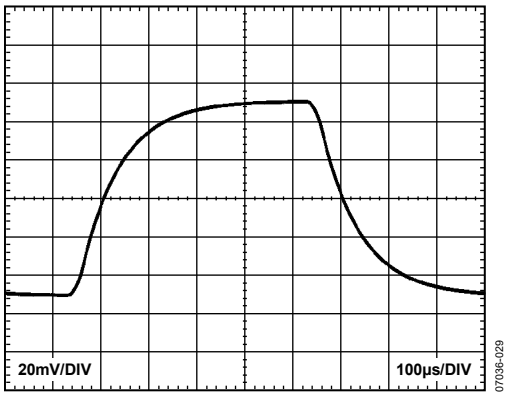

Figure 54. Small-Signal Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF

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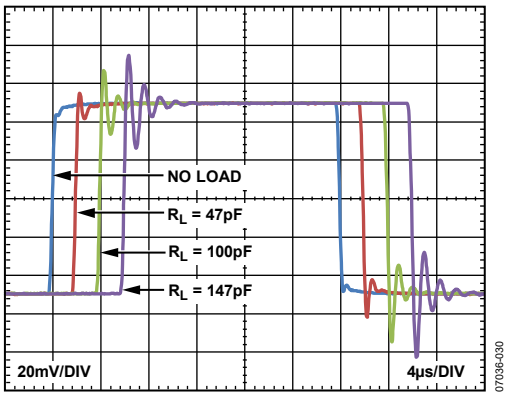

Figure 55. Small-Signal Response with Various Capacitive Loads, $G = 1$, $R_L = \infty$

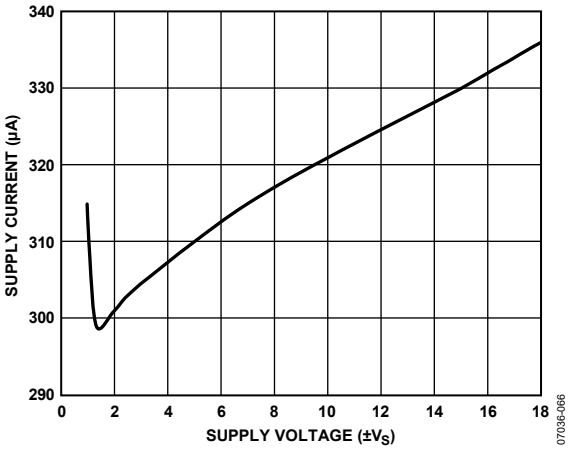

Figure 57. Supply Current vs. Supply Voltage

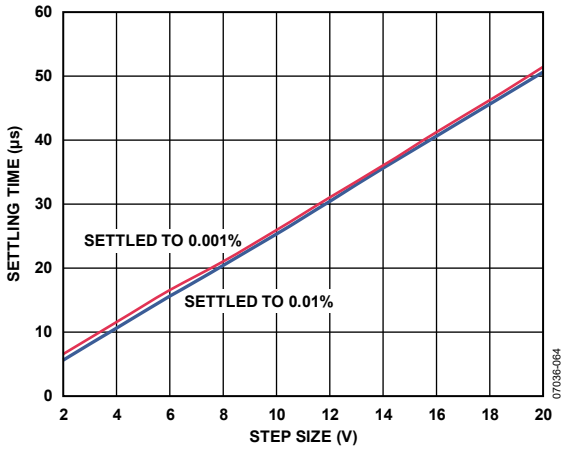

Figure 56. Settling Time vs. Step Size, $V_S = \pm 15$ V Dual Supplies

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THEORY OF OPERATION

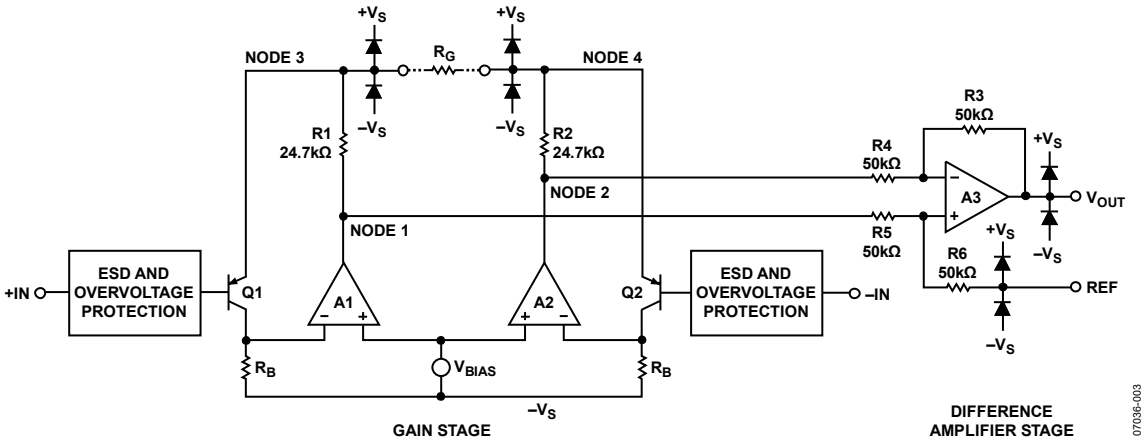

Figure 58. Simplified Schematic

ARCHITECTURE

The AD8226 is based on the classic 3-op-amp topology. This topology has two stages: a preamplifier to provide differential amplification, followed by a difference amplifier to remove the common-mode voltage. Figure 58 shows a simplified schematic of the AD8226.

The first stage works as follows: in order to maintain a constant voltage across the bias resistor R_B, A1 must keep Node 3 a constant diode drop above the positive input voltage. Similarly, A2 keeps Node 4 at a constant diode drop above the negative input voltage. Therefore, a replica of the differential input voltage is placed across the gain-setting resistor, R_G. The current that flows across this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs. Note that, in addition to a gained differential signal, the original common-mode signal, shifted a diode drop up, is also still present.

The second stage is a difference amplifier, composed of A3 and four 50 kΩ resistors. The purpose of this stage is to remove the common-mode signal from the amplified differential signal.

The transfer function of the AD8226 is

$$V_{OUT} = G(V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8226, which can be calculated by referring to Table 7 or by using the following gain equation:

$$R_G = \frac{49.4\ \text{k}\Omega}{G - 1}$$

Table 7. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

The AD8226 defaults to G = 1 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the AD8226 specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

If a gain of 5 is required and minimal gain drift is important, consider using the AD8227. The AD8227 has a default gain of 5 that is set with internal resistors. Because all resistors are internal, the gain drift is extremely low (<5 ppm/°C maximum).

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REFERENCE TERMINAL

The output voltage of the AD8226 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8226 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For the best performance, source impedance to the REF terminal should be kept below 2 Ω. As shown in Figure 59, the reference terminal, REF, is at one end of a 50 kΩ resistor. Additional impedance at the REF terminal adds to this 50 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be computed by $2(50\ k\Omega + R_{REF})/(100\ k\Omega + R_{REF})$.

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

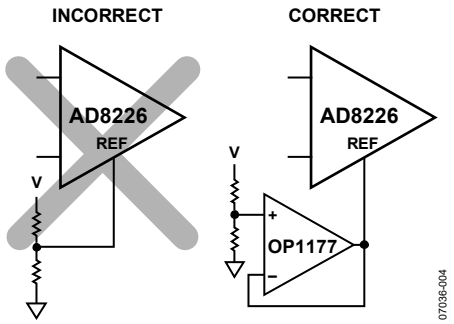

Figure 59. Driving the Reference Pin

INPUT VOLTAGE RANGE

Figure 9 through Figure 15 and Figure 18 show the allowable common-mode input voltage ranges for various output voltages and supply voltages. The 3-op-amp architecture of the AD8226 applies gain in the first stage before removing common-mode voltage with the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 58) experience a combination of a gained signal, a common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited.

For most applications, Figure 9 through Figure 15 and Figure 18 provide sufficient information to achieve a good design. For applications where a more detailed understanding is needed, Equation 1 to Equation 3 can be used to understand how the gain (G), common-mode input voltage (V_{CM}), differential input voltage (V_{DIFF}), and reference voltage (V_{REF}) interact. The values for the constants, V_{-LIMIT}, V_{+LIMIT}, and V_{REF_LIMIT}, are shown in Table 8. These three formulas, along with the input and output range specifications in Table 2 and Table 3, set the operating boundaries of the part.

$$V_{CM} - \left|\frac{(V_{DIFF})(G)}{2}\right| > -V_S + V_{-LIMIT} \quad (1)$$

$$V_{CM} + \left|\frac{(V_{DIFF})(G)}{2}\right| < +V_S - V_{+LIMIT} \quad (2)$$

$$\frac{\frac{(V_{DIFF})(G)}{2} + V_{CM} + V_{REF}}{2} < +V_S - V_{REF_LIMIT} \quad (3)$$

Table 8. Input Voltage Range Constants for Various Temperatures

Temperature	V_{-LIMIT}	V_{+LIMIT}	V_{REF_LIMIT}
−40°C	−0.55 V	0.8 V	1.3 V
+25°C	−0.35 V	0.7 V	1.15 V
+85°C	−0.15 V	0.65 V	1.05 V
+125°C	−0.05 V	0.6 V	0.9 V

Performance Across Temperature

The common-mode input range shifts upward with temperature. At cold temperatures, the part requires extra headroom from the positive supply, and operation near the negative supply has more margin. Conversely, hot temperatures require less headroom from the positive supply, but are the worst-case conditions for input voltages near the negative supply.

Recommendation for Best Performance

A typical part functions up to the boundaries described in this section. However, for best performance, designing with a few hundred millivolts extra margin is recommended. As signals approach the boundary, internal transistors begin to saturate, which can affect frequency and linearity performance.

If the application requirements exceed the boundaries, one solution is to apply less gain with the AD8226, and then apply additional gain later in the signal chain. Another option is to use the pin-compatible AD8227.

LAYOUT

To ensure optimum performance of the AD8226 at the PCB level, care must be taken in the design of the board layout. The AD8226 pins are arranged in a logical manner to aid in this task.

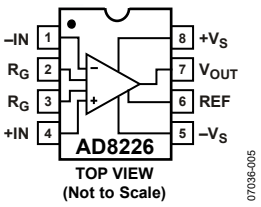

Figure 60. Pinout Diagram

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Common-Mode Rejection Ratio Over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR across frequency high, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. If the board design has a component at the gain-setting pins (for example, a switch or jumper), the part should be chosen so that the parasitic capacitance is as small as possible.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Note that noise on the supply pins can adversely affect performance. For more information, see the PSRR performance curves in Figure 23 and Figure 24.

A 0.1 µF capacitor should be placed as close as possible to each supply pin. As shown in Figure 61, a 10 µF tantalum capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.

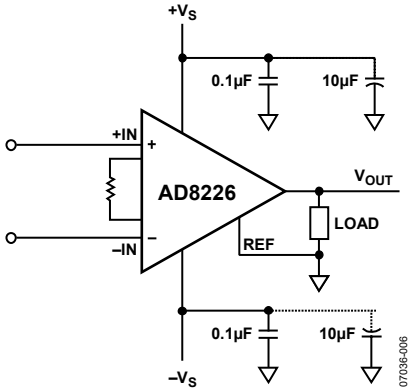

Figure 61. Supply Decoupling, REF, and Output Referred to Local Ground

References

The output voltage of the AD8226 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8226 must have a return path to ground. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 62.

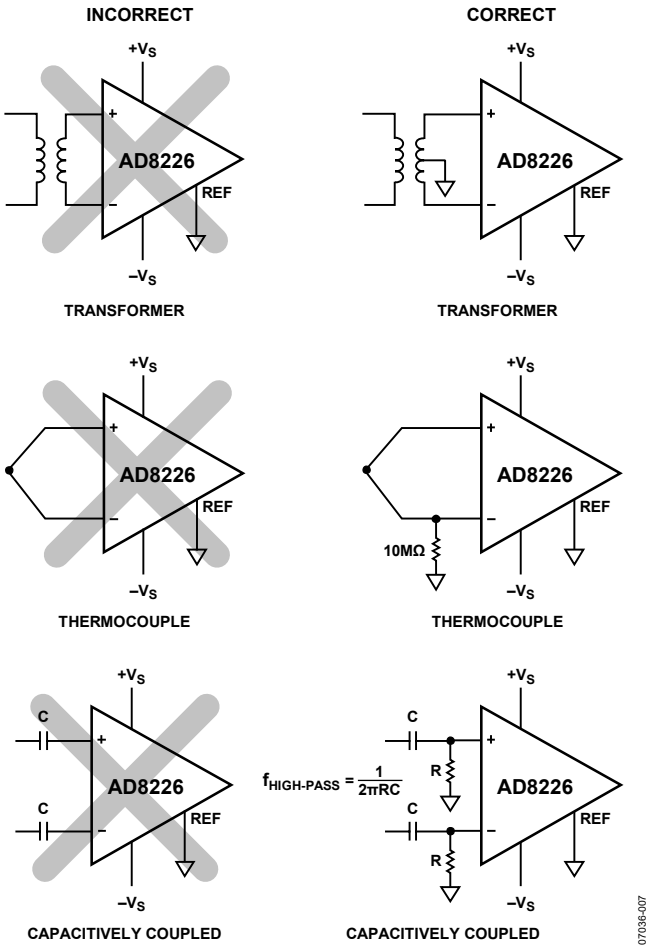

Figure 62. Creating an I_{BIAS} Path

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INPUT PROTECTION

The AD8226 has very robust inputs and typically does not need additional input protection. Input voltages can be up to 40 V from the opposite supply rail. For example, with a +5 V positive supply and a −8 V negative supply, the part can safely withstand voltages from −35 V to 32 V. Unlike some other instrumentation amplifiers, the part can handle large differential input voltages even when the part is in high gain. Figure 16, Figure 17, Figure 19, and Figure 20 show the behavior of the part under overvoltage conditions.

The rest of the AD8226 terminals should be kept within the supplies. All terminals of the AD8226 are protected against ESD.

For applications where the AD8226 encounters voltages beyond the allowed limits, external current-limiting resistors and low-leakage diode clamps such as the BAV199L, the FJH1100s, or the SP720 should be used.

RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications having strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 63. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

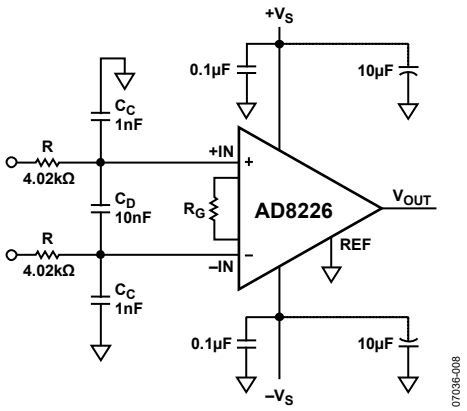

Figure 63. RFI Suppression

C_D affects the difference signal and C_C affects the common-mode signal. Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at the negative input degrades the CMRR of the AD8226. By using a value of C_D that is one magnitude larger than C_C, the effect of the mismatch is reduced and performance is improved.

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APPLICATIONS INFORMATION

DIFFERENTIAL DRIVE

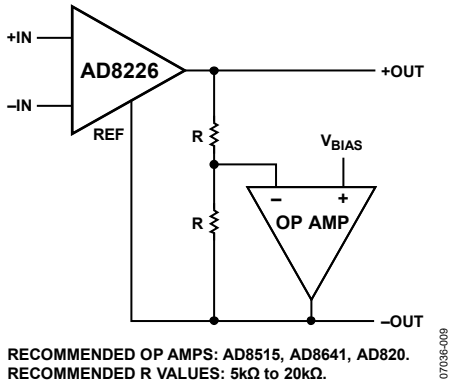

Figure 64. Differential Output Using an Op Amp

Figure 64 shows how to configure the AD8226 for differential output.

The differential output is set by the following equation:

$$V_{DIFF_OUT} = V_{OUT+} - V_{OUT-} = Gain \times (V_{IN+} - V_{IN-})$$

The common-mode output is set by the following equation:

$$V_{CM_OUT} = (V_{OUT+} - V_{OUT-})/2 = V_{BIAS}$$

The advantage of this circuit is that the dc differential accuracy depends on the AD8226, not on the op amp or the resistors. In addition, this circuit takes advantage of the precise control that the AD8226 has of its output voltage relative to the reference voltage. Although the dc performance and resistor matching of the op amp affect the dc common-mode output accuracy, such errors are likely to be rejected by the next device in the signal chain and therefore typically have little effect on overall system accuracy.

Tips for Best Differential Output Performance

For best ac performance, an op amp with at least a 2 MHz gain bandwidth and a 1 V/µs slew rate is recommended. Good choices for op amps are the AD8641, AD8515, and AD820.

Keep trace lengths from the resistors to the inverting terminal of the op amp as short as possible. Excessive capacitance at this node can cause the circuit to be unstable. If capacitance cannot be avoided, use lower value resistors.

For best linearity and ac performance, a minimum positive supply voltage ($+V_S$) is required. Table 9 shows the minimum supply voltage required for optimum performance. In this mode, V_{CM_MAX} indicates the maximum common-mode voltage expected at the input of the AD8226.

Table 9. Minimum Positive Supply Voltage

Temperature	Equation
Less than −10°C	$+V_S > (V_{CM_MAX} + V_{BIAS})/2 + 1.4$ V
−10°C to 25°C	$+V_S > (V_{CM_MAX} + V_{BIAS})/2 + 1.25$ V
More than 25°C	$+V_S > (V_{CM_MAX} + V_{BIAS})/2 + 1.1$ V

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PRECISION STRAIN GAGE

The low offset and high CMRR over frequency of the AD8226 make it an excellent candidate for performing bridge measurements. The bridge can be connected directly to the inputs of the amplifier (see Figure 65).

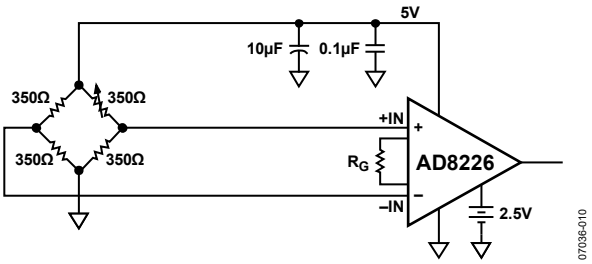

Figure 65. Precision Strain Gage

DRIVING AN ADC

Figure 66 shows several methods for driving an ADC. The ADuC7026 microcontroller was chosen for this example because it contains ADCs with an unbuffered, charge-sampling architecture that is typical of most modern ADCs. This type of architecture typically requires an RC buffer stage between the ADC and amplifier to work correctly.

Option 1 shows the minimum configuration required to drive a charge-sampling ADC. The capacitor provides charge to the ADC sampling capacitor while the resistor shields the AD8226 from the capacitance. To keep the AD8226 stable, the RC time constant of the resistor and capacitor needs to stay above 5 µs. This circuit is mainly useful for lower frequency signals.

Option 2 shows a circuit for driving higher speed signals. It uses a precision op amp (AD8616) with relatively high bandwidth and output drive. This amplifier can drive a resistor and capacitor with a much higher time constant and is therefore suited for higher frequency applications.

Option 3 is useful for applications where the AD8226 needs to run off a large voltage supply but drive a single-supply ADC. In normal operation, the AD8226 output stays within the ADC range, and the AD8616 simply buffers it. However, in a fault condition, the output of the AD8226 may go outside the supply range of both the AD8616 and the ADC. This is not an issue in the circuit, however, because the 10 kΩ resistor between the two amplifiers limits the current into the AD8616 to a safe level.

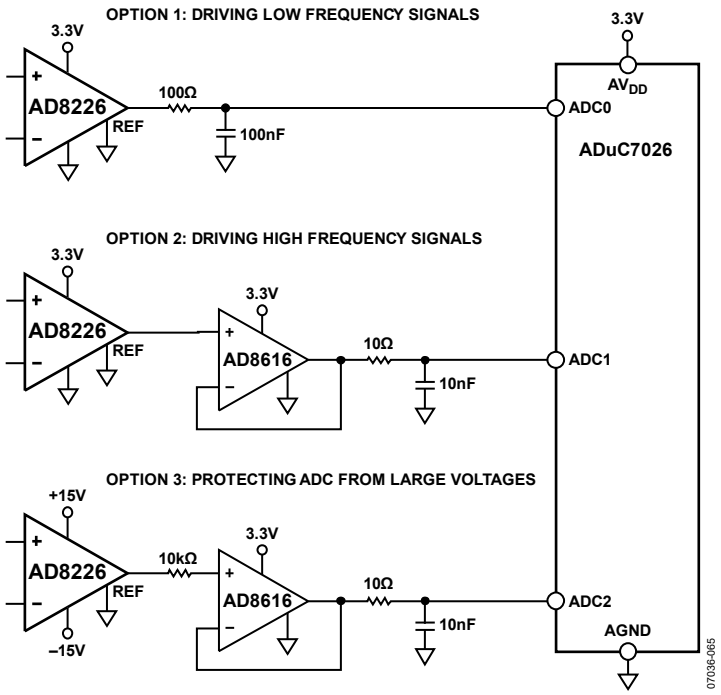

Figure 66. Driving an ADC

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OUTLINE DIMENSIONS

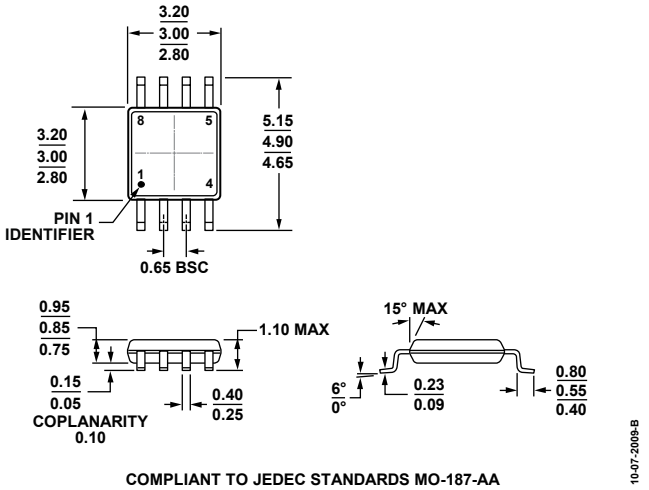

Figure 67. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

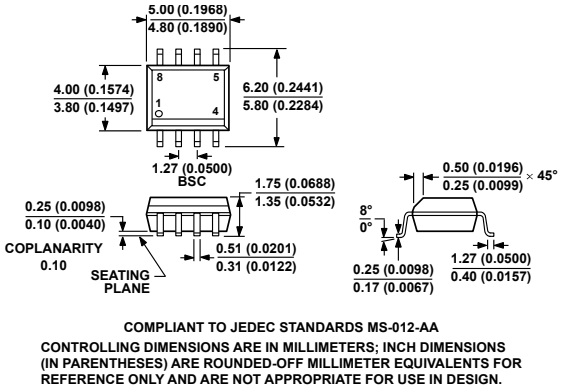

Figure 68. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
AD8226ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	Y18
AD8226ARMZ-RL	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y18
AD8226ARMZ-R7	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y18
AD8226ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8226ARZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8226ARZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8226BRMZ	−40°C to +125°C	8-Lead MSOP	RM-8	Y19
AD8226BRMZ-RL	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y19
AD8226BRMZ-R7	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y19
AD8226BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8226BRZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8226BRZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	

[1] Z = RoHS Compliant Part.

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