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AD7880–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V, f_{CLKIN} = 2.5 MHz, MODE = V_{DD} unless otherwise noted. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Versions[1]	C Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3] (SNR)	70	70	dB min	Typically SNR Is 72 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Total Harmonic Distortion (THD)	–80	–80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Peak Harmonic or Spurious Noise	–80	–80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 66 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	–80	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
Third Order Terms	–80	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
DC ACCURACY				
Resolution	12	12	Bits	All DC ACCURACY Specifications Apply for the Three Analog Input Ranges
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±15	±5	LSB max	
Bipolar Zero Error	±10	±5	LSB max	
Unipolar Offset Error	±5	±5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	See Figure 5
	0 to 2 V_{REF}	0 to 2 V_{REF}	Volts	See Figure 6
	±V_{REF}	±V_{REF}	Volts	See Figure 7
Input Resistance	10	10	MΩ min	0 to V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: 0 to 2 V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT				
V_{REF} (For Specified Performance)	5	5	V	±5%: Normally V_{REF} = V_{DD} (See Reference Input Section)
I_{REF}	1.5	1.5	mA max	
Nominal Reference Range	2.5/V_{DD}	2.5/V_{DD}	V min/max	See Figure 3 for Degradation in Performance Down to 2.5 V
LOGIC INPUTS				
$\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$, CLKIN				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
MODE INPUT				
Input High Voltage, V_{INH}	4	4	V min	
Input Low Voltage, V_{INL}	1	1	V max	
Input Current, I_{IN}	±125	±125	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
CONVERSION				
Conversion Time	12	12	µs max	f_{CLKIN} = 2.5 MHz
Track/Hold Acquisition Time	3	3	µs max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}				
Normal Power Mode @ +25°C	7.5	7.5	mA max	Typically 4 mA; MODE = V_{DD}
T_{MIN} to T_{MAX}	10	10	mA max	Typically 5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	750	750	µA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
T_{MIN} to T_{MAX}	1	1	mA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
Power Dissipation				
Normal Power Mode @ +25°C	37.5	37.5	mW max	V_{DD} = 5 V: Typically 20 mW; MODE = V_{DD}
T_{MIN} to T_{MAX}	50	50	mW max	V_{DD} = 5 V: Typically 25 mW; MODE = V_{DD}
Power Save Mode @ +25°C	3.75	3.75	mW max	V_{DD} = 5 V: Typically 2 mW; MODE = 0 V
T_{MIN} to T_{MAX}	5	5	mW max	V_{DD} = 5 V: Typically 2.5 mW; MODE = 0 V

NOTES

[1]Temperature ranges are as follows: B/C Versions, –40°C to +85°C.

[2]V_{IN} = 0 to V_{REF}

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

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TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	130	130	ns min	$\overline{CONVST}$ to $\overline{BUSY}$ Falling Edge
t_3	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_7[2]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_8[3]	**5**	**5**	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	

NOTES

[1]Timing specifications in **bold** print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_7 is measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_8 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

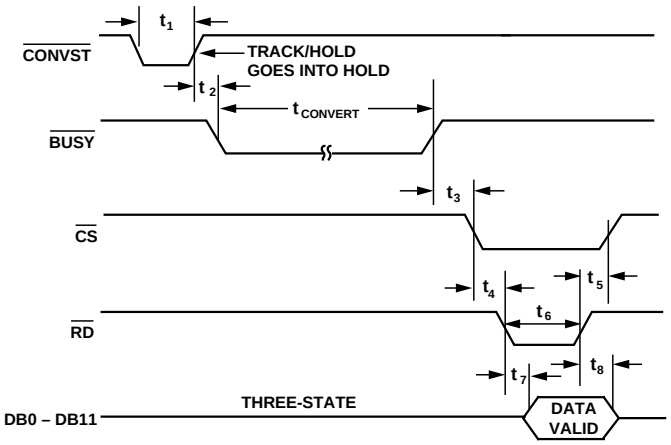

Figure 1. Timing Diagram

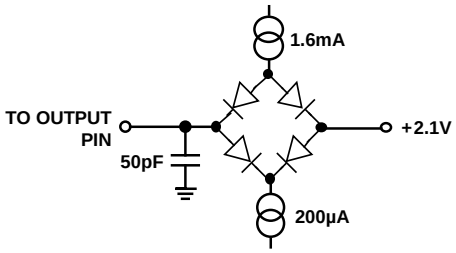

Figure 2. Load Circuit for Access and Relinquish Time

Table I. Truth Table

$\overline{CS}$	$\overline{CONVST}$	$\overline{RD}$	Function
1	1	X	Not Selected
1	j	1	Start Conversion g
0	1	0	Enable ADC Data
0	1	1	Data Bus Three Stated

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
AGND to DGND ..... –0.3 V to V_{DD} + 0.3 V
V_{INA}, V_{INB} to AGND (Figure 5) ..... –0.3 V to V_{DD} + 0.3 V
V_{INA} to AGND (Figure 6) ..... –0.6 V to 2 V_{DD} + 0.6 V
V_{INA} to AGND (Figure 7) ..... $-V_{DD}$ – 0.3 V to V_{DD} + 0.3 V
V_{REF} to AGND ..... 0.3 V to V_{DD}
Digital Inputs to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B, C Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above +75°C by ..... 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7880 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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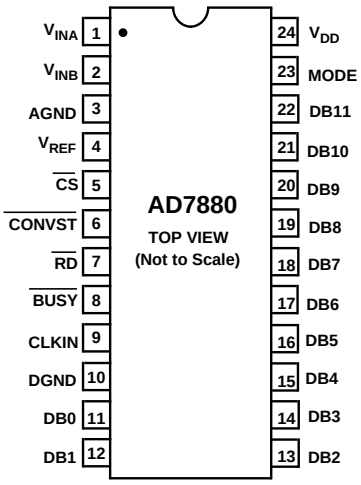
ORDERING GUIDE

Model	Temperature Range	Full-Scale Error (LSBs)	Bipolar Zero Error (LSBs)	Package Option*
AD7880BN	–40°C to +85°C	±15	±10	N-24
AD7880BQ	–40°C to +85°C	±15	±10	Q-24
AD7880CN	–40°C to +85°C	±5	±5	N-24
AD7880CQ	–40°C to +85°C	±5	±5	Q-24
AD7880BR	–40°C to +85°C	±15	±10	R-24
AD7880CR	–40°C to +85°C	±5	±5	R-24

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline Integrated Circuit).

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	V_{INA}	Analog Input.
2	V_{INB}	Analog Input.
3	AGND	Analog Ground.
4	V_{REF}	Voltage Reference Input. This is normally tied to V_{DD}.
5	$\overline{CS}$	Chip Select. Active Low Logic input. The device is selected when this input is active.
6	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into hold mode and starts conversion. This input is asynchronous to the CLKIN and is independent of $\overline{CS}$ and $\overline{RD}$.
7	$\overline{RD}$	Read. Active Low Logic Input. This input is used in conjunction with $\overline{CS}$ low to enable data outputs.
8	$\overline{BUSY}$	Active Low Logic Output. This status line indicates converter status. $\overline{BUSY}$ is low during conversion.
9	CLKIN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark/space ratio of the clock can vary from 40/60 to 60/40.
10	DGND	Digital Ground.
11 . . . 22	DB0–DB11	Three-State Data Outputs. These become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
23	MODE	MODE Input. This input is used to put the device into the power save mode (MODE = 0 V). During normal operation, the MODE input will be a logic high (MODE = V_{DD}).
24	V_{DD}	Power Supply. This is nominally +5 V.

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CIRCUIT INFORMATION

The AD7880 is a +5 V single supply 12-bit A/D converter. The part requires no external components apart from a 2.5 MHz external clock and power supply decoupling capacitors. It contains a 12-bit successive approximation ADC based on a fast-settling voltage-output DAC, a high speed comparator and SAR, as well as the necessary control logic. The charge balancing comparator used in the AD7880 provides the user with an inherent track-and-hold function. The ADC is specified to work with sampling rates up to 66 kHz.

CONVERTER DETAILS

The AD7880 conversion cycle is initiated on the rising edge of the CONVST pulse, as shown in the timing diagram of Figure 1. The rising edge of the $\overline{\text{CONVST}}$ pulse places the track/hold amplifier into "HOLD" mode. The conversion cycle then takes between 26 and 28 clock periods. The maximum specified conversion time is 12 µs. This corresponds to a conversion cycle time of 28 clock periods with a CLKIN frequency of 2.5 MHz and also includes internal propagation delays. During conversion the $\overline{\text{BUSY}}$ output will remain low, and the output databus drivers will be three-stated. When a conversion is completed, the $\overline{\text{BUSY}}$ output will go to a high level, and the result of the conversion can be read by bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low.

The track/hold amplifier acquires a 12-bit input signal in 3 µs. The overall throughput time for the AD7880 is equal to the conversion time plus the track/hold acquisition time. For a 2.5 MHz input clock the throughput time is 15 µs.

REFERENCE INPUT

For specified performance, it is recommended that the reference input be tied to V_{DD}. The part, however, will operate with a reference down to 2.5 V though with reduced performance specifications. Figure 3 shows a graph of signal-to-noise ratio (SNR) versus V_{REF}.

V_{REF} must not be allowed to go above V_{DD} by more than 100 mV.

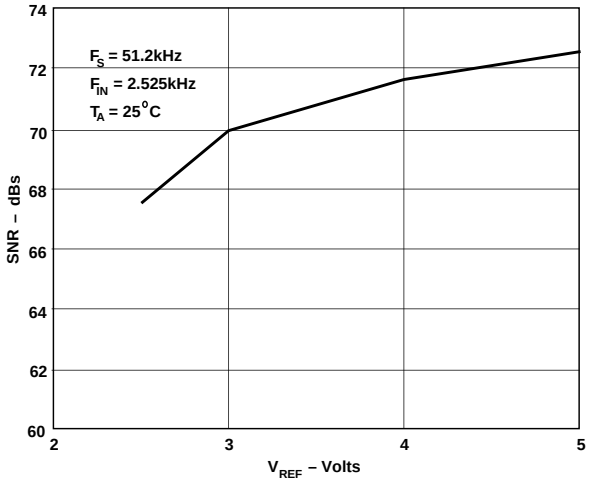

Figure 3. SNR vs. V_{REF}

ANALOG INPUT

The AD7880 has two analog input pins, V_{INA} and V_{INB}. Figure 4 shows the input circuitry to the ADC sampling comparator. The on-board attenuator network, made up of equal resistors, allows for various input ranges.

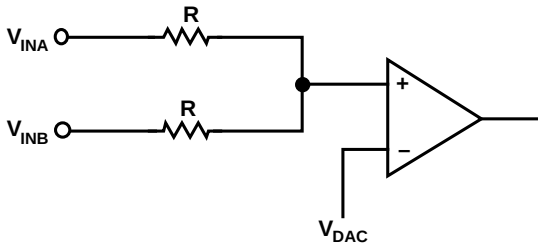

Figure 4. AD7880 Input Circuit

The AD7880 accommodates three separate input ranges, 0 to V_{REF}, 0 to 2 V_{REF} and ±V_{REF}. The input configurations corresponding to these ranges are shown in Figures 5, 6 and 7.

With $V_{REF} = V_{DD}$ and using a nominal V_{DD} of +5 V, the input ranges are 0 V to 5 V, 0 V to 10 V and +5 V, as shown in Table II.

Table II. Analog Input Ranges

Analog Input Range	V_{REF}	Input Connections		Connection Diagram
		V_{INA}	V_{INB}	
0 V to +5 V	V_{DD}	V_{IN}	V_{IN}	Figure 5
0 V to +10 V	V_{DD}	V_{IN}	AGND	Figure 6
±5 V	V_{DD}	V_{IN}	V_{REF}	Figure 7

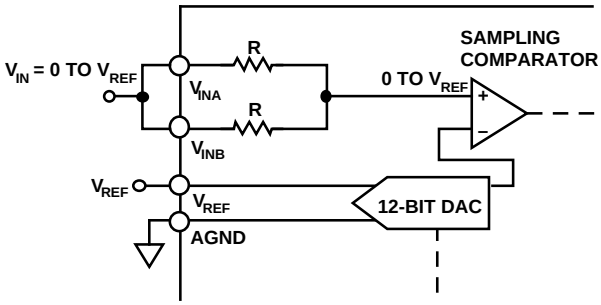

Figure 5. 0 to V_{REF} Unipolar Input Configuration

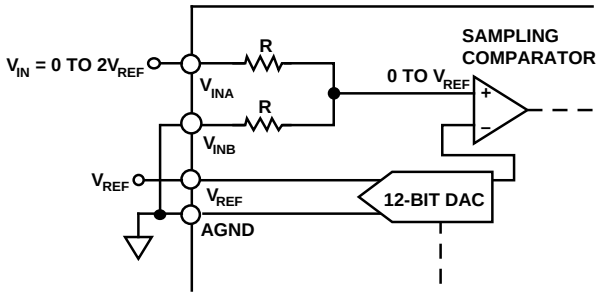

Figure 6. 0 to 2 V_{REF} Unipolar Input Configuration

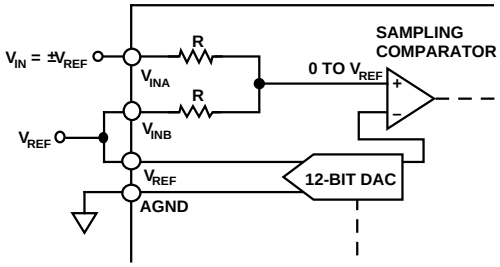

Figure 7. ±V_{REF} Bipolar Input Configuration

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The AD7880 has two unipolar input ranges, 0 V to 5 V and 0 V to 10 V. Figure 5 shows the analog input for the 0 V to 5 V range. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs). The output code is straight binary with 1 *LSB* = *FS*/4096 = 5 *V*/4096 = 1.22 mV. The same applies for the 0 V to 10 V range, as shown in Figure 6, except that the LSB size is bigger. In this case 1 *LSB* = *FS*/4096 = 10 *V*/4096 = 2.44 mV. The ideal input/output transfer characteristic for both these unipolar ranges is shown in Figure 8.

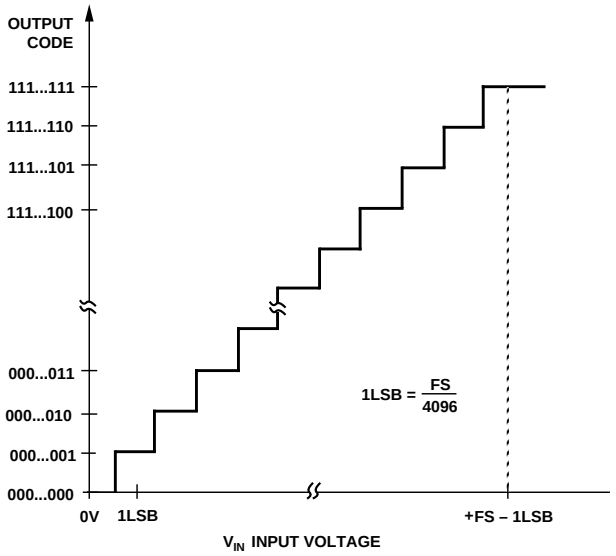

Figure 8. AD7880 Unipolar Transfer Characteristic

Figure 7 shows the AD7880's ±5 V bipolar analog input configuration. Once again the designed code transitions occur midway between successive integer LSB values. The output code is straight binary with 1 *LSB* = *FS*/4096 = 10 *V*/4096 = 2.44 *mV*. The ideal bipolar input/output transfer characteristic is shown in Figure 9.

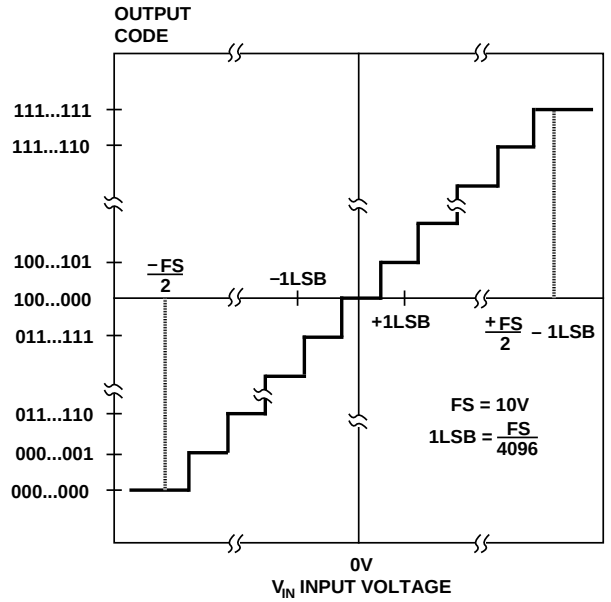

Figure 9. AD7880 Bipolar Transfer Characteristic

CLOCK INPUT

The AD7880 is specified to operate with a 2.5 MHz clock connected to the CLKIN input pin. This pin may be driven directly by CMOS or TTL buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal track-and-hold amplifier. Figure 10 is a typical plot of accuracy versus clock frequency for the ADC.

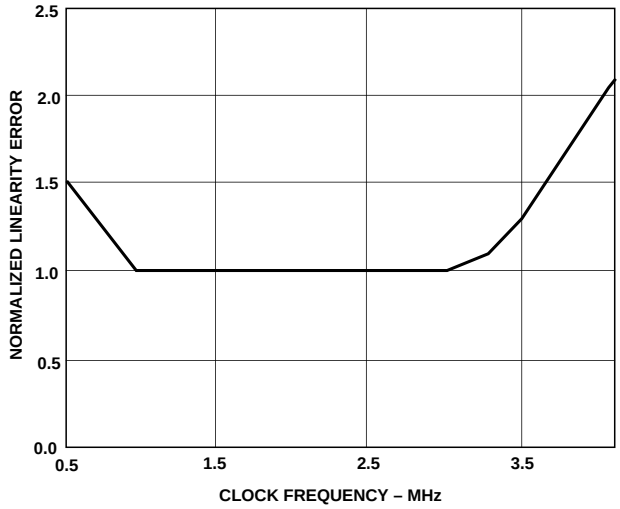

Figure 10. Normalized Linearity Error vs. Clock Frequency

TRACK/HOLD AMPLIFIER

The charge balanced comparator used in the AD7880 for the A/D conversion provides the user with an inherent track/hold function. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 3 µs. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5 MHz input clock, the throughput time is 15 µs.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion, i.e., on the rising edge of $\overline{\text{CONVST}}$ as shown in Figure 1.

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal range match the maximum possible dynamic range of the ADC. In such applications, offset and full-scale error will have to be adjusted to zero.

The following sections describe suggested offset and full-scale adjustment techniques which rely on adjusting the inherent offset of the op amp driving the input to the ADC as well as tweaking an additional external potentiometer as shown in Figure 11.

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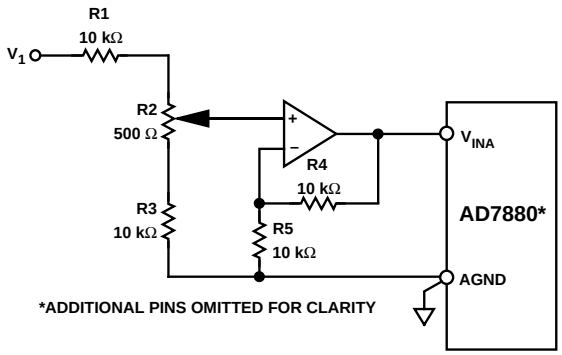

Figure 11. Offset and Full-Scale Adjust Circuit

Unipolar Adjustments

In the case of the 0 V to 5 V unipolar input configuration, unipolar offset error must be adjusted before full-scale error. Adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7880. This is done by applying an input voltage of 0.61 mV (1/2 LSB) to V_1 in Figure 11 and adjusting the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 4.9982 V (FS–3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

The same procedure is required for the 0 V to 10 V input configuration of Figure 6. An input voltage of 1.22 mV (1/2 LSB) is applied to V_1 in Figure 11 and the op amp's offset voltage is adjusted until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 9.9963 V (FS–3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

Bipolar Adjustments

Bipolar zero and full-scale errors for the bipolar input configuration of Figure 7 are adjusted in a similar fashion to the unipolar case. Again, bipolar zero error must be adjusted before full-scale error. Bipolar zero error adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7880 while the input voltage is 1/2 LSB below ground. This is done by applying an input voltage of –1.22 mV (1/2 LSB) to V_1 in Figure 11 and adjusting the op amp offset voltage until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000. For full-scale adjustment, an input voltage of 4.9982 V (FS/2–3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

DYNAMIC SPECIFICATIONS

The AD7880 is specified and tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. The ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7880 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by:

$$SNR = (6.02\ N + 1.76)\ dB \quad (1)$$

where N is the number of bits.

Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the V_{IN} input which is sampled at a 66 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 12 shows a typical 2048 point FFT plot of the AD7880 with an input signal of 2.5 kHz and a sampling frequency of 61 kHz. The SNR obtained from this graph is 73 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

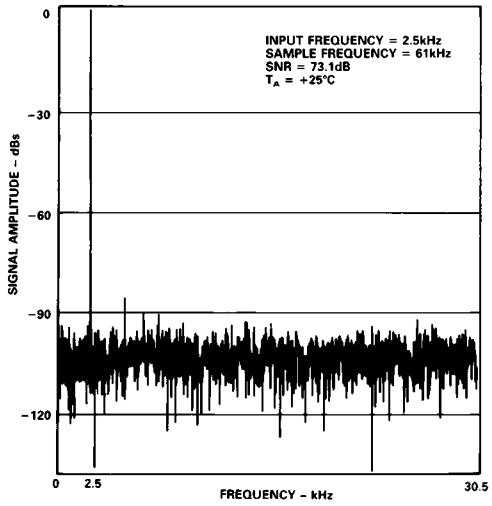

Figure 12. FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 13 shows a plot of effective number of bits versus input frequency for an AD7880 with a sampling frequency of 61 kHz. The effective number of bits typically remains better than 11.5 for frequencies up to 12 kHz.

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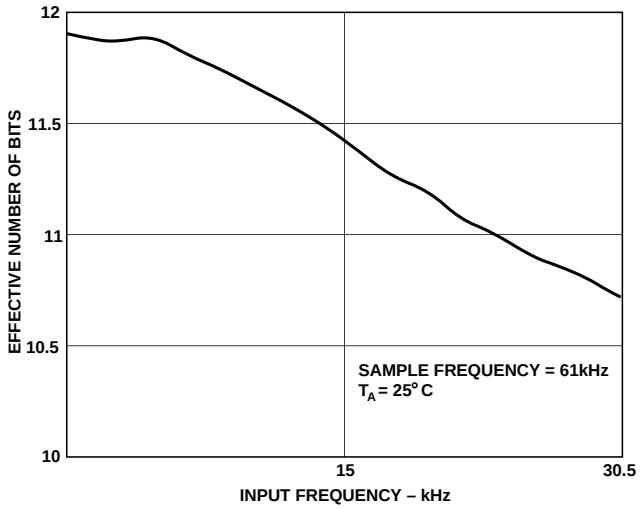

Figure 13. Effective Number of Bits vs. Frequency

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7880, THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}+V_6^{\,2}}}{V_1} \quad (3)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion, sine waves. Figure 14 shows a typical IMD plot for the AD7880.

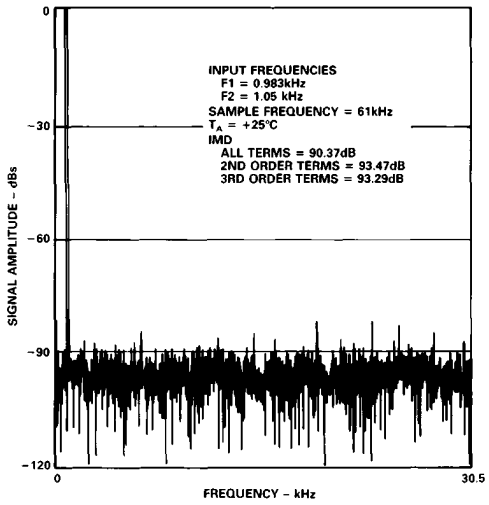

Figure 14. IMD Plot

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

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MICROPROCESSOR INTERFACING

The AD7880 high speed bus timing allows direct interfacing to real time digital signal processors, DSPs, as well as modern high speed, 16-bit microprocessors. Suitable microprocessor interfaces are shown in Figures 15 through 20.

AD7880–ADSP-2100 Interface

Figure 15 shows an interface between the AD7880 and the ADSP-2100. Conversion is initiated using a timer to drive the $\overline{\text{CONVST}}$ input asynchronously to the microprocessor. This allows very accurate control of the sampling instant. When conversion is complete, the AD7880 $\overline{\text{BUSY}}$ line goes high. An inverter on this $\overline{\text{BUSY}}$ output drives the $\overline{\text{IRQ}}$ line low thus providing an interrupt to the ADSP-2100 when conversion is completed. The conversion result is then read from the AD7880 into the ADSP-2100 with the following instruction:

MR0 = DM(ADC)

where *MR0* is the ADSP-2100 MR0 Register and
ADC is the AD7880 address.

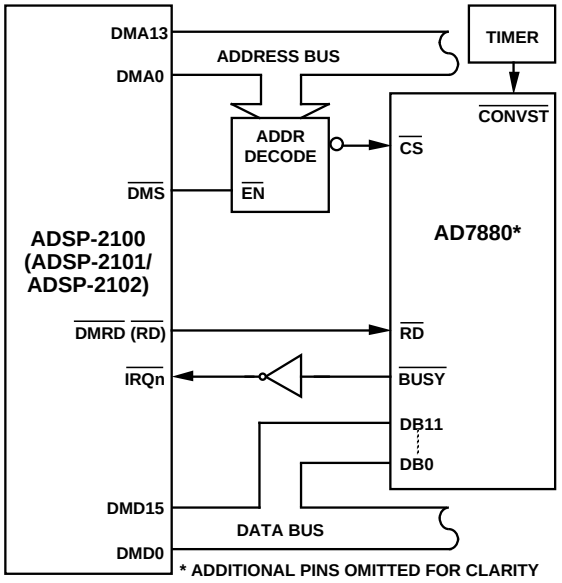

Figure 15. AD7880–ADSP-2100 (ADSP-2101/ADSP-2102) Interface

AD7880-ADSP-2101/ADSP-2102 Interface

The interface outlined in Figure 15 also forms the basis for an interface between the AD7880 and the ADSP-2101/ADSP-2102. The READ line of the ADSP-2101/ADSP-2102 is labeled $\overline{\text{RD}}$. In this interface, the $\overline{\text{RD}}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The instruction used to read a conversion result is as outlined for the ADSP-2100.

AD7880-TMS32010 Interface

An interface between the AD7880 and the TMS32010 is shown in Figure 16. Once again the conversion is initiated using an external timer and the TMS32010 is interrupted when conversion is completed. The following instruction is used to read the conversion result from the AD7880:

IN D,ADC

where *D* is Data Memory Address and
ADC is the AD7880 address.

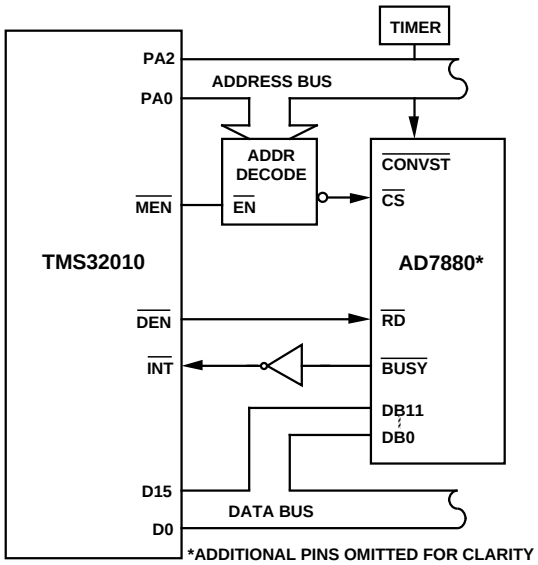

Figure 16. AD7880–TMS32010 Interface

AD7880–TMS320C25 Interface

Figure 17 shows an interface between the AD7880 and the TMS320C25. As with the two previous interfaces, conversion is initiated with a timer, and the processor is interrupted when the conversion sequence is completed. The TMS320C25 does not have a separate $\overline{\text{RD}}$ output to drive the AD7880 $\overline{\text{RD}}$ input directly. This has to be generated from the processor $\overline{\text{STRB}}$ and R/$\overline{\text{W}}$ outputs with the addition of some logic gates. The $\overline{\text{RD}}$ signal is OR-gated with the $\overline{\text{MSC}}$ signal to provide the one WAIT state required in the read cycle for correct interface timing. Conversion results are read from the AD7880 using the following instruction:

IN D,ADC

where *D* is Data Memory Address and
ADC is the AD7880 address.

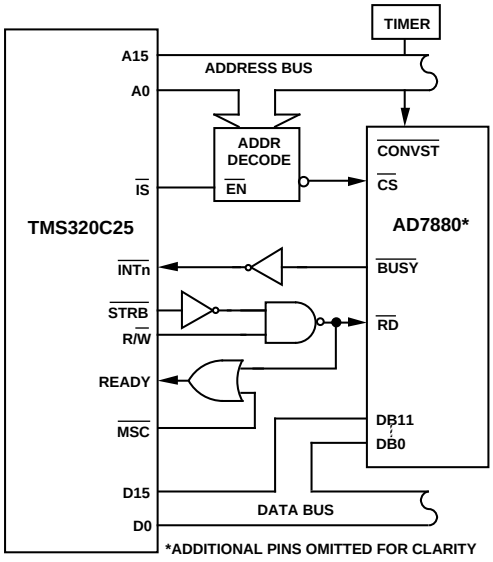

Figure 17. AD7880–TMS320C25 Interface

Some applications may require that the conversion be initiated by the microprocessor rather than an external timer. One option is to decode the AD7880 $\overline{\text{CONVST}}$ from the address bus so that

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a write operation starts a conversion. Data is read at the end of the conversion sequence as before. Figure 19 shows an example of initiating conversion using this method. A similar implementation can be used for DSPs. Note that for all interfaces, a read operation should not be attempted during conversion.

AD7880–MC68000 Interface

An interface between the AD7880 and the MC68000 is shown in Figure 18. As before, conversion is initiated using an external timer. The AD7880 $\overline{BUSY}$ line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7880 is attempted. Because of the nature of its interrupts, the 68000 requires additional logic (not shown in Figure 18) to allow it to be interrupted correctly. For further information on 68000 interrupts, consult the 68000 users manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate a separate $\overline{RD}$ input signal for the AD7880. $\overline{CS}$ is used to drive the 68000 $\overline{DTACK}$ input to allow the processor to execute a normal read operation to the AD7880. The conversion results are read using the following 68000 instruction:

MOVE.W ADC, D0

where *D0* is the 68000 D0 register

ADC is the AD7880 address

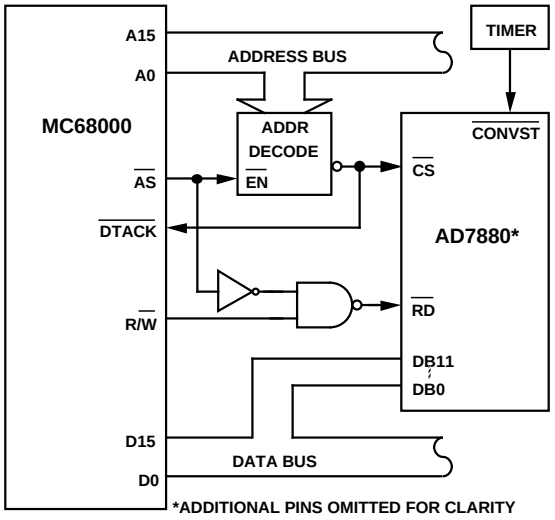

Figure 18. AD7880–MC68000 Interface

AD7880–8086 Interface

Figure 19 shows an interface between the AD7880 and the 8086 microprocessor. Unlike the previous interface examples, the microprocessor initiates conversion. This is achieved by gating the 8086 $\overline{WR}$ signal with a decoded address output (different to the AD7880 $\overline{CS}$ address). Conversion is initiated and the result is read from the AD7880 using the following instruction:

MOV AX, ADC

where *AX* is the 8086 accumulator and
ADC is the AD7880 address

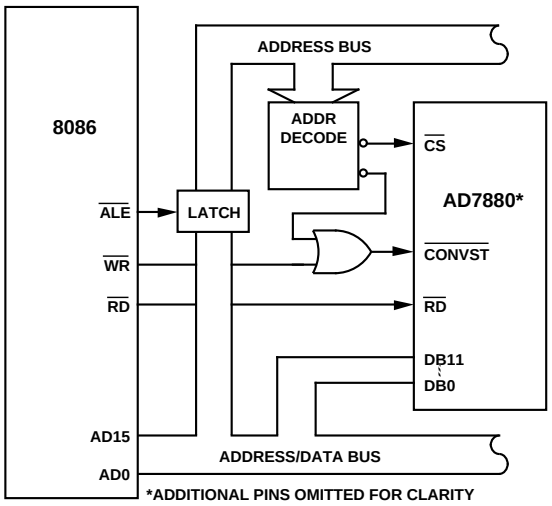

Figure 19. AD7880–8086 Interface

AD7880–6809 Interface

The AD7880 can also interface quite easily with 8-bit microprocessors. The 12-bit parallel data output from the AD7880 can be read into the microprocessor as an 8+4 byte structure. Figure 20 shows an interface to the MC6809 8-bit microprocessor. As in previous cases, conversion is initiated using an external timer. At the end of conversion, $\overline{BUSY}$ triggers a one-shot which drives the $\overline{IRQ}$ interrupt input of the microprocessor. A double read is then performed to two unique addresses. The first read fetches the lower 8 bits (DB0–DB7) and loads the 74HC374 latch with the upper 4 bits (DB8–DB11). The second read fetches these upper 4 bits.

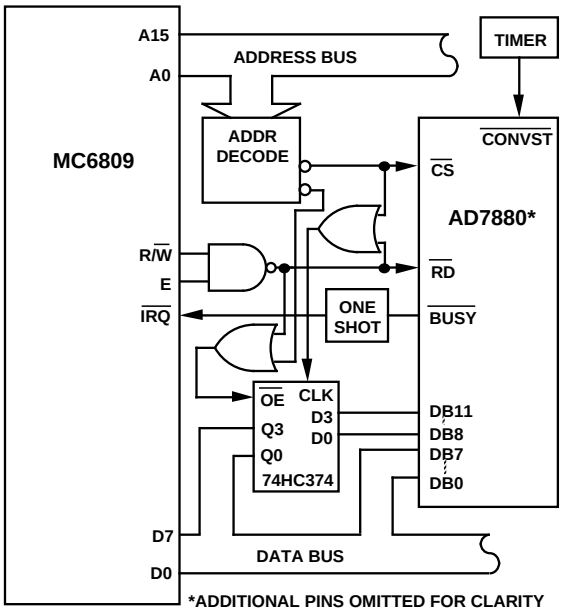

Figure 20. AD7880–6809 Interface

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APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7880's comparator is required to make bit decisions on an LSB size of 1.22 mV. To achieve this, the designer must be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended, as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run digital tracks alongside analog signal tracks. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7880 AGND pin or as close as possible to the AD7880. Connect all other grounds and the AD7880 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 26 and 27 have both analog and digital ground planes which are kept separated and only joined together at the AD7880 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

ANALOG INPUT BUFFERING

To achieve specified performance, it is recommended that the analog input (V_{INA}, V_{INB}) be driven from a low impedance source. This necessitates the use of an input buffer amplifier. The choice of op amp will be a function of the particular application and the desired analog input range. The data acquisition circuit, described in this data sheet allows for various op amp configurations. Figure 21 shows the analog input buffer circuit.

The options available to drive the supply of the op amp are:

Single +5 V (derived from PCB 5 V supply)

Dual Supply (externally supplied to V+ and V–)
±5 V, ±12 V or ±15 V

The simplest configuration is the 0 V to 5 V range of Figure 5. A single supply 5 V op amp is recommended for such an implementation. This will allow for operation of the AD7880 in the 0 V to 5 V unipolar range without supplying an external supply to V+ and V–. The 5 V supply is derived from the systems +5 V V_{DD} supply.

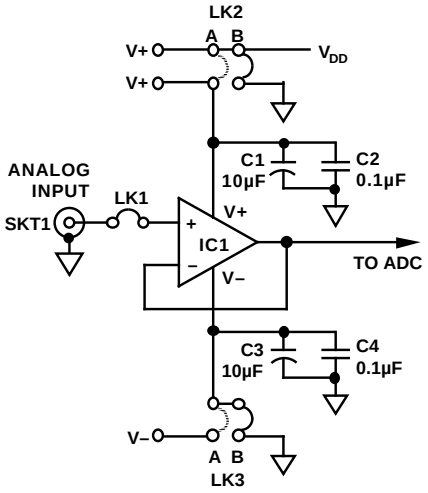

Figure 21. Analog Input Buffering

When it is required to drive the AD7880 with the 0 V to 10 V input range, an external supply must be connected to V+ (see Figure 21).

In bipolar operation, positive and negative supplies must be connected to V+ and V–.

The AD711 is a general purpose op amp which could be used to drive the analog input of the AD7880.

POWER-DOWN CONTROL (MODE INPUT)

The AD7880 is designed for systems which need to have minimum power consumption. This includes such applications as hand held, portable battery powered systems and remote monitoring systems. As well as consuming minimum power under normal operating conditions, typically 20 mW, the AD7880 can be put into a power-down or sleep mode when not required to convert signals. When in this power-down mode, the AD7880 consumes approximately 2 mW of power.

The AD7880 is powered down by bringing the MODE input pin to a Logic Low in conjunction with keeping the $\overline{RD}$ input control High. The AD7880 will remain in the power-down mode until MODE is brought to a Logic High again. The MODE input should be driven with CD4000 or HCMOS logic levels.

It is recommended that one "dummy" conversion be implemented before reading conversion data from the AD7880 after it has been in the power-down mode. This is required to reset all internal logic and control circuitry. In a remote monitoring system where, say, 10 conversions are required to be taken with a sampling interval of 1 second, an additional 11th conversion must be carried out. Figure 22 gives a plot of power consumption

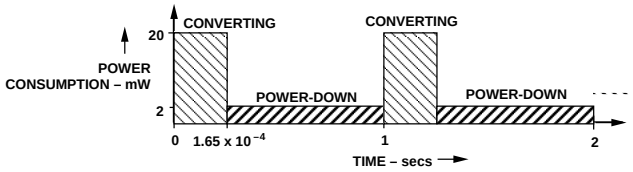

Figure 22. Power Consumption for Normal Operation and Power-Down Operation vs. Time

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as a function of time for such operation. The total conversion time for each cycle is 11 × 15 µs (where 15 µs is the time taken for a single conversion) corresponding to 1.65×10^{-4} secs. Hence:

Average Power = $Power_{CONVERTING} + Power_{POWER\text{-}DOWN}$
= $\{20\ mW \times (1.65 \times 10^{-4})/(10)\}$
+ $\{2\ mW \times (9.9998)/(10)\}$
= 2.029 mW

AD7880 DATA ACQUISITION LAYOUT

Figure 24 shows the AD7880 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 25 to 27.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other input conditioning circuitry. To facilitate this option there is a shorting link (labeled LK1 on the PCB) on the analog input track. With LK1 in place, the analog input connects to the buffer amplifier driving the AD7880. With LK1 removed, a wire link is needed to connect the analog input to the PCB component grid.

INTERFACE CONNECTIONS

The data acquisition board contains a parallel connection port labeled SKT4. This is a 26-contact IDC Connector and provides for direct microprocessor connection to the board. This connector, the pinout of which is shown in Figure 23, contains all data, control and status signals of the AD7880 (with the exception of the $\overline{CONVST}$ and the CLKIN inputs both of which are provided via SKT2 and SKT3 respectively). It also contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for interfacing to many microprocessors including the TMS320C25 and the Motorola 68000 series. Link LK7 selects $\overline{RD}$ directly or alternatively, the decoded version. Note that the AD7880 $\overline{CS}$ input must be decoded prior to the AD7880 evaluation board.

SKT1, SKT2 and SKT3 are three sub-miniature connectors (SMC) which provide input connections for the analog input, the $\overline{CONVST}$ input and the CLKIN input. Three different input ranges can be accepted by the AD7880 each of which is configured by selecting shorting plug options A, B or C of LK4. Position A corresponds to the 0 V to 5 V unipolar configuration of Figure 5, position B corresponds to the bipolar ±5 V configuration of Figure 7 and position C allows for a 0 V to +10 V unipolar range as shown in Figure 6.

POWER SUPPLY CONNECTIONS

The PCB requires a single +5 V power supply (labeled V_{DD}). Good decoupling allows this supply to drive the AD7880 V_{DD} which also drives the V_{REF} input as well as the op amp power supply. In circumstances where bipolar ±5 V or a unipolar 0 V to 10 V input ranges are required, provision has been allowed for the connection of separate op amp power supplies (±15 V, ±12 V, ±5 V, etc.) to V+ and V–. LK2 and LK3 shorting links allow for the selection of user defined op amp power supplies or the on-board single +5 V supply.

LINK OPTIONS

There are seven link options which must be set before using the board. These are outlined below:

LK1 Connects the analog input to a buffer amplifier. The analog input may also be connected to a component grid for signal conditioning.

LK2, LK3 Allows for various op amp power supplies to be used to drive the input buffer of the AD7880. External supplies may be connected to V+ and V–. Alternatively, the AD7880's +5 V system supply and AGND can be selected to drive a single supply op amp.

LK4 Configures the various analog input ranges, 0 V to 5 V, 0 V to 10 V or ±5 V.

LK5 Selects reference input to V_{REF} of AD7880. Normally connected to V_{DD}. An external reference could also be wired in.

LK6 Selects power-down or sleep mode. The shorting plug is connected to V_{DD} for normal operation.

LK7 Connects the AD7880 $\overline{RD}$ input directly to the $\overline{RD}$ input of SKT4 or to a decoded $\overline{STRB}$ and R/$\overline{W}$ input. This shorting plug setting depends on the microprocessor, e.g., the TMS320C25 requires a decoded $\overline{RD}$ signal.

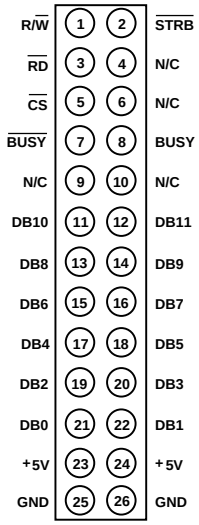

Figure 23. SKT4, IDC Connector Pinout

COMPONENT LIST

IC1	Op Amp*
IC2	AD7880 Analog-to-Digital Converter
IC3	74HC00 Quad NAND Gate
C1, C3, C5	10 µF Capacitors
C2, C4, C6, C7	0.1 µF Capacitors
R1, R2	10 kΩ Pull-up Resistors
LK1, LK2, LK3 LK4, LK5, LK6 LK7	Shorting Links
SKT1, SKT2, SKT3	Sub-Miniature Connectors
	Vendor No: Sealectro 50-051-0000 (Socket) Sealectro 50-007-0000 (Plug)
SKT4	26-Contact (2 Row) IDC Connector

NOTE
*See ANALOG INPUT BUFFERING section.

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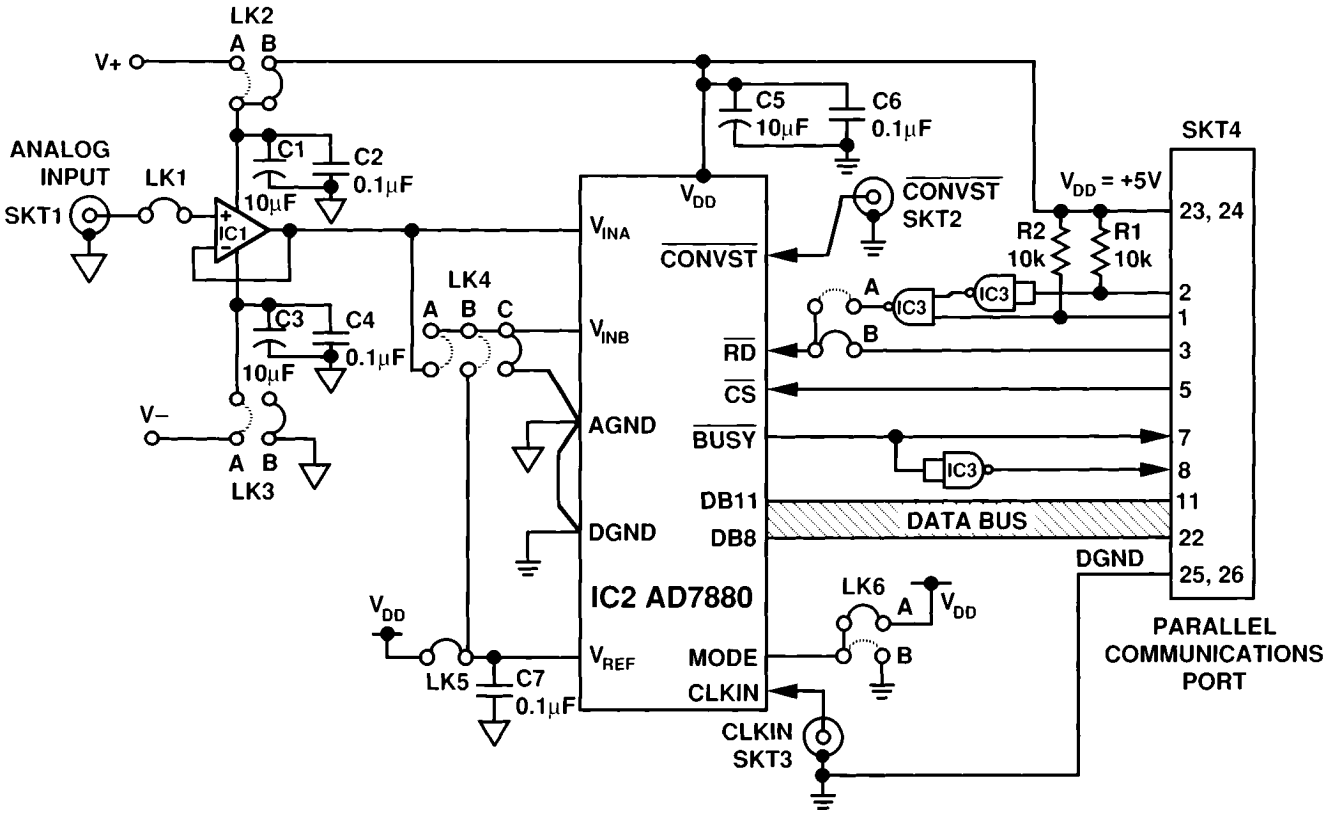

Figure 24. Data Acquisition Circuit Using the AD7880

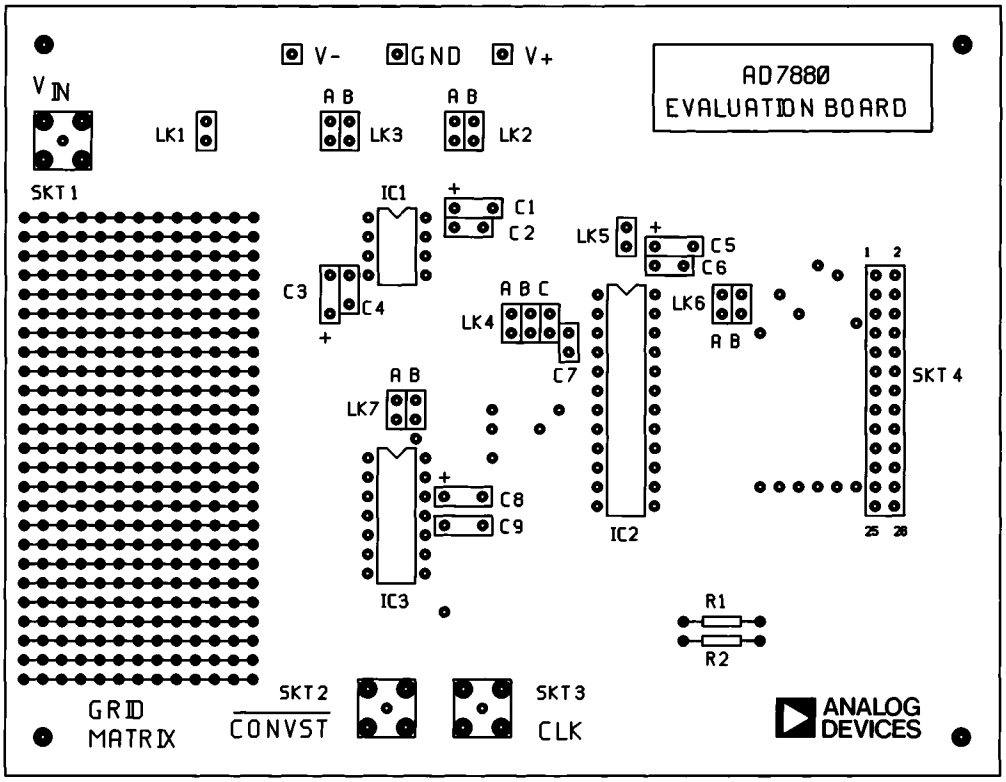

Figure 25. PCB Silkscreen for Figure 24

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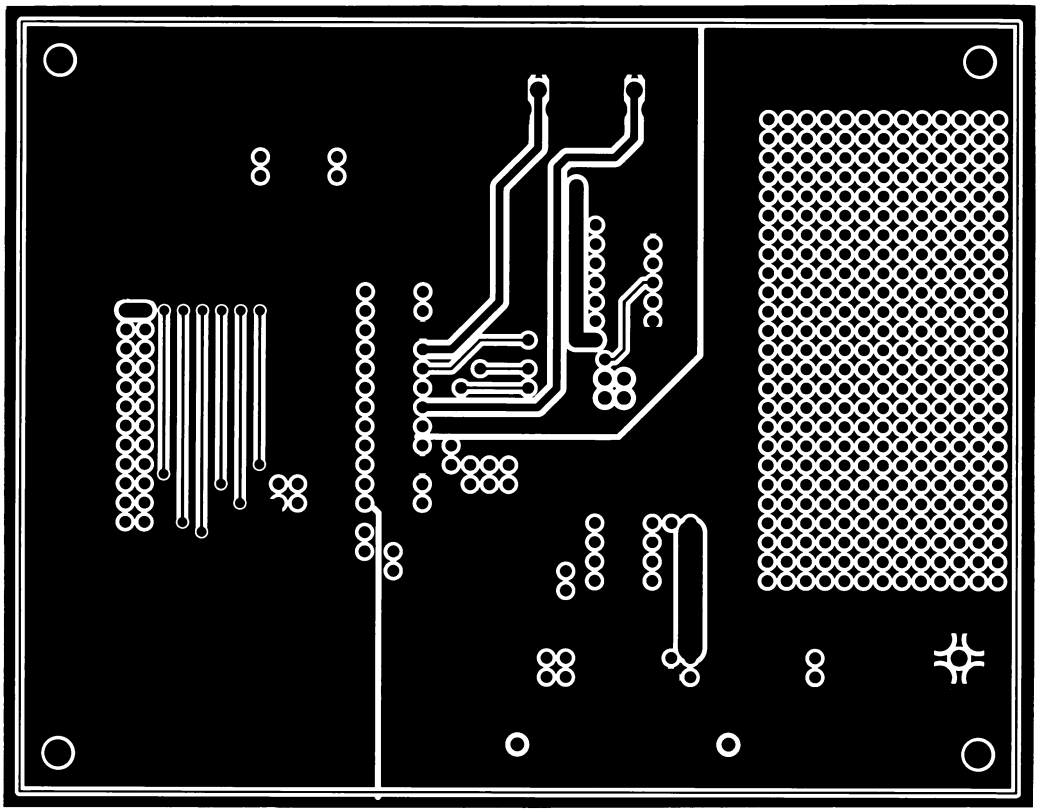

Figure 26. PCB Component Side Layout for Figure 24

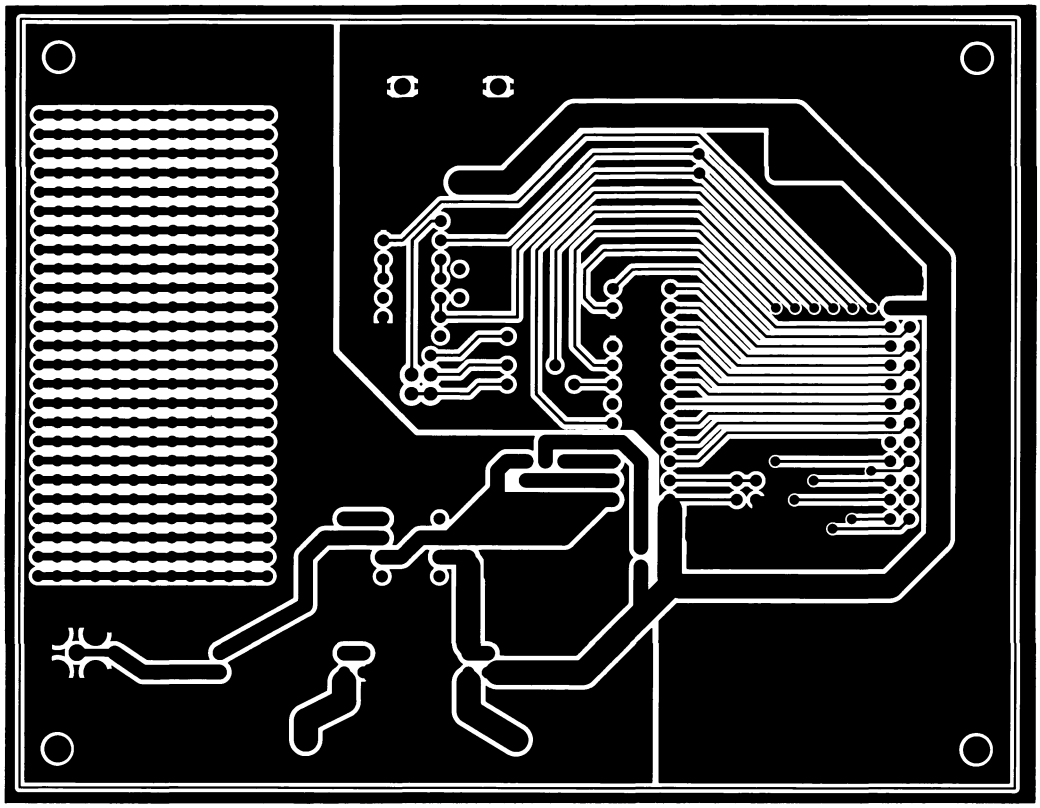

Figure 27. PCB Solder Side Layout for Figure 24

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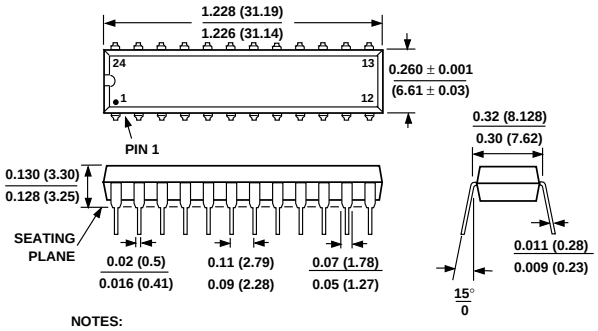
OUTLINE DIMENSIONS

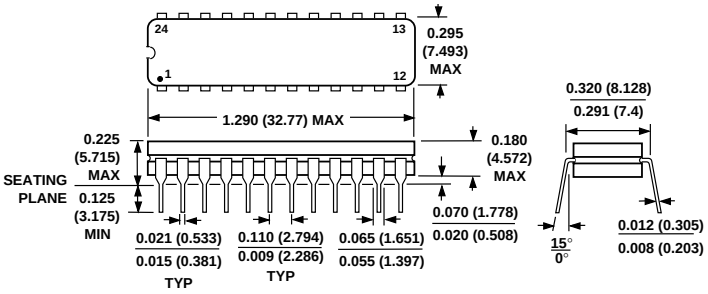
Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24)



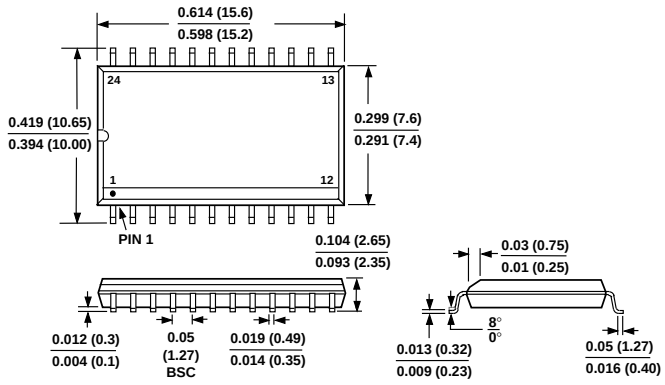
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead Cerdip (Q-24)



1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead SOIC (R-24)



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