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REVISION HISTORY

8/13—Rev. 0 to Rev. A

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5/03—Revision 0: Initial Version

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SPECIFICATIONS

–40°C to +105°C; AV_{DD} = 5 V ± 5%; DV_{DD} = 2.7 V to 3.6 V, or 5 V ± 5%; REFIN(+) = 2.5 V; REFIN(–) = 0 V, AINCOM = 2.5 V; Internal Buffer On, AIN Range = ±1.25 V; f_{MCLKIN} = 6.144 MHz; unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC PERFORMANCE, CHOPPING ENABLED					
Conversion Time Rate	372		11840	Hz	Configure via conv. time register
No Missing Codes[1, 2]	24			Bits	FW ≥ 12 (conversion time ≥ 290 µs)
Output Noise		See Table 5			
Resolution		See Table 6 and Table 7			
Integral Nonlinearity (INL)[2]		±0.0005	±0.0015	% of FSR	
Offset Error (Unipolar, Bipolar)[3]		±10		µV	Before calibration
Offset Drift vs. Temperature[1]			±25	nV/°C	
Gain Error[3]			±0.2	%	Before calibration
Gain Drift vs. Temperature[1]			±2.5	ppm of FS/°C	
Positive Full-Scale Error[3]			±0.2	% of FSR	Before calibration
Positive Full-Scale Drift vs. Temp.[1]			±2.5	ppm of FS/°C	
Bipolar Negative Full-Scale Error[4]		±0.0030		% of FSR	After calibration
Common-Mode Rejection	80	95		dB	At dc, AIN = 1 V
Power Supply Rejection	70	80		dB	At dc, AIN = 1 V
ADC PERFORMANCE, CHOPPING DISABLED					
Conversion Time Rate	737		15133	Hz	Configure via conv. time register
No Missing Codes[1, 2]	24			Bits	FW ≥ 12 (conversion time ≥ 290 µs)
Output Noise		See Table 8			
Resolution		See Table 9 and Table 10			
Integral Nonlinearity (INL)[2]		±0.0015		% of FSR	
Offset Error (Unipolar, Bipolar)[5]		±1		mV	Before calibration
Offset Drift vs. Temperature		±1.5		µV/°C	
Gain Error[3]		±0.2		%	Before calibration
Gain Drift vs. Temperature		±2.5		ppm of FS/°C	
Positive Full-Scale Error[3]		±0.2		% of FSR	Before calibration
Positive Full-Scale Drift vs. Temp.		±2.5		ppm of FS/°C	
Bipolar Negative Full-Scale Error[4]		±0.0030		% of FSR	After calibration
Common-Mode Rejection		75		dB	At dc, AIN = 1 V
Power Supply Rejection		65		dB	At dc, AIN = 1 V
ANALOG INPUTS					
Analog Input Voltage[1, 6]					
±2.5 V Range		±2.5		V	
2.5 V Range		0 to 2.5		V	
±1.25 V Range		±1.25		V	
1.25 V Range		0 to 1.25		V	
±0.625 V Range		±0.625		V	
0.625 V Range		0 to 0.625		V	
AIN, AINCOM Common-Mode/ Absolute Voltage[1]	0.2		AV_{DD} – 0.3	V	
Analog Input Slew Rate[1, 7]			0.5	V/conv. time	AIN absolute voltage > 3 V
AIN, AINCOM Input Current[1, 8]		1	5	nA	Only one channel, chop disabled

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS					
REFIN(+) to REFIN(−) Voltage[1, 9]	2.475	2.5	2.525	V	
NOREF Trigger Voltage		0.5		V	NOREF bit in channel status register
REFIN(+), REFIN(−) Common-Mode/ Absolute Voltage[1]	0		AV_{DD}	V	
Reference Input DC Current[10]			400	µA	
SYSTEM CALIBRATION[1, 11]					
Full-Scale Calibration Limit			+1.05 × FS	V	
Zero-Scale Calibration Limit	−1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
LOGIC INPUTS					
Input Current			±1	µA	
Input Current $\overline{CS}$			±10	µA	$\overline{CS}$ = DV_{DD}
			−40	µA	$\overline{CS}$ = DGND, internal pull-up resistor
Input Capacitance		5		pF	
V_{T+}[1]	1.4		2	V	DV_{DD} = 5 V
V_{T-}[1]	0.8		1.4	V	DV_{DD} = 5 V
$V_{T+} - V_{T-}$[1]	0.3		0.85	V	DV_{DD} = 5 V
V_{T+}[1]	0.95		2	V	DV_{DD} = 3 V
V_{T-}[1]	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} - V_{T-}$[1]	0.3		0.85	V	DV_{DD} = 3 V
MCLK IN ONLY					
Input Current			±10	µA	
Input Capacitance		5		pF	
V_{INL} Input Low Voltage			0.8	V	DV_{DD} = 5 V
V_{INH} Input High Voltage	3.5			V	DV_{DD} = 5 V
V_{INL} Input Low Voltage			0.4	V	DV_{DD} = 3 V
V_{INH} Input High Voltage	2.5			V	DV_{DD} = 3 V
LOGIC OUTPUTS[12]					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 800 µA, DV_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 µA, DV_{DD} = 5 V
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 100 µA, DV_{DD} = 3 V
V_{OH} Output High Voltage	DV_{DD} − 0.6			V	I_{SOURCE} = 100 µA, DV_{DD} = 3 V
Floating State Leakage Current			±1	µA	
Floating State Leakage Capacitance		3		pF	
P0, P1 INPUTS/OUTPUTS					Levels referenced to analog supplies
Input Current			±10	µA	
V_{INL} Input Low Voltage			0.8	V	AV_{DD} = 5 V
V_{INH} Input High Voltage	3.5			V	AV_{DD} = 5 V
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 8 mA, AV_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 µA, AV_{DD} = 5 V

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
AV_{DD} to AGND Voltage	4.75		5.25	V	
DV_{DD} to DGND Voltage	4.75		5.25	V	
	2.70		3.60	V	
AV_{DD} Current (Normal Mode)		13.6	16	mA	
AV_{DD} Current (Reduced Power Mode)		9.2	11	mA	MCLK = 4 MHz
AV_{DD} Current (Internal Buffer Off)		8.5		mA	
DV_{DD} Current (Normal Mode)[13]		2.7	3	mA	DV_{DD} = 5 V
DV_{DD} Current (Normal Mode)[13]		1.0	1.5	mA	DV_{DD} = 3 V
Power Dissipation (Normal Mode)[13]		85	100	mW	
Power Dissipation (Reduced Power Mode)[13]		60	70	mW	DV_{DD} = 5 V, MCLK = 4 MHz
Power Dissipation (Reduced Power Mode)[13]		50		mW	DV_{DD} = 3 V, MCLK = 4 MHz
AV_{DD} + DV_{DD} Current (Standby Mode)[14]		80		µA	
Power Dissipation (Standby Mode)[14]		500		µW	

[1] Specification is not production tested, but is supported by characterization data at initial product release.
[2] See Typical Performance Characteristics.
[3] Specifications before calibration. Channel system calibration reduces these errors to the order of the noise.
[4] Applies after the zero-scale and full-scale calibration. The negative full-scale error represents the remaining error after removing the offset and gain error.
[5] Specifications before calibration. ADC zero-scale self-calibration or channel zero-scale system calibration reduce this error to the order of the noise.
[6] For specified performance. The output data span corresponds to the specified nominal input voltage range. The ADC is functional outside the nominal input voltage range, but the performance might degrade. Outside the nominal input voltage range, the OVR bit in the channel status register is set and the channel data register value depends on the clamp bit in the mode register. See the register and circuit descriptions for details.
[7] For specified performance. If the analog input absolute voltage (referred to AGND) changes more than 0.5 V during one conversion time, the result can be affected by distortion in the input buffer. This limit does not apply to analog input absolute voltages below 3 V.
[8] If chopping is enabled or when switching between channels, a dynamic current charges the capacitance of the multiplexer. See the circuit description for details.
[9] For specified performance. Part is functional with lower V_{REF}.
[10] Dynamic current charging the sigma-delta (Σ-Δ) modulator input switching capacitor.
[11] Outside the specified calibration range, calibration is possible but the performance may degrade.
[12] These logic output levels apply to the MCLK OUT output when it is loaded with a single CMOS load.
[13] With external MCLK, MCLKOUT disabled (CLKDIS bit set in the mode register).
[14] External MCLKIN = 0 V or DV_{DD}, digital inputs = 0 V or DV_{DD}, P0 and P1 = 0 V or AV_{DD}.

TIMING SPECIFICATIONS

AV_{DD} = 5 V ± 5%, DV_{DD} = 2.7 V to 3.6 V or 5 V ± 5%, Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise noted.[1]

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MASTER CLOCK RANGE	1		6.144	MHz	
	1		4	MHz	Reduced power mode
t_1	50			ns	$\overline{SYNC}$ pulse width
t_2	500			ns	$\overline{RESET}$ pulse width
READ OPERATION					
t_4	0			ns	$\overline{CS}$ falling edge to SCLK falling edge setup time
t_5[2]					SCLK falling edge to data valid delay
	0		60	ns	DV_{DD} of 4.75 V to 5.25 V
	0		80	ns	DV_{DD} of 2.7 V to 3.3 V
t_{5A}[2, 3]					$\overline{CS}$ falling edge to data valid delay
	0		60	ns	DV_{DD} of 4.75 V to 5.25 V
	0		80	ns	DV_{DD} of 2.7 V to 3.3 V
t_6	50			ns	SCLK high pulse width
t_7	50			ns	SCLK low pulse width
t_8	0			ns	$\overline{CS}$ rising edge after SCLK rising edge hold time
t_9[4]	10		80	ns	Bus relinquish time after SCLK rising edge

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WRITE OPERATION					
t_{11}	0			ns	$\overline{CS}$ falling edge to SCLK falling edge setup
t_{12}	30			ns	Data valid to SCLK rising edge setup time
t_{13}	25			ns	Data valid after SCLK rising edge hold time
t_{14}	50			ns	SCLK high pulse width
t_{15}	50			ns	SCLK low pulse width
t_{16}	0			ns	$\overline{CS}$ rising edge after SCLK rising edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V. See Figure 2 and Figure 3.
[2] These numbers are measured with the load circuit of Figure 4 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[3] This specification is relevant only if $\overline{CS}$ goes low while SCLK is low.
[4] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 4. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the Timing Specifications are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

TIMING DIAGRAMS

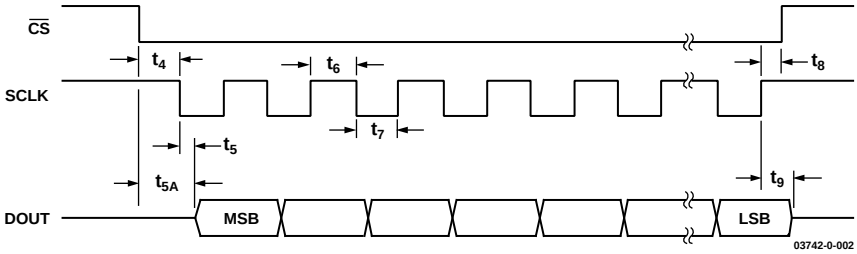

Figure 2. Read Cycle Timing Diagram

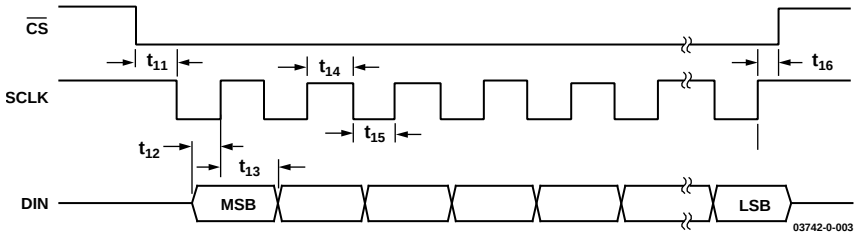

Figure 3. Write Cycle Timing Diagram

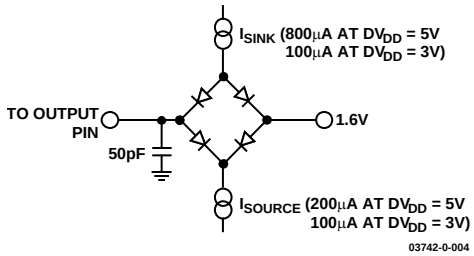

Figure 4. Load Circuit for Access Time and Bus Relinquish Time

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND, DV_{DD} to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
AV_{DD} to DV_{DD}	−5 V to +5 V
AIN, AINCOM to AGND	−0.3 V to AV_{DD} + 0.3 V
REFIN(+), REFIN(−) to AGND	−0.3 V to AV_{DD} + 0.3 V
P0, P1 Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
ESD Rating (ESD Association Human Body Model, S5.1)	4000 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package θ_{JA} Thermal Impedance	128°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

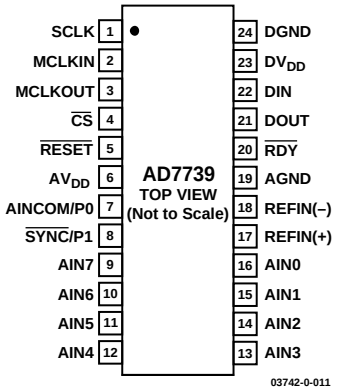

Figure 5. Pin Configuration (24-Lead TSSOP)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock. Schmitt triggered logic input. An external serial clock is applied to this input to transfer serial data to or from the AD7739.
2	MCLKIN	Master Clock Signal for the ADC. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLKIN and MCLKOUT pins. Alternatively, MCLKIN can be driven with a CMOS compatible clock and MCLKOUT can be left unconnected.
3	MCLKOUT	Master Clock Signal for the ADC. When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLKIN and MCLKOUT. If an external clock is applied to the MCLKIN, MCLKOUT provides an inverted clock signal or can be switched off to reduce the device power consumption. MCLKOUT can drive one CMOS load.
4	$\overline{CS}$	Chip Select. Active low Schmitt triggered logic input with an internal pull-up resistor. With this input hardwired low, the AD7739 can operate in its 3-wire interface mode using SCLK, DIN, and DOUT. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus. It can also be used as an 8-bit frame synchronization signal.
5	$\overline{RESET}$	Schmitt Triggered Logic Input. Active low input that resets the control logic, interface logic, digital filter, analog modulator, and all on-chip registers of the part to power-on status. Effectively, everything on the part except the clock oscillator is reset when the $\overline{RESET}$ pin is exercised.
6	AV_{DD}	Analog Positive Supply Voltage, 5 V to AGND Nominal.
7	AINCOM/P0	Analog Inputs Common Terminal/Digital Output. The function of this pin is determined by the P0 DIR bit in the I/O port register; the digital value can be written as the P0 bit in the I/O port register. The digital voltage is referenced to analog supplies. When configured as an input (P0 DIR bit set to 1), the single-ended analog inputs 0 to 7 (AIN0 to AIN7) can be referenced to the voltage level of this pin.
8	$\overline{SYNC}$/P1	$\overline{SYNC}$/Digital Input/Digital Output. The pin direction is determined by the P1 DIR bit; the digital value can be read/written as the P1 bit in the I/O port register. When the sync bit in the I/O port register is set to 1, then the $\overline{SYNC}$/P1 pin can be used to synchronize the AD7739 modulator and digital filter with other devices in the system. The digital voltage is referenced to the analog supplies. When configured as an input, tie the pin high or low.
9 to 16	AIN0 to AIN7	Analog Inputs.
17	REFIN(+)	Positive Terminal of the Differential Reference Input. REFIN(+) voltage potential can lie anywhere between AV_{DD} and AGND. In normal circuit configuration, connect this pin to a 2.5 V reference voltage.
18	REFIN(–)	Negative Terminal of the Differential Reference Input. REFIN(–) voltage potential can lie anywhere between AV_{DD} and AGND. In normal circuit configuration, connect this pin to a 0 V reference voltage.

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Pin No.	Mnemonic	Description
19	AGND	Ground Reference Point for Analog Circuitry.
20	$\overline{\text{RDY}}$	Logic Output. Used as a status output in both conversion mode and calibration mode. In conversion mode, a falling edge on this output indicates that either any channel or all channels have unread data available, according to the RDYFN bit in the I/O port register. In calibration mode, a falling edge on this output indicates that calibration is complete (see the Digital Interface Description section for details).
21	DOUT	Serial Data Output. Serial data is read from the output shift register on the part. This output shift register can contain information from any AD7739 register, depending on the address bits of the communications register.
22	DIN	Serial Data Input (Schmitt Triggered). Serial data is written to the input shift register on the part. Data from this input shift register is transferred to any AD7739 register, depending on the address bits of the communications register.
23	DV_{DD}	Digital Supply Voltage, 3 V or 5 V Nominal.
24	DGND	Ground Reference Point for Digital Circuitry.

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TYPICAL PERFORMANCE CHARACTERISTICS

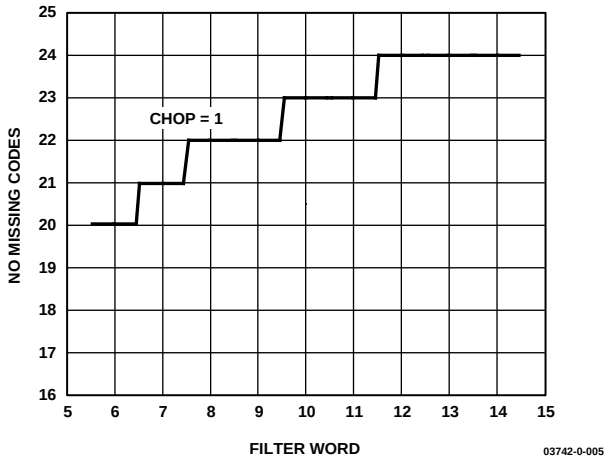

Figure 6. No Missing Codes Performance, Chopping Enabled

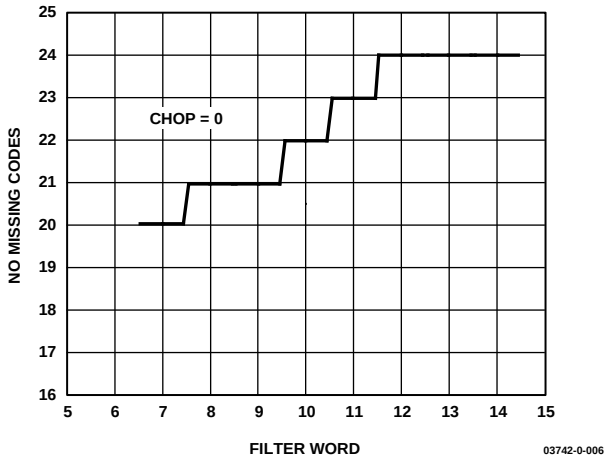

Figure 7. No Missing Codes Performance, Chopping Disabled

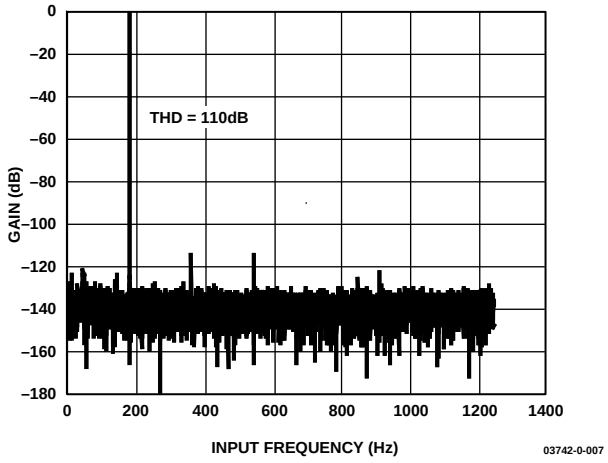

Figure 8. Typical FFT Plot; Input Sine Wave 183 Hz,1.2 V Peak, AIN Range ±1.25 V, Conversion Time 397 µs, Chopping Enabled, MCLK = 6.144 MHz

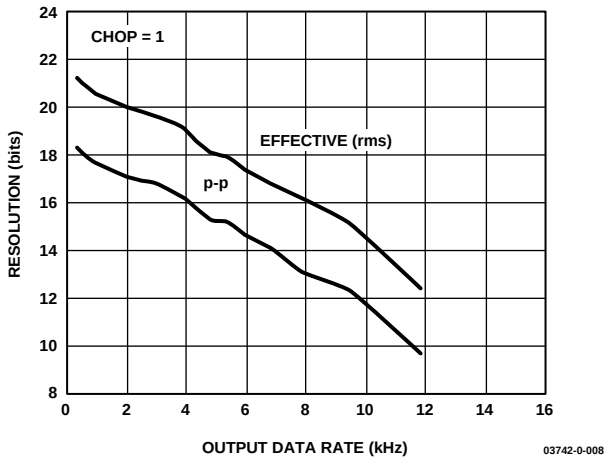

Figure 9. Typical Effective and Peak-to-Peak Resolution; AIN Voltage = 0 V, AIN Range ±1.25 V, Chopping Enabled, MCLK = 6.144 MHz

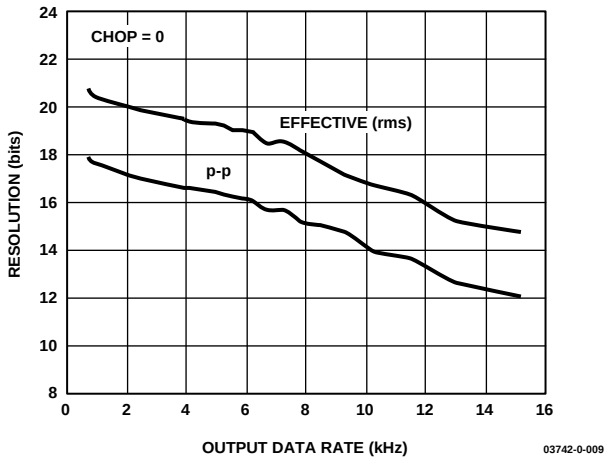

Figure 10. Typical Effective and Peak-to-Peak Resolution; AIN Voltage = 0 V, AIN Range ±1.25 V, Chopping Disabled, MCLK = 6.144 MHz

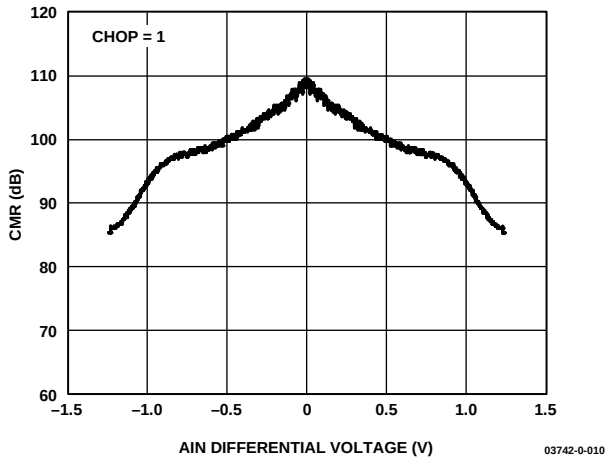

Figure 11. Typical Common-Mode Rejection vs. AIN Voltage; AIN Range ±1.25 V, Conversion Time 397 µs, Chopping Enabled, MCLK = 6.144 MHz

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OUTPUT NOISE AND RESOLUTION SPECIFICATION

The AD7739 can be operated with chopping enabled or disabled, allowing the ADC to be programmed to optimize either the offset drift performance or the throughput rate and channel switching time. Noise tables for these two primary modes of operation are outlined below for a selection of output rates and settling times.

The AD7739 noise performance depends on the selected chopping mode, the filter word (FW) value, and the selected analog input range. The AD7739 noise does not vary significantly with MCLK frequency.

CHOPPING ENABLED

The first mode, in which the AD7739 is configured with chopping enabled (chop = 1), provides very low noise with lower output rates.

Table 5 to Table 7 show the −3 dB frequencies and typical performance versus the channel conversion time and equivalent output data rate, respectively.

Table 5 shows the typical output rms noise. Table 6 shows the typical effective resolution based on rms noise. Table 7 shows the typical output peak-to-peak resolution, representing values for which there is no code flicker within a 6-sigma limit. The peak-to-peak resolutions are not calculated based on rms noise but on peak-to-peak noise.

These typical numbers are generated from 4096 data samples acquired in continuous conversion mode with an analog input voltage set to 0 V and MCLK = 6.144 MHz. The conversion time is selected via the channel conversion time register.

Table 5. Typical Output RMS Noise in µV vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	−3 dB Frequency (Hz)	Input Range/RMS Noise (µV)	
					±2.5 V, +2.5 V	±1.25 V, +1.25 V, ±0.625 V, +0.625 V
127	0xFF	2689	372	200	1.8	1.1
46	0xAE	1001	999	500	2.7	1.7
17	0x91	397	2519	1325	4.8	2.7
10	0x8A	251	3982	2209	9.3	4.7
9	0x89	230	4342	2450	10.8	6.3
2	0x82	84	11838	9500	600	460

Table 6. Typical Effective Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	−3 dB Frequency (Hz)	Input Range/Effective Resolution (Bits)					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±0.625 V	+0.625 V
127	0xFF	2689	372	200	21.4	20.4	21.2	20.2	20.2	19.2
46	0xAE	1001	999	500	20.8	19.8	20.5	19.5	19.5	18.5
17	0x91	397	2519	1325	20.0	19.0	19.8	18.8	18.8	17.8
10	0x8A	251	3982	2209	19.0	18.0	19.0	18.0	18.0	17.0
9	0x89	230	4342	2450	18.8	17.8	18.6	17.6	17.6	16.6
2	0x82	84	11838	9500	12.9	11.9	12.4	11.4	11.4	10.4

Table 7. Typical Peak-to-Peak Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	−3 dB Frequency (Hz)	Input Range/Peak-to-Peak Resolution (Bits)					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±0.625 V	+0.625 V
127	0xFF	2689	372	200	18.6	17.6	18.3	17.3	17.3	16.3
46	0xAE	1001	999	500	17.9	16.9	17.6	16.6	16.6	15.6
17	0x91	397	2519	1325	17.1	16.1	16.9	15.9	15.9	14.9
10	0x8A	251	3982	2209	16.2	15.2	16.2	15.2	15.2	14.2
9	0x89	230	4342	2450	16.0	15.0	15.8	14.8	14.8	13.8
2	0x82	84	11838	9500	10.7	0.7	9.7	8.7	8.7	7.7

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CHOPPING DISABLED

The second mode, in which the AD7739 is configured with chopping disabled (chop = 0), provides faster conversion time while maintaining high resolution. Table 8 to Table 10 show the −3 dB frequencies and typical performance versus the channel conversion time and equivalent output data rate, respectively. Table 8 shows the typical output rms noise. Table 9 shows the typical effective resolution based on the rms noise.

Table 10 shows the typical output peak-to-peak resolution, representing values for which there is no code flicker within a 6-sigma limit. The peak-to-peak resolutions are not calculated based on rms noise but on peak-to-peak noise.

These typical numbers are generated from 4096 data samples acquired in continuous conversion mode with an analog input voltage set to 0 V and MCLK = 6.144 MHz. The conversion time is selected via the channel conversion time register.

Table 8. Typical Output RMS Noise in µV vs. Conversion Time and Input Range with Chopping Disabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	−3 dB Frequency (Hz)	Input Range/RMS Noise (µV)	
					±2.5 V, +2.5 V	±1.25 V, +1.25 V, ±0.625 V, +0.625 V
127	0x7F	1358	737	675	2.4	1.5
92	0x5C	993	1007	950	3.0	1.8
35	0x23	399	2504	2500	4.5	2.7
16	0x10	201	4963	5400	6.9	4.1
12	0x0C	160	6257	7250	9.6	5.3
11	0x0B	149	6693	7900	11.4	6.9
3	0x03	66	15133	29000	200	90

Table 9. Typical Effective Resolution in Bits vs. Conversion Time and Input Range with Chopping Disabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	−3 dB Frequency (Hz)	Input Range/Effective Resolution (Bits)					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±0.625 V	+0.625 V
127	0x7F	1358	737	675	21.0	20.0	20.6	19.6	19.6	18.6
92	0x5C	993	1007	950	20.7	19.7	20.4	19.4	19.4	18.4
35	0x23	399	2504	2500	20.1	19.1	19.8	18.8	18.8	17.8
16	0x10	201	4963	5400	19.4	18.4	19.2	18.2	18.2	17.2
12	0x0C	160	6257	7250	18.9	17.9	18.8	17.8	17.8	16.8
11	0x0B	149	6693	7900	18.8	17.8	18.5	17.5	17.5	16.5
3	0x03	66	15133	29000	14.6	13.6	14.7	13.7	13.7	12.7

Table 10. Typical Peak-to-Peak Resolution in Bits vs. Conversion Time and Input Range with Chopping Disabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	−3 dB Frequency (Hz)	Input Range/Peak-to-Peak Resolution (Bits)					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±0.625 V	+0.625 V
127	0x7F	1358	737	675	18.2	17.2	17.8	16.8	16.8	15.8
92	0x5C	993	1007	950	17.8	16.8	17.6	16.6	16.6	15.6
35	0x23	399	2504	2500	17.2	16.2	17.0	16.0	16.0	15.0
16	0x10	201	4963	5400	16.6	15.6	16.4	15.4	15.4	14.4
12	0x0C	160	6257	7250	16.1	15.1	16.0	15.0	15.0	14.0
11	0x0B	149	6693	7900	16.0	15.0	15.7	14.7	14.7	13.7
3	0x03	66	15133	29000	11.7	10.7	12.0	11.0	11.0	10.0

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REGISTER DESCRIPTIONS

Table 11. Register Summary

Register	Addr (hex)	Dir	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Default Value							
Communications	0x00	W	0	R/$\overline{W}$	6-bit register address					
I/O Port	0x01	R/W	P0	P1	P0 DIR	P1 DIR	RDYFN	REDPWR	0	Sync
			P0 pin	P1 pin	1	1	0	0	0	0
Revision	0x02	R	Chip revision code				Chip generic code			
			x	x	x	x	1	0	0	1
Test	0x03	R/W	24-bit manufacturing test register							
ADC Status	0x04	R	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
			0	0	0	0	0	0	0	0
Checksum	0x05	R/W	16-bit checksum register							
ADC Zero-Scale Calibration	0x06	R/W	24-bit ADC zero-scale calibration register							
			0x80 0000							
ADC Full-Scale Calibration	0x07	R/W	24-bit ADC full-scale register							
			0x80 0000							
Channel Data[1]	0x08 to 0x0F	R	16-/24-bit data registers							
			0x8000							
Channel Zero-Scale Calibration[1]	0x10 to 0x17	R/W	24-bit channel zero-scale calibration registers							
			0x80 0000							
Channel Full-Scale Calibration[1]	0x18 to 0x1F	R/W	24-bit channel full-scale calibration registers							
			0x20 0000							
Channel Status[1]	0x20 to 0x27	R	CH2	CH1	CH0	0/P0	RDY/P1	NOREF	Sign	OVR
			Channel number			0	0	0	0	0
Channel Setup[1]	0x28 to 0x2F	R/W	BUFOFF	COM1	COM0	Stat OPT	Enable	RNG2	RNG1	RNG0
			0	0	0	0	0	0	0	0
Channel Conversion Time[1]	0x30 to 0x37	R/W	Chop	FW (7-bit filter word)						
			1	0x11						
Mode[2]	0x38 to 0x3F	R/W	MD2	MD1	MD0	CLKDIS	Dump	Cont RD	24/16 bit	Clamp
			0	0	0	0	0	0	0	0

[1] The three LSBs of the register address, that is, Bit 2, Bit 1, and Bit 0 in the communications register, specify the channel number of the register being accessed.
[2] The AD7739 has only one mode register, although the mode register can be accessed in one of eight address locations. The address used to write the mode register specifies the ADC channel on which the mode is applied. Only Address 0x38 must be used for reading from the mode register.

Table 12. Operational Mode Summary

MD2	MD1	MD0	Mode
0	0	0	Idle
0	0	1	Continuous conversion
0	1	0	Single conversion
0	1	1	Power-down (standby)
1	0	0	ADC zero-scale self-calibration
1	0	1	ADC full-scale self-calibration (for 2.5 V)
1	1	0	Channel zero-scale system calibration
1	1	1	Channel full-scale system calibration

Table 13. Input Range Summary

RNG2	RNG1	RNG0	Nominal Input Voltage Range
1	0	0	±2.5 V
1	0	1	+2.5 V
0	0	0	±1.25 V
0	0	1	+1.25 V
0	1	0	±0.625 V
0	1	1	+0.625 V

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REGISTER ACCESS

The AD7739 is configurable through a series of registers. Some of them configure and control general AD7739 features, while others are specific to each channel. The register data widths vary from 8 bits to 24 bits. All registers are accessed through the communications register, that is, any communication to the AD7739 must start with a write to the communications register specifying which register is subsequently read or written.

COMMUNICATIONS REGISTER

8 Bits, Write-Only Register, Address 0x00

All communications to the part must start with a write operation to the communications register (see Table 14 and Table 15). The data written to the communications register determines whether the subsequent operation is a read or write and to which register this operation is directed. The digital interface defaults to expect a write operation to the communications register after power-on, after reset, or after the subsequent read or write operation to the selected register is complete. If the interface sequence is lost, the part can be reset by writing at least 32 serial clock cycles with DIN high and $\overline{CS}$ low. (Note that all of the parts, including the modulator, filter, interface, and all registers are reset in this case.) Remember to keep DIN low while reading 32 bits or more either in continuous read mode or with the dump bit and 24/16 bit in the mode register set.

Table 14. Communications Register Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	0	R/$\overline{W}$	6-bit register address					

Table 15. Communications Register Bit Descriptions

Bit	Mnemonic	Description
7	0	This bit must be 0 for proper operation.
6	R/$\overline{W}$	A 0 in this bit indicates that the next operation is a write to a specified register. A 1 in this bit indicates that the next operation is a read from a specified register.
5 to 0	Address	These bits specify to which register the read or write operation is directed. For channel specific registers, the three LSBs, that is, Bit 2, Bit 1, and Bit 0, specify the channel number. When the subsequent operation writes to the mode register, the three LSBs specify the channel selected for the operation determined by the mode register value. The analog inputs configuration depends on the COM1 and COM0 bits in the channel setup register.

Bit 2	Bit 1	Bit 0	Channel	Single Input	Differential Input
0	0	0	0	AIN0 to AINCOM	AIN0 to AIN1
0	0	1	1	AIN1 to AINCOM	AIN2 to AIN3
0	1	0	2	AIN2 to AINCOM	AIN4 to AIN5
0	1	1	3	AIN3 to AINCOM	AIN6 to AIN7
1	0	0	4	AIN4 to AINCOM	AIN0 to AIN1
1	0	1	5	AIN5 to AINCOM	AIN2 to AIN3
1	1	0	6	AIN6 to AINCOM	AIN4 to AIN5
1	1	1	7	AIN7 to AINCOM	AIN6 to AIN7

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I/O PORT REGISTER

8 Bits, Read/Write Register, Address 0x01, Default Value 0x30 + Digital Input Value × 0x40

The bits in this register are used to configure and access the digital I/O port on the AD7739 (see Table 16 and Table 17).

REVISION REGISTER

8 Bits, Read-Only Register, Address 0x02, Default Value 0x09 + Chip Revision × 0x10

This register contains the 4-bit revision code and the 4-bit generic code for the ADC (see Table 18 and Table 19). This register can be used to correctly identify the ADC, or as a check to ensure that serial communication is working correctly.

TEST REGISTER

24 Bits, Read/Write Register, Address 0x03

This register is used for testing the part in the manufacturing process. The user must not change the default configuration of this register.

ADC STATUS REGISTER

8 Bits, Read-Only Register, Address 0x04, Default Value 0x00

In conversion modes, the register bits reflect the individual channel status. When a conversion is complete, the corresponding channel data register is updated and the corresponding RDY bit is set to 1. When the channel data register is read, the corresponding bit is reset to 0. The bit is reset to 0 also when no read operation has taken place and the result of the next conversion is being updated to the channel data register. Writing to the mode register resets all the bits to 0.

In calibration modes, all the register bits are reset to 0 while a calibration is in progress; all the register bits are set to 1 when the calibration is complete.

The $\overline{\text{RDY}}$ pin output is related to the content of the ADC status register as defined by the RDYFN bit in the I/O port register. The RDY0 bit corresponds to Channel 0, the RDY1 bit corresponds to Channel 1, and so on (see Table 20).

Table 16. I/O Port Register Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	P0	P1	P0 DIR	P1 DIR	RDYFN	REDPWR	0	Sync
Default	P0 pin	P1 pin	1	1	0	0	0	0

Table 17. I/O Port Register Bit Descriptions

Bit	Mnemonic	Description
7, 6	P0, P1	When the P0 and P1 pins are configured as outputs, the P0 and P1 bits determine the output level of the pin. When the P0 and P1 pins are configured as inputs, the P0 and P1 bits reflect the current input level on the pins.
5, 4	P0 DIR, P1 DIR	These bits determine whether the P0 and P1 pins are configured as inputs or outputs. When set to 1, the corresponding pin is an input; when reset to 0, the corresponding pin is an output.
3	RDYFN	This bit is used to control the function of the $\overline{\text{RDY}}$ pin on the AD7739. When this bit is reset to 0, the $\overline{\text{RDY}}$ pin goes low when any channel has unread data. When this bit is set to 1, the $\overline{\text{RDY}}$ pin goes low only if all enabled channels have unread data.
2	REDPWR	Reduced power. If this bit is set to 1, the AD7739 works in the reduced power mode. The maximum MCLK frequency is limited to 4 MHz in the reduced power mode.
1	0	This bit must be 0 for proper operation.
0	Sync	This bit enables the $\overline{\text{SYNC}}$ pin function. By default, this bit is 0 and $\overline{\text{SYNC}}$/P1 can be used as a digital I/O pin. When the sync bit is set to 1, the $\overline{\text{SYNC}}$ pin can be used to synchronize the AD7739 modulator and digital filter with other devices in the system.

Table 18. Revision Register Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	Chip revision code				Chip generic code			
Default	X	X	X	X	1	0	0	1

Table 19. Revision Register Bit Descriptions

Bit	Mnemonic	Description
7 to 4	Chip revision code	4-bit factory chip revision code
3 to 0	Chip generic code	On the AD7739, these bits read back as 0x09.

Table 20. ADC Status Register Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
Default	0	0	0	0	0	0	0	0

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CHECKSUM REGISTER

16 Bits, Read/Write Register, Address 0x05

This register is described in the AN-626 Application Note, *Using the AD7732/AD7734/ AD7738/AD7739 Checksum Register*.

ADC ZERO-SCALE CALIBRATION REGISTER

24 Bits, Read/Write Register, Address 0x06, Default Value 0x80 0000

This register holds the ADC zero-scale calibration coefficient. The value in this register is used in conjunction with the value in the ADC full-scale calibration register and the corresponding channel zero-scale and channel full-scale calibration registers to scale digitally the conversion results of all channels. The value in this register is updated automatically following the execution of an ADC zero-scale self-calibration. Writing this register is possible in the idle mode only (see the Calibration section for details).

ADC FULL-SCALE CALIBRATION REGISTER

24 Bits, Read/Write Register, Address 0x07, Default Value 0x80 0000

This register holds the ADC full-scale calibration coefficient. The value in this register is used in conjunction with the value in the ADC zero-scale and the corresponding channel zero-scale and channel full-scale calibration registers to scale digitally the conversion results of all channels. The value in this register is updated automatically following the execution of an ADC full-scale self-calibration. Writing this register is possible in the idle mode only. Use the ADC full-scale self-calibration only on +2.5 V and ±2.5 V input voltage ranges (see the Calibration section for details).

CHANNEL DATA REGISTERS

16-Bit/24-Bit, Read-Only Registers, Address 0x08 to Address 0x0F, Default Width 16 Bits, Default Value 0x8000

These registers contain the most up-to-date conversion results corresponding to each analog input channel. The 16-bit or 24-bit data width can be configured by setting the 24/16 bit in the mode register. The relevant RDY bit in the channel status register goes high when the result is updated. The RDY bit returns low once the data register reading begins. The $\overline{\text{RDY}}$ pin can be configured to indicate when any channel has unread data or to wait until all enabled channels have unread data. If any channel data register read operation is in progress when a new result is updated, no update of the data register occurs. This avoids having corrupted data. Reading the status registers can be associated with reading the data registers in the dump mode. Reading the status registers is always associated with reading the data registers in the continuous read mode (see the Digital Interface Description section for details).

CHANNEL ZERO-SCALE CALIBRATION REGISTERS

24 Bits, Read/Write Registers, Address 0x10 to Address 0x17, Default Value 0x80 0000

These registers hold the particular channel zero-scale calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding channel full-scale calibration register, the ADC zero-scale calibration register, and the ADC full-scale calibration register to digitally scale the particular channel conversion results. The value in this register is updated automatically following the execution of a channel zero-scale system calibration.

The format of the channel zero-scale calibration register is a sign bit and a 22-bit unsigned value. Writing this register is possible in the idle mode only (see the Calibration section for details).

CHANNEL FULL-SCALE CALIBRATION REGISTERS

24 Bits, Read/Write Registers, Address 0x18 to Address 0x1F, Default Value 0x20 0000

These registers hold the particular channel full-scale calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding channel zero-scale calibration register, the ADC zero-scale calibration register, and the ADC full-scale calibration register to digitally scale the particular channel conversion results. The value in this register is updated automatically following the execution of a channel full-scale system calibration. Writing this register is possible in the idle mode only (see the Calibration section for details).

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CHANNEL STATUS REGISTERS

8 Bits, Read-Only Registers, Address 0x20 to Address 0x27, Default Value 0x20 × Channel Number

These registers contain individual channel status information and some general AD7739 status information (see Table 21 and Table 22). Reading the status registers can be associated with reading the data registers in the dump mode. Reading the status registers is always associated with reading the data registers in the continuous read mode (see the Digital Interface Description section for details).

Table 21. Channel Status Registers Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CH2	CH1	CH0	0/P0	RDY/P1	NOREF	Sign	OVR
Default	Channel number			0	0	0	0	0

Table 22. Channel Status Registers Bit Descriptions

Bit	Mnemonic	Description
7 to 5	CH2 to CH0	These bits reflect the channel number. This can be used for current channel identification and easier operation of the dump mode and continuous read mode.
4	0/P0	When the status option bit of the corresponding channel setup register is reset to 0, this bit is read as a 0. When the status option bit is set to 1, this bit reflects the state of the P0 pin, whether it is configured as an input or an output.
3	RDY/P1	When the status option bit of the corresponding channel setup register is reset to 0, this bit reflects the selected channel RDY bit in the ADC status register. When the status option bit is set to 1, this bit reflects the state of the P1 pin, whether it is configured as an input or an output.
2	NOREF	This bit indicates the reference input status. If the voltage between the REFIN(+) and REFIN(−) pins is less than NOREF, the trigger voltage, and a conversion is executed, then the NOREF bit goes to 1.
1	Sign	This bit reflects the voltage polarity at the analog input. It is 0 for a positive voltage and 1 for a negative voltage.
0	OVR	This bit reflects either the overrange or the underrange on the analog input. The bit is set to 1 when the analog input voltage goes over or under the nominal voltage range (see the Extended Voltage Range of the Analog Input section).

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CHANNEL SETUP REGISTERS

8 Bits, Read/Write Registers, Address 0x28 to Address 0x2F, Default Value 0x00

These registers are used to configure the selected channel, to configure its input voltage range, and to set up the corresponding channel status register (see Table 23 and Table 24).

Table 23. Channel Setup Registers Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	BUFOFF	COM1	COM0	Stat OPT	Enable	RNG2	RNG1	RNG0
Default	0	0	0	0	0	0	0	0

Table 24. Channel Setup Registers Bit Descriptions

Bit	Mnemonic	Description				
7	BUFOFF	Buffer off. If reset to 0, then the internal buffer is enabled. Operation only with the internal buffer enabled is recommended.				
6 to 5	COM1, COM0	Analog inputs configuration.				
		Channel	**COM1 0**	**COM0 0**	**COM1 1**	**COM0 1**
		0	AIN0 to AINCOM		AIN0 to AIN1	
		1	AIN1 to AINCOM		AIN2 to AIN3	
		2	AIN2 to AINCOM		AIN4 to AIN5	
		3	AIN3 to AINCOM		AIN6 to AIN7	
		4	AIN4 to AINCOM		AIN0 to AIN1	
		5	AIN5 to AINCOM		AIN2 to AIN3	
		6	AIN6 to AINCOM		AIN4 to AIN5	
		7	AIN7 to AINCOM		AIN6 to AIN7	
4	Stat OPT	Status option. When this bit is set to 1, the P0 and P1 bits in the channel status register reflect the state of the P0 and P1 pins. When this bit is reset to 0, the RDY bit in the channel status register reflect the channel corresponding to the RDY bit in the ADC status register.				
3	Enable	Channel enable. Set this bit to 1 to enable the channel in the continuous conversion mode. A single conversion takes place regardless of the value of this bit.				
2 to 0	RNG2 to RNG0	This is the channel input voltage range.				
		RNG2	**RNG1**	**RNG0**	**Nominal Input Voltage Range**	
		1	0	0	±2.5 V	
		1	0	1	+2.5 V	
		0	0	0	±1.25 V	
		0	0	1	+1.25 V	
		0	1	0	±0.625 V	
		0	1	1	+0.625 V	

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CHANNEL CONVERSION TIME REGISTERS

8 Bits, Read/Write Registers, Address 0x30 to Address 0x37, Default Value 0x91

The conversion time registers enable or disable chopping and configure the digital filter for a particular channel (see Table 25 and Table 26). This register value affects the conversion time, frequency response, and noise performance of the ADC.

MODE REGISTER

8 Bits, Read/Write Register, Address 0x38 to Address 0x3F, Default Value 0x00

The mode register configures the part and determines its operating mode (see Table 27, Table 28, and Table 29). Writing to the mode register clears the ADC status register, sets the $\overline{\text{RDY}}$ pin to a logic high level, exits all current operations, and starts the mode specified by the mode bits.

The AD7739 contains only one mode register. The two LSBs of the address are used for writing to the mode register to specify the channel selected for the operation determined by the MD2 to MD0 bits. Only the address 0x38 must be used for reading from the mode register.

Table 25. Channel Conversion Time Registers Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	Chop	FW (7-bit filter word)						
Default	1	0x11						

Table 26. Channel Conversion Time Registers Bit Descriptions

Bit	Mnemonic	Description
7	Chop	Chopping enable bit. Set to 1 to apply chopping mode for a particular channel.
6 to 0	FW	Chop = 1, single conversion or continuous conversion with one channel enabled. Conversion Time (μs) = (FW × 128 + 262)/MCLK Frequency (MHz), the FW range is 2 to 127. Chop = 1, continuous conversion with two or more channels enabled. Conversion Time (μs) = (FW × 128 + 263)/MCLK Frequency (MHz), the FW range is 2 to 127. Chop = 0, single conversion or continuous conversion with one channel enabled. Conversion Time (μs) = (FW × 64 + 213)/MCLK Frequency (MHz), the FW range is 3 to 127. Chop = 0, continuous conversion with two or more channels enabled. Conversion Time (μs) = (FW × 64 + 214)/MCLK Frequency (MHz), the FW range is 3 to 127.

Table 27. Mode Register Bits

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	MD2	MD1	MD0	CLKDIS	Dump	Cont RD	24/16 BIT	Clamp
Default	0	0	0	0	0	0	0	0

Table 28. Mode Register Bit Descriptions

Bit	Mnemonic	Description				
7 to 5	MD2 to MD0	Mode bits. These three bits determine the AD7739 operation mode. Writing a new value to the mode bits exit the part from the mode in which it has been operating and place it in the newly requested mode immediately. The function of the mode bits follows.				
		MD2	**MD1**	**MD0**	**Mode**	**Address Used for Mode Register Write Specifies**
		0	0	0	Idle	
		0	0	1	Continuous conversion	First channel to start converting
		0	1	0	Single conversion	Channel to convert
		0	1	1	Power-down (standby)	
		1	0	0	ADC zero-scale self-calibration	Conversion time for calibration
		1	0	1	ADC full-scale self-calibration (for 2.5 V)	Conversion time for calibration
		1	1	0	Channel zero-scale system calibration	Channel to calibrate
		1	1	1	Channel full-scale system calibration	Channel to calibrate

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Bit	Mnemonic	Description
4	CLKDIS	Master clock output disable. When this bit is set to 1, the master clock is disabled from appearing at the MCLKOUT pin and the MCLKOUT pin is in a high impedance state. This allows turning off the MCLKOUT as a power saving feature. When using an external clock on MCLKIN, the AD7739 continues to have internal clocks and converts normally regardless of the CLKDIS bit state. When using a crystal oscillator or ceramic resonator across the MCLKIN and MCLKOUT pins, the AD7739 clock is stopped and no conversions can take place when the CLKDIS bit is active. The AD7739 digital interface can still be accessed using the SCLK pin.
3	Dump	Dump mode. When this bit is reset to 0, the channel status register and channel data register are addressed and read separately. When the dump bit is set to 1, the channel status register is followed immediately by a read of the channel data register regardless of whether the status or data register has been addressed through the communications register. The continuous read mode is always dump mode reading the channel status and channel data registers, regardless of the dump bit value (see the Digital Interface Description section for details).
2	Cont RD	When this bit is set to 1, the AD7739 operates in the continuous read mode (see the Digital Interface Description section for details).
1	24/16 bit	Channel data register data width selection bit. When set to 1, the channel data registers are 24 bits wide. When set to 0, the channel data registers is 16 bits wide.
0	Clamp	This bit determines the value of the channel data register when the analog input voltage is outside the nominal input voltage range. When the clamp bit is set to 1, the channel data register is digitally clamped to either all 0s or all 1s when the analog input voltage goes outside the nominal input voltage range. When the clamp bit is reset to 0, the data registers reflect the analog input voltage even outside the nominal voltage range (see the Extended Voltage Range of the Analog Input section).

Table 29. Mode Settings

MD2	MD1	MD0	Operating Mode	Description
0	0	0	Idle	The default mode after power-on or reset. The AD7739 automatically returns to this mode after any calibration or after a single conversion.
0	0	1	Continuous conversion	The AD7739 performs a conversion on the specified channel. After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7739 continues converting on the next enabled channel. The part cycles through all enabled channels until it is put into another mode or reset. The cycle period is the sum of all enabled channels' conversion times, set by the corresponding channel conversion time registers.
0	1	0	Single conversion	The AD7739 performs a conversion on the specified channel. After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, the $\overline{RDY}$ pin goes low, the MD2 to MD0 bits are reset, and the AD7739 returns to idle mode. Requesting a single conversion ignores the channel setup register enable bits; a conversion is performed even if that channel is disabled.
0	1	1	Power-down (standby)	The ADC and the analog front end (internal buffer) go into the power-down mode. The AD7739 digital interface can still be accessed. The CLKDIS bit works separately, and the MCLKOUT mode is not affected by the power-down (standby) mode.
1	0	0	ADC zero-scale self-calibration	A zero-scale self-calibration is performed on internally shorted ADC inputs. After the calibration is complete, the contents of the ADC zero-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2 to MD0 bits are reset, and the AD7739 returns to idle mode.
1	0	1	ADC full-scale self-calibration	A full-scale self-calibration is performed on an internally generated full-scale signal. After the calibration is complete, the contents of the ADC full-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2 to MD0 bits are reset, and the AD7739 returns to idle mode.
1	1	0	Channel zero-scale system calibration	A zero-scale system calibration is performed on the selected channel. An external system zero-scale voltage must be provided at the AD7739 analog input and this voltage must remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding channel zero-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2 to MD0 bits are reset, and the AD7739 returns to idle mode.
1	1	1	Channel full-scale system calibration	A full-scale system calibration is performed on the selected channel. An external system full-scale voltage must be provided at the AD7739 analog input and this voltage must remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding channel full-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2 to MD0 bits are reset, and the AD7739 returns to idle mode.

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DIGITAL INTERFACE DESCRIPTION

HARDWARE

The AD7739 serial interface can be connected to the host device via the serial interface in several different ways.

The $\overline{CS}$ pin can be used to select the AD7739 as one of several circuits connected to the host serial interface. When $\overline{CS}$ is high, the AD7739 ignores the SCLK and DIN signals and the DOUT pin goes to the high impedance state. When the $\overline{CS}$ signal is not used, connect the $\overline{CS}$ pin to DGND.

The $\overline{RDY}$ pin can be polled for high-to-low transition or can drive the host device interrupt input to indicate that the AD7739 has finished the selected operation and/or new data from the AD7739 is available. The host system can also wait a designated time after a given command is written to the device before reading. Alternatively, the AD7739 status can be polled. When the $\overline{RDY}$ pin is not used in the system, leave it as an open circuit. (Note that the $\overline{RDY}$ pin is always an active digital output, that is, it never goes into a high impedance state.)

The $\overline{RESET}$ pin can be used to reset the AD7739. When not used, connect this pin to DV_{DD}.

The AD7739 interface can be reduced to just two wires connecting the DIN and DOUT pins to a single bidirectional data line. The second signal in this 2-wire configuration is the SCLK signal. The host system must change the data line direction with reference to the AD7739 timing specification (see the Bus Relinquish Time in Table 2). The AD7739 cannot operate in the continuous read mode in 2-wire serial interface configuration.

All the digital interface inputs are Schmitt triggered; therefore, the AD7739 interface features higher noise immunity and can be easily isolated from the host system via optocouplers. Figure 12, Figure 13, and Figure 14 outline some of the possible host device interfaces: SPI without using the $\overline{CS}$ signal (Figure 12), a DSP interface (Figure 13), and a 2-wire configuration (Figure 14).

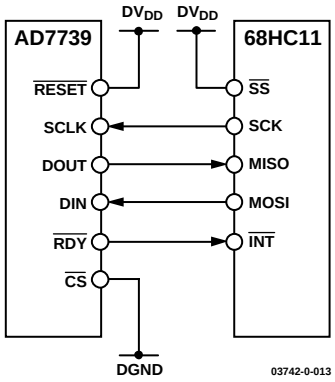

Figure 12. AD7739 to Host Device Interface, SPI

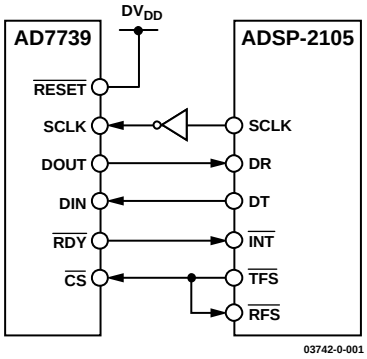

Figure 13. AD7739 to Host Device Interface, DSP

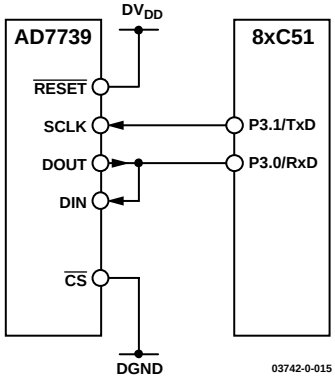

Figure 14. AD7739 to Host Device Interface, 2-Wire Configuration

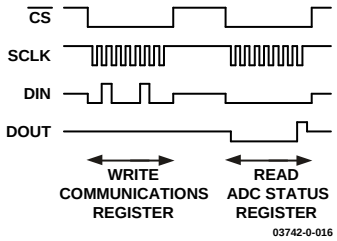

Figure 15. Serial Interface Signals—Registers Access

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RESET

The AD7739 can be reset by the $\overline{\text{RESET}}$ pin or by writing a reset sequence to the AD7739 serial interface. The reset sequence is N × 0 + 32 × 1, which can be the data sequence 0x00 + 0xFF + 0xFF + 0xFF + 0xFF in a byte-oriented interface.

The AD7739 also features a power-on reset with a trip point of 2 V and goes to the defined default state after power-on.

It is the responsibility of the system designer to prevent an unwanted write operation to the AD7739. The unwanted write operation can happen when a spurious clock appears on the SCLK while the $\overline{\text{CS}}$ pin is low. Note that if the AD7739 interface signals are floating or undefined at system power-on, the part can be inadvertently configured into an unknown state. This can be easily overcome by initiating either a hardware reset event or a 32 ones reset sequence as the first step in the system configuration.

ACCESS THE AD7739 REGISTERS

All communications to the part start with a write operation to the communications register followed by either reading or writing the addressed register. In a simultaneous read-write interface (such as SPI), write 0 to the AD7739 while reading data.

Figure 15 shows the AD7739 interface read sequence for the ADC status register.

SINGLE CONVERSION AND READING DATA

When the mode register is being written, the ADC status byte is cleared and the $\overline{\text{RDY}}$ pin goes high, regardless of its previous state. When the single conversion command is written to the mode register, the ADC starts the conversion on the channel selected by the address of the mode register. After the conversion is completed, the data register is updated, the mode register is changed to idle mode, the relevant RDY bit is set, and the $\overline{\text{RDY}}$ pin goes low. The RDY bit is reset and the $\overline{\text{RDY}}$ pin returns high when the relevant channel data register is being read.

Figure 16 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{\text{RDY}}$ pin to go low, and reading the Channel 0 data register.

DUMP MODE

When the dump bit in the mode register is set to 1, the channel status register is read immediately by a read of the channel data register, regardless of whether the status or the data register is addressed through the communications register. The DIN pin must not be high while reading 24-bit data in dump mode; otherwise, the AD7739 is reset.

Figure 17 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{\text{RDY}}$ pin to go low, and reading the Channel 0 status register and data register in the dump mode.

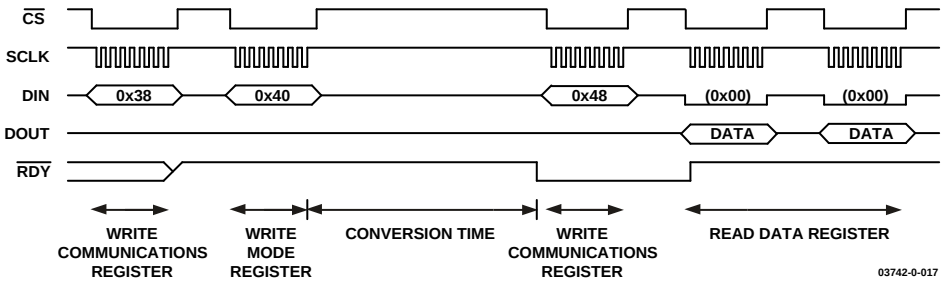

Figure 16. Serial Interface Signals—Single Conversion Command and 16-Bit Data Reading

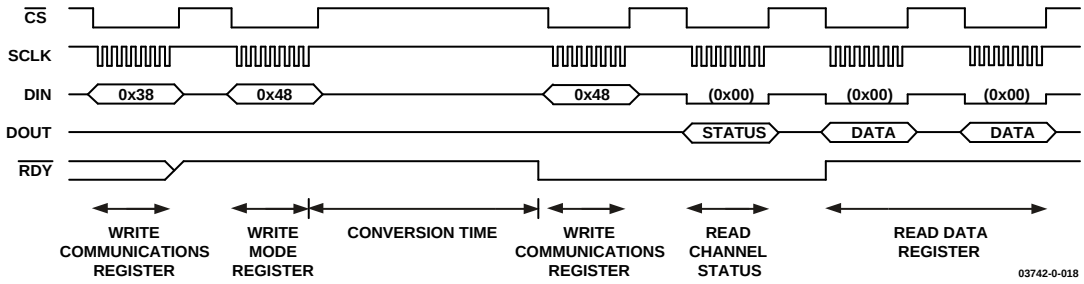

Figure 17. Serial Interface Signals—Single Conversion Command, 16-Bit Data Reading, Dump Mode

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CONTINUOUS CONVERSION MODE

When the mode register is being written, the ADC status byte is cleared and the $\overline{RDY}$ pin goes high, regardless of its previous state. When the continuous conversion command is written to the mode register, the ADC starts conversion on the channel selected by the address of the mode register.

After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7739 continues converting on the next enabled channel. The part cycles through all enabled channels until put into another mode or reset. The cycle period is the sum of all conversion times of enabled channels, set by the corresponding channel conversion time registers.

The RDY bit is reset when the relevant channel data register is being read. The behavior of the $\overline{RDY}$ pin depends on the RDYFN bit in the I/O port register. When the RDYFN bit is 0, the $\overline{RDY}$ pin goes low when any channel has unread data. When the RDYFN bit is set to 1, the $\overline{RDY}$ pin goes low only if all enabled channels have unread data.

If an ADC conversion result is not read before a new ADC conversion is completed, the new result overwrites the previous one. The relevant RDY bit goes low and the $\overline{RDY}$ pin goes high for at least 163 MCLK cycles (~26.5 µs), indicating when the data register is updated, and the previous conversion data is lost.

If the data register is being read as an ADC conversion completes, the data register is not updated with the new result (to avoid data corruption) and the new conversion data is lost.

Figure 18 shows the sequence of the digital interface signal for the continuous conversion mode with Channels 0 and 1 enabled and the RDYFN bit set to 0. The $\overline{RDY}$ pin goes low and the data register is read after each conversion. Figure 19 shows a similar sequence but with the RDYFN bit set to 1. The $\overline{RDY}$ pin goes low and all data registers are read after all conversions are completed. Figure 20 shows the $\overline{RDY}$ pin when no data is read from the AD7739.

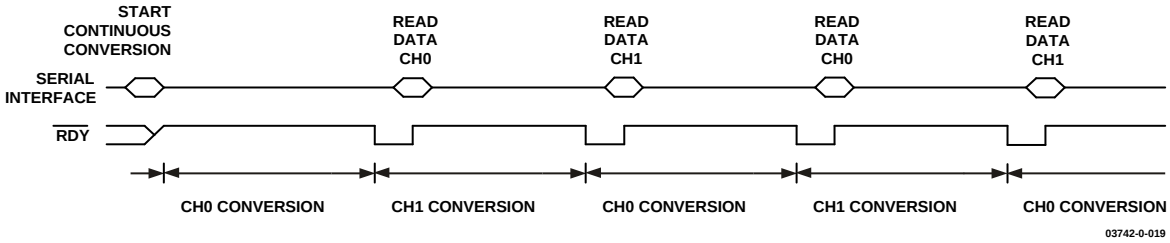

Figure 18. Continuous Conversion, CH0 and CH1, RDYFN = 0

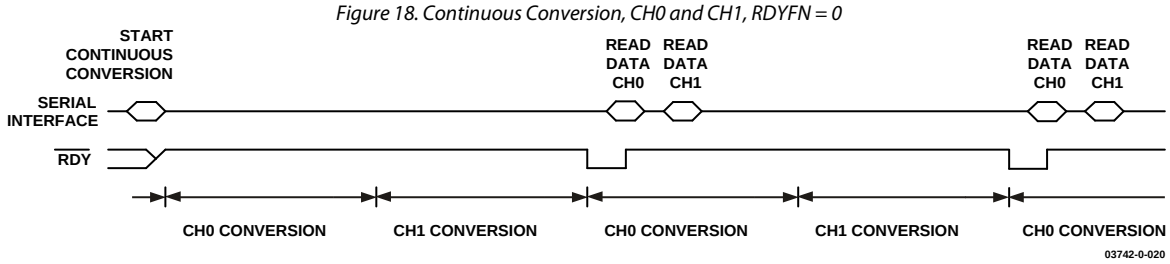

Figure 19. Continuous Conversion, CH0 and CH1, RDYFN = 1

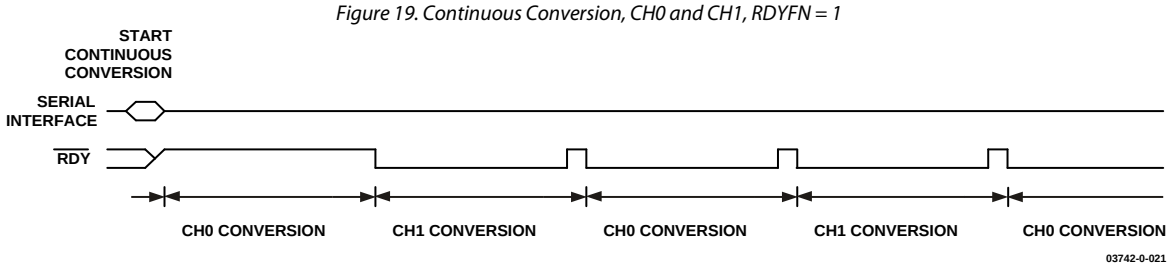

Figure 20. Continuous Conversion, CH0 and CH1, No Data Read

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CONTINUOUS READ (CONTINUOUS CONVERSION) MODE

When the Cont RD bit in the mode register is set, the first write of 0x48 to the communications register starts the continuous read mode. As shown in Figure 21, subsequent accesses to the part sequentially read the channel status and data registers of the last completed conversion without any further configuration of the communications register being required.

Note that the continuous conversion bit in the mode register must be set when entering the continuous read mode.

Note that the continuous read mode is a dump mode reading of the channel status and data registers regardless of the dump bit value. Use the channel bits in the channel status register to check/recognize which channel data is actually being shifted out.

Note that the last completed conversion result is being read. Therefore, the RDYFN bit in the I/O port register must be 0, and reading the result must always start before the next conversion is completed.

The AD7739 stays in continuous read mode as long as the DIN pin is low while the $\overline{CS}$ pin is low; therefore, write 0 to the AD7739 while reading in continuous read mode. To exit continuous read mode, take the DIN pin high for at least 100 ns after a read is complete. (Write 0x80 to the AD7739 to exit continuous reading.)

Taking the DIN pin high does not change the Cont RD bit in the mode register. Therefore, the next write of 0x48 starts the continuous read mode again. To completely stop the continuous read mode, write to the mode register to clear the Cont RD bit.

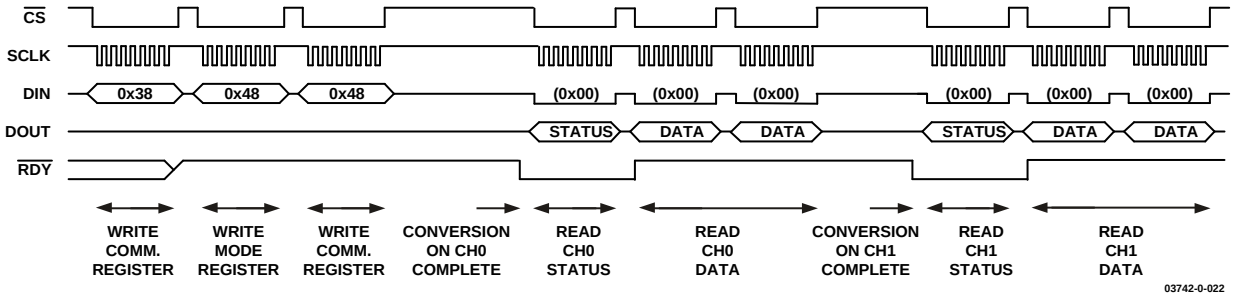

Figure 21. Continuous Conversion, CH0 and CH1, Continuous Read

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CIRCUIT DESCRIPTION

The AD7739 is a high precision analog-to-digital converter that is intended for the measurement of wide dynamic range, low frequency signals in industrial process control, instrumentation, and PLC systems.

It contains a multiplexer, an input buffer, a Σ-Δ (or charge balancing) ADC, a digital filter, a clock oscillator, a digital I/O port, and a serial communications interface.

ANALOG INPUTS

The AD7739 has nine analog input pins connected to the ADC through the internal multiplexer. The analog front end can be configured as eight single-ended inputs or four differential inputs or any combination of these (via the channel setup registers).

The AD7739 contains a wide bandwidth, fast settling time differential input buffer capable of driving the dynamic load of a high speed Σ-Δ modulator. With the internal buffer enabled, the analog inputs feature high input impedance.

If chopping is enabled or when switching between channels, there is a dynamic current on analog inputs charging the internal capacitance of the multiplexer and input buffer. The capacitance is approximately 10 pF.

At the start of each conversion, there is a delay to allow the capacitance to be charged (see the Multiplexer, Conversion, and Data Output Timing section). If the analog inputs resistive source impedance does not exceed 50 kΩ, the internal capacitance is charged fast enough and the AD7739 performance is not affected at the 16-bit level.

An external RC filter connected to the analog inputs averages the multiplexer channel-to-channel switching dynamic currents to a dc current leading to a dc voltage drop across the external input resistance. To avoid additional gain errors, offset errors, and channel-to-channel crosstalk due to this effect, use low resistor values in the low-pass RC filter for the AD7739. The recommended low-pass RC filter for the analog inputs is 100 Ω and 100 nF.

The average (dc) current, charging the capacitance on the multiplexer output, is related to the equation:

$$I \approx C_{MUX} \times V_{MUX} \times f_S$$

where:
C_{MUX} is the capacitance on the multiplexer output, approximately 10 pF.
V_{MUX} is the voltage difference on the multiplexer output between two subsequent conversions, which can be up to 5 V.
f_S is the channel sampling frequency, which relates to the sum of conversion times on all subsequently sampled channels.

SIGMA-DELTA ADC

The AD7739 core consists of a charge balancing Σ-Δ modulator and a digital filter. The architecture is optimized for fast, fully settled conversion. This allows for fast channel-to-channel switching while maintaining inherently excellent linearity, high resolution, and low noise.

CHOPPING

With chopping enabled, the multiplexer repeatedly reverses the ADC inputs. Every output data result is then calculated as an average of two conversions, the first with the positive and the second with the negative offset term included. This effectively removes any offset error of the input buffer and Σ-Δ modulator. Figure 22 shows the channel signal chain with chopping enabled.

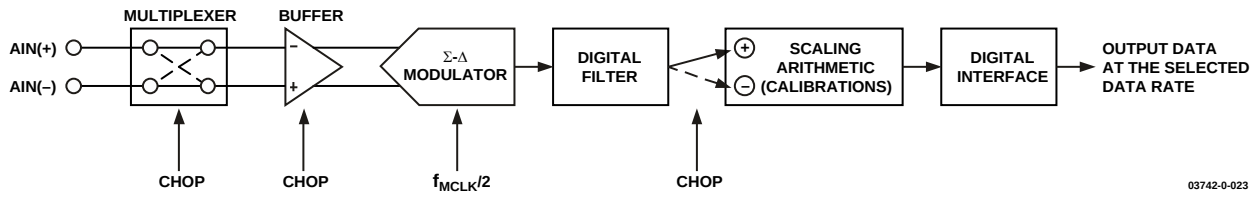

Figure 22. Channel Signal Chain Diagram with Chopping Enabled

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MULTIPLEXER, CONVERSION, AND DATA OUTPUT TIMING

The specified conversion time includes one or two settling and sampling periods and a scaling time.

With chopping enabled (Figure 23), a conversion cycle starts with a settling time of 43 MCLK cycles or 44 MCLK cycles (~7 µs with a 6.144 MHz MCLK) to allow the circuits following the multiplexer to settle. The Σ-Δ modulator then samples the analog signals and the digital filter processes the digital data stream. The sampling time depends on FW, that is, on the channel conversion time register contents. After another settling of 42 MCLK cycles (~6.8 µs), the sampling time is repeated with a reversed (chopped) analog input signal. Then, during the scaling time of 163 MCLK cycles (~26.5 µs), the two results from the digital filter are averaged, scaled using the calibration registers, and written into the channel data register.

With chopping disabled (Figure 24), only one sampling time is preceded by a settling time of 43 MCLK or 44 MCLK cycles and followed by a scaling time of 163 MCLK cycles.

The $\overline{\text{RDY}}$ pin goes high during the scaling time, regardless of its previous state. The relevant RDY bit is set in the ADC status register and in the channel status register, and the $\overline{\text{RDY}}$ pin goes low when the channel data register is updated and the channel conversion cycle is finished. If in continuous conversion mode, the part automatically continues with a conversion cycle on the next enabled channel.

Note that every channel can be configured independently for conversion time and chopping mode. The overall cycle and effective per channel data rates depend on all enabled channel settings.

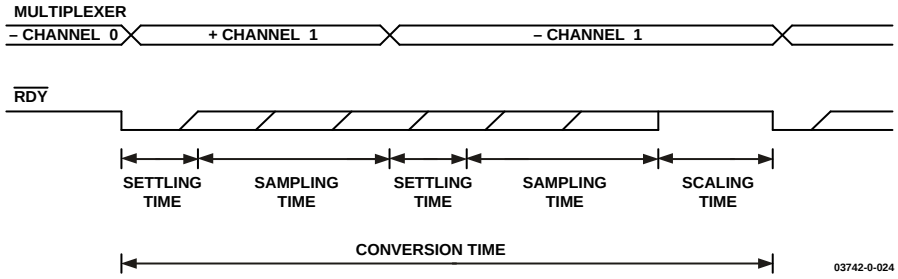

Figure 23. Multiplexer and Conversion Timing—Continuous Conversion on Several Channels with Chopping Enabled

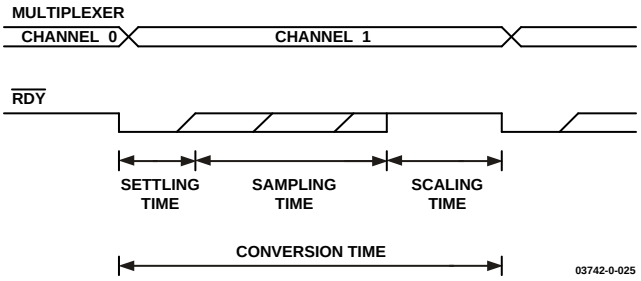

Figure 24. Multiplexer and Conversion Timing—Continuous Conversion on Several Channels with Chopping Disabled

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FREQUENCY RESPONSE

The Σ-Δ modulator runs at ½ the MCLK frequency, which is effectively the sampling frequency. Therefore, the modulator Nyquist frequency is ¼ of the MCLK.

If chopping is enabled, the input signal is resampled by chopping. Therefore, the overall frequency response features notches close to the frequency of 1/channel conversion time.

The typical ADC frequency response plots are given in Figure 25 and Figure 26. The plots are normalized to 1/channel conversion time.

Note that these figures apply to each channel separately and are based on individual channel conversion time. The signal is effectively resampled once more in the multiplexer by switching between enabled analog inputs.

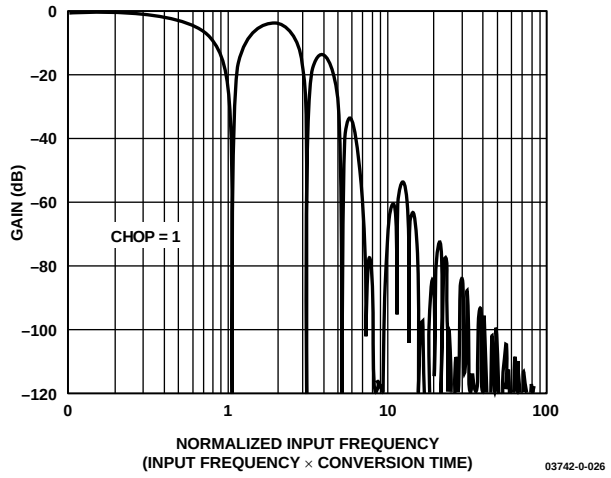

Figure 25. Typical ADC Frequency Response, Chopping Enabled

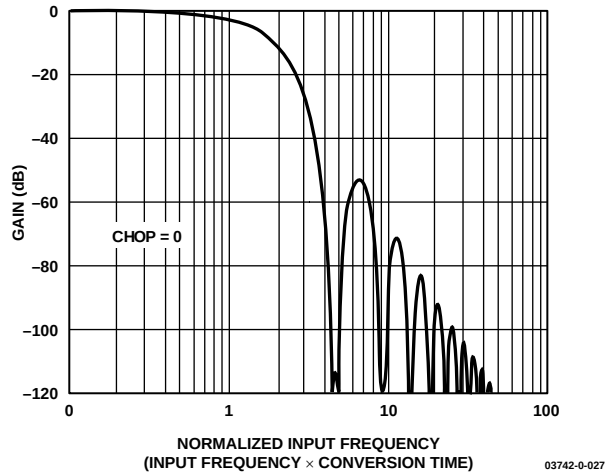

Figure 26. Typical ADC Frequency Response, Chopping Disabled

EXTENDED VOLTAGE RANGE OF THE ANALOG INPUT

The AD7739 output data code span corresponds to the nominal input voltage range. The ADC is functional outside the nominal input voltage range, but the performance might degrade. The Σ-Δ modulator was designed to fully cover 16% analog input overrange; outside this range, the performance might degrade more rapidly.

When the clamp bit in the mode register is set to 1, the channel data register is digitally clamped to either all 0s or all 1s when the analog input voltage goes outside the nominal input voltage range.

As shown in Table 30 and Table 31, when clamp = 0, the data reflects the analog input voltage outside the nominal voltage range. In this case, the sign and OVR bits in the channel status register must be considered along with the data register value to decode the actual conversion result.

Note that the OVR bit in the channel status register is generated digitally from the conversion result and indicates the Σ-Δ modulator (nominal) overrange. The OVR bit does not indicate exceeding the absolute voltage limits of the AIN pin.

Table 30. Extended Input Voltage Range, Nominal Voltage Range ±1.25 V, 16 Bits, Clamp = 0

Input (V)	Data (hex)	Sign	OVR
+1.45000	0x147B	0	1
+1.25008	0x0001	0	1
+1.25004	0x0000	0	1
+1.25000	0xFFFF	0	0
+0.00004	0x8001	0	0
0.00000	0x8000	0	0
−0.00004	0x7FFF	1	0
−1.25000	0x0000	1	0
−1.25004	0xFFFF	1	1
−1.25008	0xFFFE	1	1
−1.45000	0xEB85	1	1

Table 31. Extended Input Voltage Range, Nominal Voltage Range +1.25 V, 16 Bits, Clamp = 0

Input (V)	Data (hex)	Sign	OVR
+1.45000	0x28F5	0	1
+1.25004	0x0001	0	1
+1.25002	0x0000	0	1
+1.25000	0xFFFF	0	0
+0.00002	0x0001	0	0
+0.00000	0x0000	0	0
−0.00002	0x0000	1	1

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VOLTAGE REFERENCE INPUTS

The AD7739 has a differential reference input, REF IN(+) and REF IN(−). The common-mode range for these inputs is from AGND to AV_{DD}. The nominal differential reference voltage for specified operation is 2.5 V. Both reference inputs feature dynamic load. Therefore, connect the reference inputs to a low impedance reference voltage source. External resistance/capacitance combinations may result in gain errors on the part.

The output noise performance outlined in Table 5 through Table 10 is for an analog input of 0 V and is unaffected by noise on the reference. Obtaining the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7739. If the reference noise in the bandwidth of interest is excessive, it degrades the performance of the AD7739.

Recommended reference voltage sources for the AD7739 include the ADR431, ADR421, AD780, REF43, and REF192.

REFERENCE DETECT

The AD7739 includes on-chip circuitry to detect if the part has a valid reference for conversions. If the voltage between the REFIN(+) and REFIN(−) pins goes below the NOREF trigger voltage (0.5 V typ.) and the AD7739 is performing a conversion, the NOREF bit in the channel status register is set.

I/O PORT

The AD7739 P0 pin can be used as a general-purpose digital output or as a common analog input.

The P1 pin ($\overline{SYNC}$/P1) can be used as a general-purpose digital I/O pin or to synchronize the AD7739 with other devices in the system. When the sync bit in the I/O port register is set and the $\overline{SYNC}$ pin is low, the AD7739 does not process any conversion. If it is put into single conversion mode, continuous conversion mode, or any calibration mode, the AD7739 waits until the $\overline{SYNC}$ pin goes high and then starts operation. This allows conversion to start from a known point in time, that is, the rising edge of the $\overline{SYNC}$ pin. When configured as input, the $\overline{SYNC}$ pin must be tied high or low.

The digital P0 and P1 voltage is referenced to the analog supplies.

CALIBRATION

The AD7739 provides zero-scale self-calibration, and zero- and full-scale system calibration capability that can effectively reduce the offset error and gain error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC calibration registers and the relevant channel calibration registers before being written to the data register.

For unipolar ranges,

$$Data = ((ADC\ Result - R \times ADC\ ZS\ Calibration\ Register) \times ADC\ FS\ Register/(0x20\ 0000) - R \times Channel\ ZS\ Calibration\ Register) \times Channel\ FS\ Calibration\ Register/(0x20\ 0000)$$

For bipolar ranges,

$$Data = ((ADC\ Result - R \times ADC\ ZS\ Calibration\ Register) \times ADC\ FS\ Register/(0x40\ 0000) + (0x80\ 0000) - R \times Channel\ ZS\ Calibration\ Register) \times Channel\ FS\ Calibration\ Register/(0x20\ 0000)$$

where:
The *ADC Result* is in the range of 0 to 0xFF FFFF.
$R = 1$ for input ranges +1.25 V, ±1.25 V, +2.5 V, and ±2.5 V, and
$R = 2$ for input ranges +0.625 V, and ±0.625 V.

Note that the channel zero-scale calibration register has the format of a sign bit and a 22-bit channel offset value.

To start any calibration, write the relevant mode bits to the AD7739 mode register. After the calibration is complete, the contents of the corresponding calibration registers are updated, all RDY bits in the ADC status register are set, the $\overline{SYNC}$ pin goes low, and the AD7739 reverts to idle mode. The calibration duration is the same as the conversion time configured on the selected channel. A longer conversion time gives less noise and yields a more exact calibration; therefore, use at least the default conversion time to initiate any calibration.

ADC Zero-Scale Self-Calibration

The ADC zero-scale self-calibration can reduce the ADC offset error in the chopping disabled mode. If repeated after a temperature change, it can also reduce the offset drift error in the chopping disabled mode.

The zero-scale self-calibration is performed on internally shorted ADC inputs. The negative analog input terminal on the selected channel is used to set the ADC zero-scale calibration common mode. Therefore, either the negative terminal of the selected differential pair or the AINCOM on the single-ended channel configuration must be driven to a proper common-mode voltage.

It is recommended that the ADC zero-scale calibration register be updated only as part of an ADC zero-scale self-calibration.

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ADC Full-Scale Self-Calibration

The ADC full-scale self-calibration can reduce the ADC full-scale error for the +2.5 V and ±2.5 V input range. If repeated after a temperature change, it can also reduce the full-scale drift.

The ADC full-scale self-calibration is performed with a +2.5 V input voltage range on internally generated full-scale voltage (V_{REF}), regardless of the input voltage range set in the channel setup register. Full-scale errors in the ±1.25 V, +1.25 V, ±0.625 V, and +0.625 V ranges are not calibrated as this requires an accurate low voltage source other than the reference.

If the 1.25 V or 0.625 V ranges are used on any channel, the ADC full-scale self-calibration is not recommended. Perform a system full-scale calibration if accurate gains need to be achieved on these ranges.

It is recommended that the ADC full-scale calibration register be updated only as part of an ADC full-scale self-calibration for the +2.5 V and ±2.5 V input range.

Per Channel System Calibration

The per channel system calibration can reduce the system offset error and the system gain error. If repeated after a temperature change, it can also reduce the system offset and gain drifts.

If the per channel system calibrations are used, initiate these in the following order: a channel zero-scale system calibration, followed by a channel full-scale system calibration.

The system calibration is affected by the ADC zero-scale and full-scale calibration registers. Therefore, if both self-calibration and system calibration are used in the system, perform an ADC self-calibration first, followed by a system calibration cycle.

Set the voltage range in the channel setup register before executing the channel system calibration.

While executing a system calibration, the fully settled system zero-scale voltage signal or system full-scale voltage signal must be connected to the selected channel analog inputs.

The per channel calibration registers can be read, stored, or modified and written back to the AD7739. Note that when writing the calibration registers, the AD7739 must be in idle mode. Note that outside the specified calibration range, calibration is possible, but the performance may degrade (see the System Calibration section in Table 1).

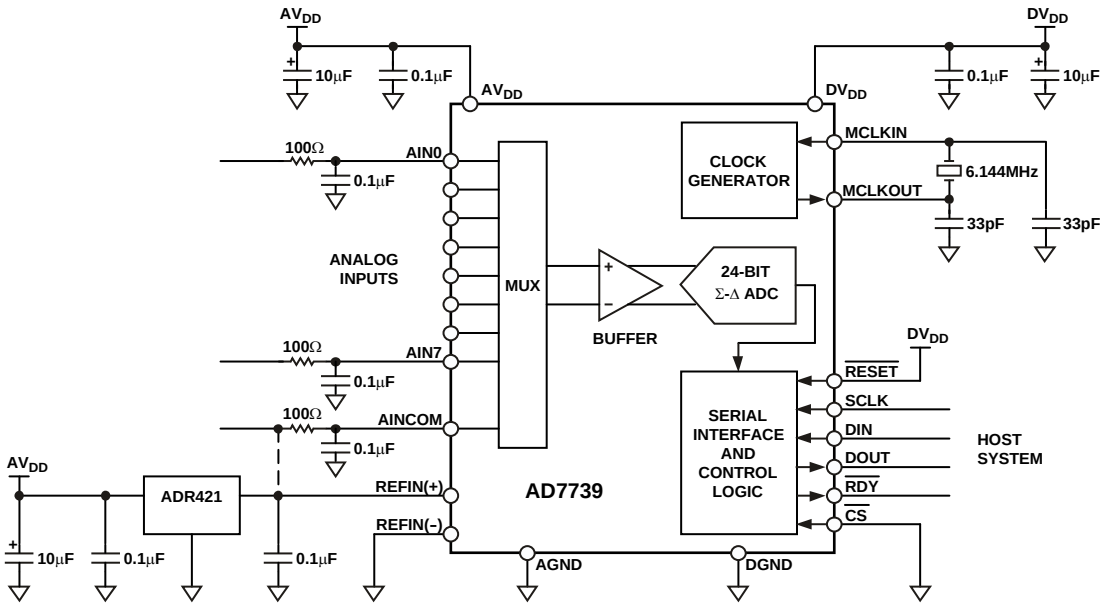

Figure 27. Typical Connections for the AD7739 Application

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OUTLINE DIMENSIONS

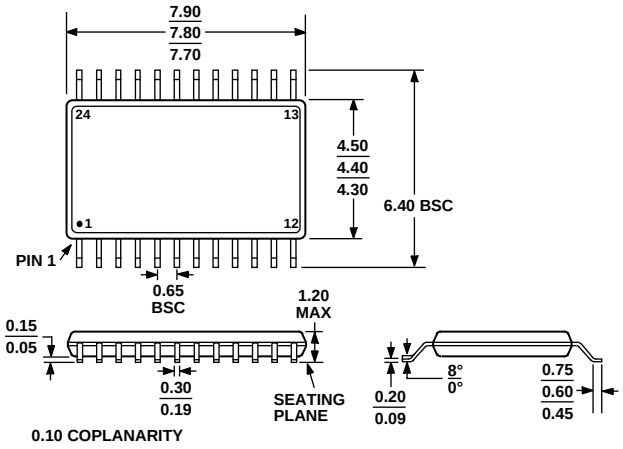

Figure 28. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Outline
AD7739BRU	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7739BRU-REEL	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7739BRUZ	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7739BRUZ-REEL7	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
EVAL-AD7739EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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