AD674B/AD774B–SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5%, unless otherwise noted.)

Model (AD674B or AD774B)	J Grade Min	J Grade Typ	J Grade Max	K Grade Min	K Grade Typ	K Grade Max	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	T Grade Min	T Grade Typ	T Grade Max	Unit
RESOLUTION			12			12			12			12			12	Bits
LINEARITY ERROR @ 25°C			±1			±1/2			±1			±1/2			±1/2	LSB
T_{MIN} to T_{MAX}			±1			±1/2			±1			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum Resolution for Which No Missing Codes are Guaranteed)	**12**			**12**			**12**			**12**			12			Bits
UNIPOLAR OFFSET[1] @ 25°C			±2			±2			±2			±2			±2	LSB
BIPOLAR OFFSET[1] @ 25°C			±6			±3			±6			±3			±3	LSB
FULL-SCALE CALIBRATION ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	**0.25**		0.1	**0.125**		0.1	**0.25**		0.1	**0.125**		0.1	**0.125**	% of FS
TEMPERATURE RANGE	**0**		**70**	**0**		**70**	**–40**		**+85**	**–40**		**+85**	**–55**		**+125**	°C
TEMPERATURE DRIFT[3] (Using Internal Reference)																
Unipolar			±2			±1			±2			±1			±1	LSB
Bipolar Offset			±2			±1			±2			±1			±2	LSB
Full-Scale Calibration			±6			±2			±8			±5			±7	LSB
POWER SUPPLY REJECTION Max Change in Full-Scale Calibration																
V_{CC} = +15 V ± 1.5 V or +12 V ± 0.6 V			±2			±1			±2			±1			±1	LSB
V_{LOGIC} = +5 V ± 0.5 V			±1/2			±1/2			±1/2			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1			±2			±1			±1	LSB
ANALOG INPUT																
Input Ranges																
Bipolar	–5		+5	–5		+5	–5		+5	–5		+5	–5		+5	V
	–10		+10	–10		+10	–10		+10	–10		+10	–10		+10	V
Unipolar	0		10	0		10	0		10	0		10	0		10	V
	0		20	0		20	0		20	0		20	0		20	V
Input Impedance																
10 V Span	**3**	5	7	**3**	5	7	**3**	5	7	**3**	5	7	**3**	5	7	kΩ
20 V Span	**6**	10	**14**	**6**	10	**14**	**6**	10	**14**	**6**	10	**14**	**6**	10	**14**	kΩ
POWER SUPPLIES																
Operating Range																
V_{LOGIC}	4.5		5.5	4.5		5.5	4.5		5.5	4.5		5.5	4.5		5.5	V
V_{CC}	11.4		16.5	11.4		16.5	11.4		16.5	11.4		16.5	11.4		16.5	V
V_{EE}	–16.5		–11.4	–16.5		–11.4	–16.5		–11.4	–16.5		–11.4	–16.5		–11.4	V
Operating Current																
I_{LOGIC}		3.5	7		3.5	7		3.5	7		3.5	7		3.5	7	mA
I_{CC}		3.5	7		3.5	7		3.5	7		3.5	7		3.5	7	mA
I_{EE}		10	**14**		10	**14**		10	**14**		10	**14**		10	**14**	mA
POWER CONSUMPTION		220	**375**		220	**375**		220	**375**		220	**375**		220	**375**	mW[4]
		175			175			175			175			175		mW[5]
INTERNAL REFERENCE VOLTAGE	**9.9**	10.0	**10.1**	**9.9**	10.0	**10.1**	**9.9**	10.0	**10.1**	**9.9**	10.0	**10.1**	**9.9**	10.0	**10.1**	V
Output Current (Available for External Loads) (External Load Should Not Change During the Conversion)			2.0			2.0			2.0			2.0			2.0	mA

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from 25°C value to the value at T_{MIN} or T_{MAX}.
[4]Tested with REF OUT tied to REF IN through 50 Ω resistor, V_{CC} = +16.5 V, V_{EE} = –16.5 V, V_{LOGIC} = +5.5 V, and outputs in high-Z mode.
[5]Tested with REF OUT tied to REF IN through 50 Ω resistor, V_{CC} = +12 V, V_{EE} = –12 V, V_{LOGIC} = +5 V, and outputs in high-Z mode.

Specifications subject to change without notice.
Specifications shown in **boldface** are tested on **all** devices at final electrical test at T_{MIN}, 25°C, and T_{MAX}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

DIGITAL SPECIFICATIONS

(For all grades T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5%, unless otherwise noted.)

Parameter		Test Conditions	Min	Max	Unit
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.0**	V_{LOGIC} + 0.5	V
V_{IL}	Low Level Input Voltage		–0.5	**+0.8**	V
I_{IH}	High Level Input Current	$V_{IN} = V_{LOGIC}$	**–10**	**+10**	µA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	**–10**	**+10**	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	**–10**	**+10**	µA
C_{OZ}	High-Z Output Capacitance			10	pF

SWITCHING SPECIFICATIONS

(For all grades T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5%, unless otherwise noted.)

CONVERTER START TIMING (Figure 1)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Unit
Conversion Time								
8-Bit Cycle (AD674B)	t_C	6	8	**10**	6	8	**10**	µs
12-Bit Cycle (AD674B)	t_C	9	12	**15**	9	12	**15**	µs
8-Bit Cycle (AD774B)	t_C	4	5	**6**	4	5	**6**	µs
12-Bit Cycle (AD774B)	t_C	6	7.3	**8**	6	7.3	**8**	µs
STS Delay from CE	t_{DSC}			200			225	ns
CE Pulsewidth	t_{HEC}	50			50			ns
CS to CE Setup	t_{SSC}	50			50			ns
CS Low During CE High	t_{HSC}	50			50			ns
R/C to CE Setup	t_{SRC}	50			50			ns
R/C LOW During CE High	t_{HRC}	50			50			ns
A_0 to CE Setup	t_{SAC}	0			0			ns
A_0 Valid During CE High	t_{HAC}	50			50			ns

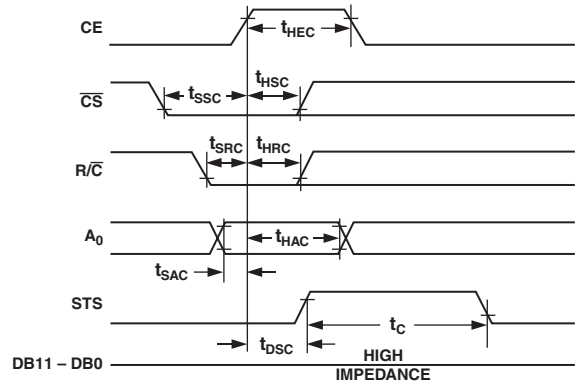


Figure 1. Convert Start Timing

READ TIMING—FULL CONTROL MODE (Figure 2)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Unit
Access Time								
C_L = 100 pF	t_{DD}[1]		75	150		75	150	ns
Data Valid After CE Low	t_{HD}	25[2]			25[2]			ns
		20[3]			15[4]			ns
Output Float Delay	t_{HL}[5]			150			150	ns
CS to CE Setup	t_{SSR}	50			50			ns
R/C to CE Setup	t_{SRR}	0			0			ns
A_0 to CE Setup	t_{SAR}	50			50			ns
CS Valid After CE Low	t_{HSR}	0			0			ns
R/C High After CE Low	t_{HRR}	0			0			ns
A_0 Valid After CE Low	t_{HAR}	50			50			ns

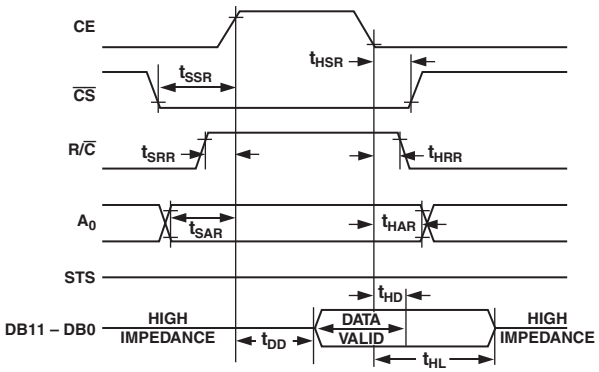
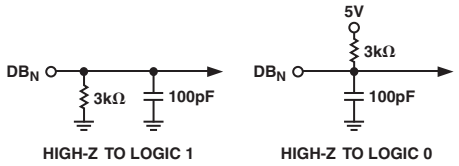
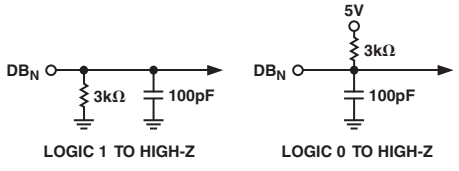


Figure 2. Read Cycle Timing



High-Z to Logic 1 *High-Z to Logic 0*

Figure 3a. Load Circuit for Access Time Test



Logic 1 to High-Z *Logic 0 to High-Z*

Figure 3b. Load Circuit for Output Float Delay Test

NOTES

[1] t_{DD} is measured with the load circuit of Figure 3a and is defined as the time required for an output to cross 0.4 V or 2.4 V.

[2] 0°C to T_{MAX}.

[3] At –40°C.

[4] At –55°C.

[5] t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 3b.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{MIN}, 25°C, and T_{MAX}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING—STAND ALONE MODE (Figures 4a and 4b)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Unit
Data Access Time	t_{DDR}			150			150	ns
Low R/C Pulsewidth	t_{HRL}	50			50			ns
STS Delay from R/C	t_{DS}			200			225	ns
Data Valid After R/C Low	t_{HDR}	25			25			ns
STS Delay After Data Valid	t_{HS}	30	200	600	30	200	600	ns
High R/C Pulsewidth	t_{HRH}	150			150			ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5 V
V_{EE} to Digital Common . . . . . 0 to –16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . . . –0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . ±24 V
REF OUT . . . . . Indefinite Short to Common
. . . . . Momentary Short to V_{CC}
Junction Temperature . . . . . 175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering (10 sec) . . . . . 300°C
Storage Temperature . . . . . –65°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

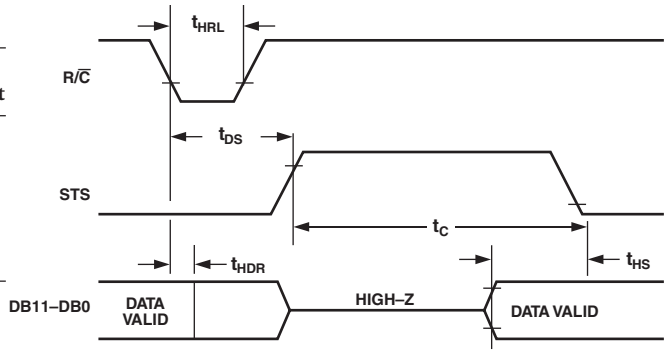


FIgure 4a. Standalone Mode Timing Low Pulse R/C

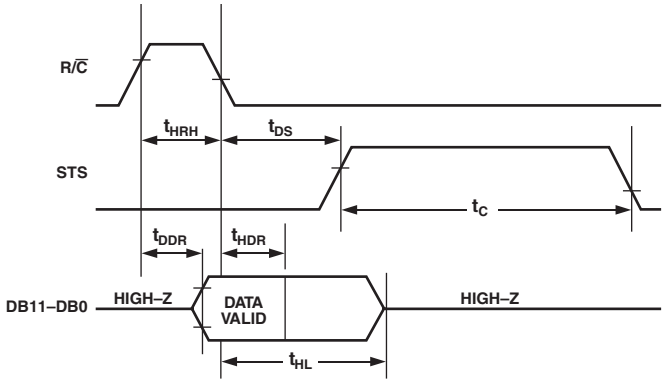


Figure 4b. Standalone Mode Timing High Pulse for R/C

ORDERING GUIDE

Model[1]	Temperature	Conversion Time (max)	INL (T_{MIN} to T_{MAX})	Package Description	Package Option[2]
AD674BJN	0°C to 70°C	15 µs	±1 LSB	Plastic DIP	N-28
AD674BKN	0°C to 70°C	15 µs	±1/2 LSB	Plastic DIP	N-28
AD674BAR	–40°C to +85°C	15 µs	±1 LSB	Plastic SOIC	R-28
AD674BBR	–40°C to +85°C	15 µs	±1/2 LSB	Plastic SOIC	R-28
AD674BAD	–40°C to +85°C	15 µs	±1 LSB	Ceramic DIP	D-28
AD674BBD	–40°C to +85°C	15 µs	±1/2 LSB	Ceramic DIP	D-28
AD674BTD	–55°C to +125°C	15 µs	±1 LSB	Ceramic DIP	D-28
AD774BJN	0°C to 70°C	8 µs	±1 LSB	Plastic DIP	N-28
AD774BKN	0°C to 70°C	8 µs	±1/2 LSB	Plastic DIP	N-28
AD774BAR	–40°C to +85°C	8 µs	±1 LSB	Plastic SOIC	R-28
AD774BBR	–40°C to +85°C	8 µs	±1/2 LSB	Plastic SOIC	R-28
AD774BAD	–40°C to +85°C	8 µs	±1 LSB	Ceramic DIP	D-28
AD774BBD	–40°C to +85°C	8 µs	±1/2 LSB	Ceramic DIP	D-28
AD774BTD	–55°C to +125°C	8 µs	±1 LSB	Ceramic DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or the current AD674B/ AD774B/883B data sheet.
[2]N = Plastic DIP; D = Hermetic DIP; R = Plastic SOIC.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD674B/AD774B features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITION OF SPECIFICATIONS

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB (1.22 mV for 10 V span) before the first code transition (all zeroes to only the LSB "on"). "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The K, B, and T grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value that falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The J and A grades are guaranteed to ±1 LSB max error. For these grades, an analog value that falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user adjustable.

Differential Linearity Error (No Missing Codes)

A specification that guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The AD674B and AD774B guarantee no missing codes to 12-bit resolution, requiring that all 4096 codes must be present over the entire operating temperature ranges.

Unipolar Offset

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The output data format is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point 4095 to the left of the MSB.

Full-Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 V for 10.000 V full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05% to 0.1% of full scale, can be trimmed out as shown in Figures 7 and 8. The full-scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full-scale gain from the initial value using the internal 10 V reference.

Temperature Drift

The temperature drift for full-scale calibration, unipolar offset, and bipolar offset specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

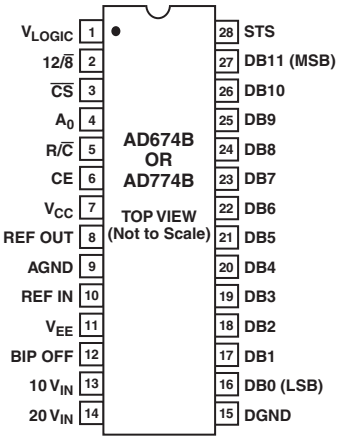
Power Supply Rejection

The standard specifications assume use of +5.00 V and ±15.00 V or ±12.00 V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all low-order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44 mV out of 10 V for a 12-bit ADC.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Symbol	Pin No.	Type*	Name and Function
AGND	9	P	Analog Ground (Common)
A_0	4	DI	Byte Address/Short Cycle. If a conversion is started with A_0 Active LOW, a full 12-bit conversion cycle is initiated. If A_0 is Active HIGH during a convert start, a shorter 8-bit conversion cycle results. During Read (R/$\overline{C}$ = 1) with 12/$\overline{8}$ LOW, A_0 = LOW enables the 8 most significant bits, and A_0 = HIGH enables DB3–DB0 and sets DB7–DB4 = 0.
BIP OFF	12	AI	Bipolar Offset. Connect through a 50 Ω resistor to REF OUT for bipolar operation or to Analog Common for unipolar operation.
CE	6	DI	Chip Enable. Chip Enable is Active HIGH and is used to initiate a convert or read operation.
$\overline{CS}$	3	DI	Chip Select. Chip Select is Active LOW.
DB11–DB8	27–24	DO	Data Bits 11 through 8. In the 12-bit format (see 12/$\overline{8}$ and A_0 pins) these pins provide the upper 4 bits of data. In the 8-bit format, they provide the upper 4 bits when A_0 is LOW and are disabled when A_0 is HIGH.
DB7–DB4	23–20	DO	Data Bits 7 through 4. In the 12-bit format these pins provide the middle 4 bits of data. In the 8-bit format they provide the middle 4 bits when A_0 is LOW and all zeroes when A_0 is HIGH.
DB3–DB0	19–16	DO	Data Bits 3 through 0. In both the 12-bit and 8-bit format these pins provide the lower 4 bits of data when A_0 is HIGH; they are disabled when A_0 is LOW.
DGND	15	P	Digital Ground (Common)
REF OUT	8	AO	10 V Reference Output
R/$\overline{C}$	5	DI	Read/Convert. In the full control mode R/$\overline{C}$ is Active HIGH for a read operation and Active LOW for a convert operation. In the standalone mode, the falling edge of R/$\overline{C}$ initiates a conversion.
REF IN	10	AI	Reference Input is connected through a 50 Ω resistor to +10 V Reference for normal operation.
STS	28	DO	Status is Active HIGH when a conversion is in progress and goes LOW when the conversion is completed.
V_{CC}	7	P	+12 V/+15 V Analog Supply
V_{EE}	11	P	–12 V/–15 V Analog Supply
V_{LOGIC}	1	P	5 V Logic Supply
10 V_{IN}	13	AI	10 V Span Input, 0 V to +10 V unipolar mode or –5 V to +5 V bipolar mode. When using the 20 V Span, 10 V_{IN} should not be connected.
20 V_{IN}	14	AI	20 V Span Input, 0 V to +20 V unipolar mode or –10 V to +10 V bipolar mode. When using the 10 V Span, 20 V_{IN} should not be connected.
12/$\overline{8}$	2	DI	The 12/$\overline{8}$ pin determines whether the digital output data is to be organized as two 8-bit words (12/$\overline{8}$ LOW) or a single 12-bit word (12/$\overline{8}$ HIGH).

*Types: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power

CIRCUIT OPERATION

The AD674B and AD774B are complete 12-bit monolithic A/D converters that require no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram is shown in Figure 5.

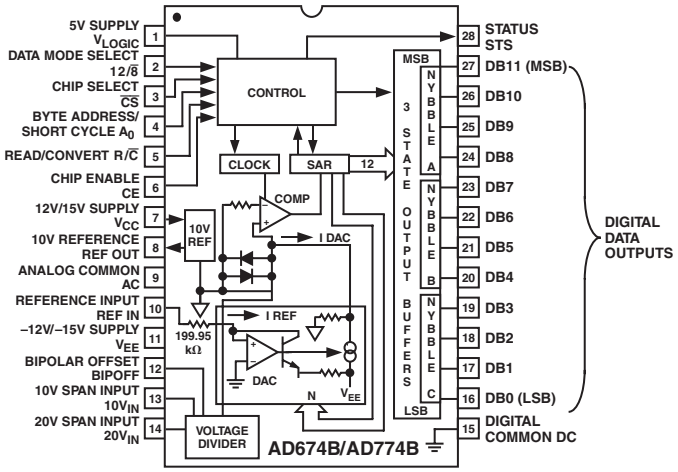


Figure 5. Block Diagram of AD674B and AD774B

When the control section is commanded to initiate a conversion (as described later) it enables the clock and resets the successive-approximation register (SAR) to all zeroes. Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most significant bit (MSB) to least significant bit (LSB) to provide an output current that accurately balances the input signal current through the divider network. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code that accurately represents the input signal to within ±1/2 LSB.

The temperature-compensated reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 V ± 1%; it can supply up to 2.0 mA to an external load in addition to the requirements of the reference input resistor (0.5 mA) and bipolar offset resistor (0.5 mA). Any external load on the reference must remain constant during conversion. The thin-film application resistors are trimmed to match the full-scale output current of the DAC. The input divider network provides a 10 V or 20 V input range. The bipolar offset resistor is grounded for unipolar operation and connected to the 10 V reference for bipolar operation.

DRIVING THE ANALOG INPUT

The AD674B and AD774B are successive-approximation analog-to-digital converters. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 1 MHz rate. Thus it is important to recognize that the signal source driving the ADC must be capable of holding a constant output voltage under dynamically changing load conditions.

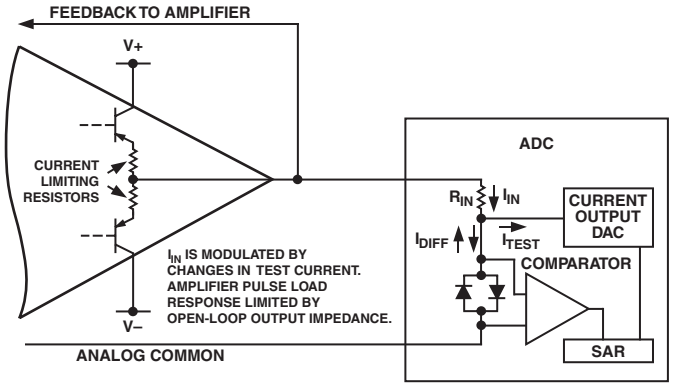


Figure 6. Op Amp—ADC Interface

The closed-loop output impedance of an op amp is equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower-connected op amp is sufficiently high to reduce the closed-loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving the ADC must either have sufficient loop gain at 1 MHz to reduce the closed-loop output impedance to a low value or have low open-loop output impedance. This can be accomplished by using a wideband op amp, such as the AD711.

If a sample-hold amplifier is required, the monolithic AD585 or AD781 is recommended, with the output buffer driving the AD674B or AD774B input directly. A better alternative is the AD1674, which is a 10 µs *sampling* ADC in the same pinout as the AD574A, AD674A, or AD774B and is functionally equivalent.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATION

It is critical that the power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies will cause unstable output codes. Switching power supplies is not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Few millivolts of noise represent several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the 5 V supply decoupling capacitor should be connected directly from Pin 1 to Pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (Pin 9). A suitable decoupling capacitor is a 4.7 µF tantalum type in parallel with a 0.1 µF ceramic disc type.

Circuit layout should attempt to locate the ADC, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit layout and manufacturing is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD674B AND AD774B

The AD674B and AD774B contain all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5 V, +12/+15 V, and –12/–15 V), the analog input, and the conversion initiation command, as discussed on the next page.

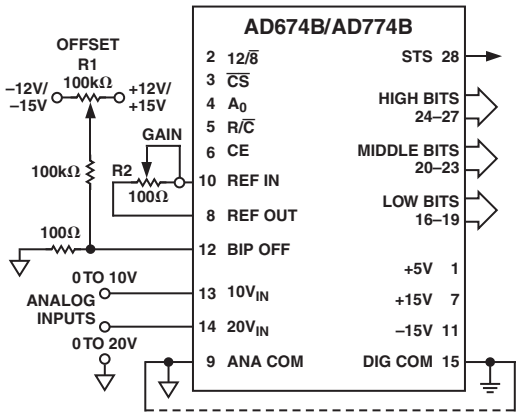


Figure 7. Unipolar Input Connections

All of the thin-film application resistors of the AD674B and AD774B are factory trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, ±2 LSB max zero offset error and ±0.25% (10 LSB) max full-scale error are guaranteed. If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed. If the full-scale trim is not required, a 50 Ω 1% metal film resistor should be connected between Pin 8 and Pin 10.

The analog input is connected between Pins 13 and 9 for a 0 V to 10 V input range, between Pins 14 and 9 for a 0 V to 20 V input range. Input signals beyond the supplies are easily accommodated. For the 10 V span input, the LSB has a nominal value of 2.44 mV; for the 20 V span, 4.88 mV. If a 10.24 V range is desired (nominal 2.5 mV/bit), the gain trimmer (R2) should be replaced by a 50 Ω resistor and a 200 Ω trimmer inserted in series with the analog input to Pin 13 (for a full-scale range of 20.48 V [5 mV/bit] use a 500 Ω trimmer into Pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into Pin 13 is 5 kΩ, and into Pin 14 is 10 kΩ.

UNIPOLAR CALIBRATION

The connections for unipolar ranges are shown in Figure 7. The AD674B or AD774B is trimmed to a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (1.22 mV for 10 V range).

If Pin 12 is connected to Pin 9, the unit will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15 mV of offset trim range.

The full-scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale (9.9963 for a 10 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 8. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50 Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (–4.9988 V for the ±5 V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale (+4.9963 V for the ±5 V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

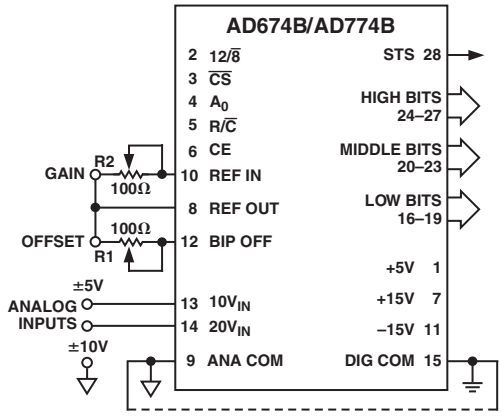


Figure 8. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at Pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the ADC; it should be connected directly to the analog reference point of the system. To achieve the high-accuracy performance available from the ADC in an environment of high digital noise content, the analog and digital commons must be connected together at the package. In some situations, the digital common at Pin 15 can be connected to the most convenient ground reference point; digital power return is preferred.

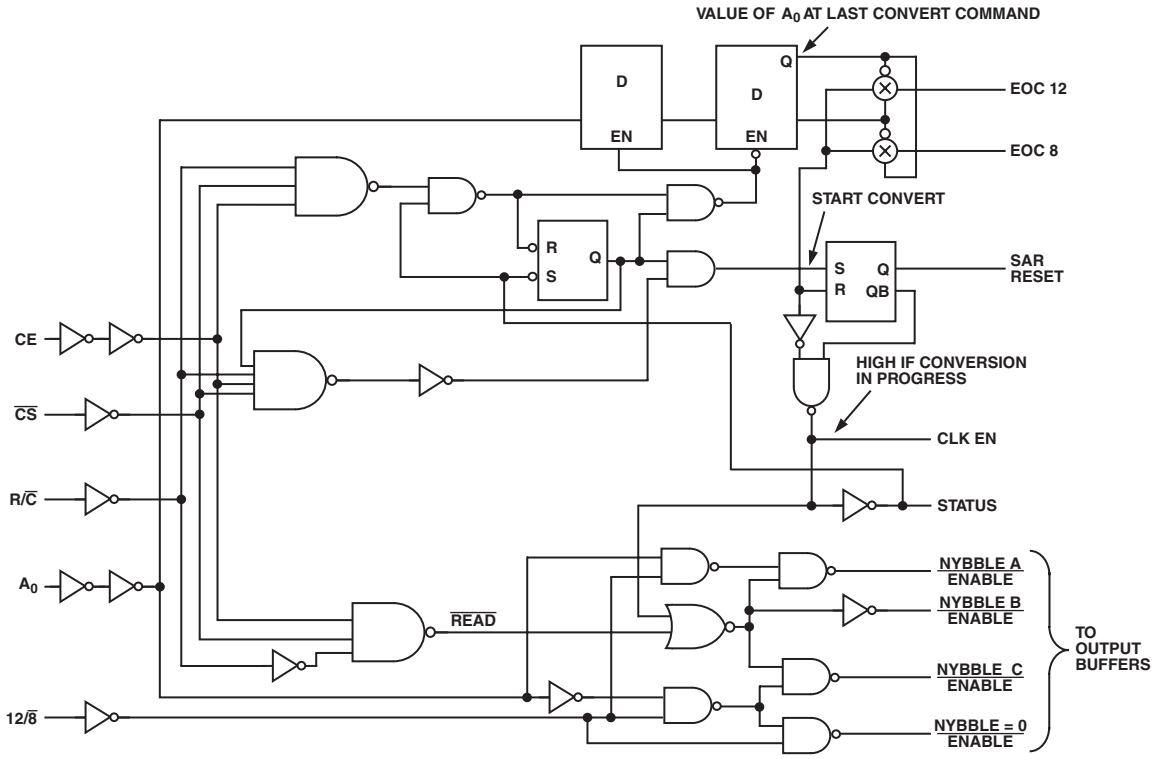


Figure 9. Equivalent Internal Logic Circuitry

CONTROL LOGIC

The AD674B and AD774B contain on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems; this internal logic circuitry is shown in Figure 9.

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs, A_0 and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to V_{LOGIC}). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

Table I. Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4 LSBs + 4 Trailing Zeroes

The ADC may be operated in one of two modes, the full-control mode and the standalone mode. The full-control mode uses all the control signals and is useful in systems that address decode multiple devices on a single data bus. The standalone mode is useful in systems with dedicated input ports available. In general, the standalone mode is capable of issuing start-convert commands on a more precise basis and therefore produces higher accuracy results. The following sections describe these two modes in more detail.

FULL-CONTROL MODE

Chip Enable (CE), Chip Select ($\overline{CS}$), and Read/Convert (R/$\overline{C}$) are used to control Convert or Read modes of operation. Either CE or $\overline{CS}$ may be used to initiate a conversion. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data Read (R/$\overline{C}$ = 1) or a Convert (R/$\overline{C}$ = 0) is in progress. R/$\overline{C}$ should be LOW before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is HIGH, a Read operation will momentarily occur, possibly resulting in system bus contention.

STANDALONE MODE

"Standalone" mode is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Standalone mode applications are generally able to issue conversion start commands more precisely than full-control mode, resulting in improved accuracy.

CE and 12/$\overline{8}$ are wired HIGH, $\overline{CS}$ and A_0 are wired LOW, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is HIGH and a conversion starts when R/$\overline{C}$ goes LOW. This gives rise to two possible control signals—a high pulse or a low pulse. Operation with a low pulse is shown in Figure 4a. In this case, the outputs are forced into the high impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes HIGH 200 ns after R/C goes LOW and returns low 600 ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 4b, the data lines are enabled during the time when R/$\overline{C}$ is HIGH. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

CONVERSION TIMING

Once a conversion is started, the STS line goes HIGH. Convert start commands will be ignored until the conversion cycle is complete. The output data buffers can be enabled up to 1.2 µs prior to STS going LOW. The STS line will return LOW at the end of the conversion cycle.

The register control inputs, A_0 and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with A_0 LOW, a full 12-bit conversion cycle is initiated. If A_0 is HIGH during a convert start, a shorter 8-bit conversion cycle results.

During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied LOW) or a single 12-bit word (12/$\overline{8}$ tied HIGH). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most integrated circuit ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD674B and AD774B provide an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also generate an interrupt upon completion of conversion if the system timing requirements are critical and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take its maximum conversion time to convert, and insert a sufficient number of "no-op" instructions to ensure that this amount of processor time is consumed.

Once conversion is complete, the data can be read. For converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD674B and AD774B include internal logic to permit direct interface to 8-bit and 16-bit data buses, selected by the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining 4 bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A_0 low) contains the 8 MSBs (DB11 through DB4). The odd address (A_0 high) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the output data lines for right-justified 8-bit bus interface.

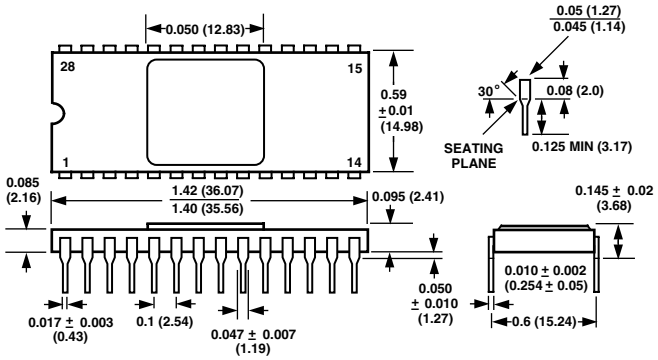
	D7							D0
XXX0 (EVEN ADDR)	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR)	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

Figure 10. Data Format for 8-Bit Bus

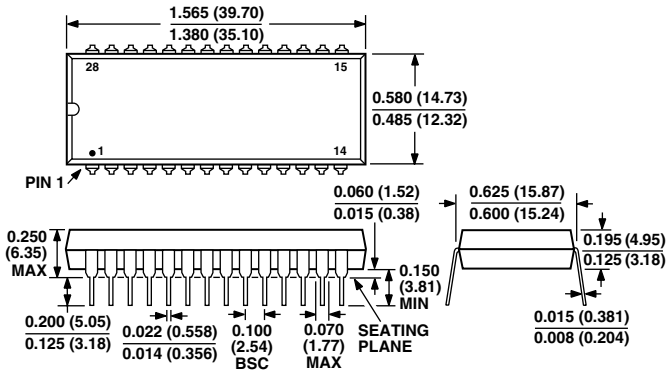
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

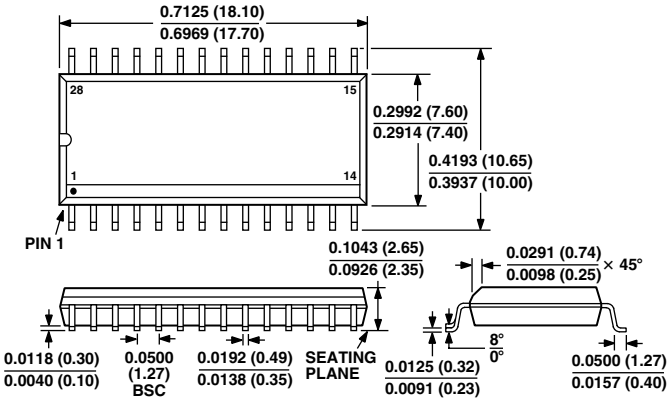
28-Lead Ceramic DIP Package
(D-28)



28-Lead Plastic DIP Package
(N-28)



28-Lead Wide Body SOIC Package
(R-28)



Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Edits to ORDERING GUIDE	5
Add 28-Lead Wide Body SOIC Package Drawing	12

C00808-0-4/02(C)

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