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REVISION HISTORY

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4/05—Rev. A to Rev. B

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11/04—Rev. 0 to Rev. A

Updated Format ... Universal
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5/03—Revision 0: Initial Version

SPECIFICATIONS

AD7466

V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS, unless otherwise noted. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. The temperature range for the B version is −40°C to +85°C.

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz sine wave
Signal-to-Noise and Distortion (SINAD)	69	dB min	1.8 V ≤ V_{DD} ≤ 2 V; see the Terminology section
	70	dB min	2.5 V ≤ V_{DD} ≤ 3.6 V
	70	dB typ	V_{DD} = 1.6 V
Signal-to-Noise Ratio (SNR)	70	dB min	1.8 V ≤ V_{DD} ≤ 2 V; see the Terminology section
	71	dB typ	1.8 V ≤ V_{DD} ≤ 2 V
	71	dB min	2.5 V ≤ V_{DD} ≤ 3.6 V
	70.5	dB typ	V_{DD} = 1.6 V
Total Harmonic Distortion (THD)	−83	dB typ	See the Terminology section
Peak Harmonic or Spurious Noise (SFDR)	−85	dB typ	See the Terminology section
Intermodulation Distortion (IMD)			fa = 29.1 kHz, fb = 29.9 kHz; see the Terminology section
Second-Order Terms	−84	dB typ	
Third-Order Terms	−86	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	40	ps typ	
Full Power Bandwidth	3.2	MHz typ	@ 3 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
	1.9	MHz typ	@ 3 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
	750	kHz typ	@ 0.1 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
	450	kHz typ	@ 0.1 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
DC ACCURACY			Maximum specifications apply as typical figures when V_{DD} = 1.6 V
Resolution	12	Bits	
Integral Nonlinearity	±1.5	LSB max	See the Terminology section
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits; see the Terminology section
Offset Error	±1	LSB max	See the Terminology section
Gain Error	±1	LSB max	See the Terminology section
Total Unadjusted Error (TUE)	±2	LSB max	See the Terminology section
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DD}	V min	1.6 V ≤ V_{DD} < 2.7 V
	2	V min	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.2 × V_{DD}	V max	1.6 V ≤ V_{DD} < 1.8 V
	0.3 × V_{DD}	V max	1.8 V ≤ V_{DD} < 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 20 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}	10	pF max	Sample tested at 25°C to ensure compliance

Parameter	B Version	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 1.6 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance	10	pF max	
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	4.70	µs max	16 SCLK cycles with SCLK at 3.4 MHz
Throughput Rate	200	kSPS max	See the Serial Interface section
POWER REQUIREMENTS			
V_{DD}	1.6/3.6	V min/max	
I_{DD}			Digital inputs = 0 V or V_{DD}
Normal Mode (Operational)	300	µA max	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
	110	µA typ	V_{DD} = 3 V, f_{SAMPLE} = 50 kSPS
	20	µA typ	V_{DD} = 3 V, f_{SAMPLE} = 10 kSPS
	240	µA max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
	80	µA typ	V_{DD} = 2.5 V, f_{SAMPLE} = 50 kSPS
	16	µA typ	V_{DD} = 2.5 V, f_{SAMPLE} = 10 kSPS
	165	µA max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
	50	µA typ	V_{DD} = 1.8 V, f_{SAMPLE} = 50 kSPS
	10	µA typ	V_{DD} = 1.8 V, f_{SAMPLE} = 10 kSPS
Power-Down Mode	0.1	µA max	SCLK on or off, typically 8 nA
Power Dissipation			See the Power Consumption section
Normal Mode (Operational)	0.9	mW max	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
	0.6	mW max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
	0.3	mW max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
Power-Down Mode	0.3	µW max	V_{DD} = 3 V

AD7467

V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS, unless otherwise noted. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. The temperature range for the B version is −40°C to +85°C.

Table 2.

Parameter	B Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			Maximum/minimum specifications apply as typical figures when V_{DD} = 1.6 V, f_{IN} = 30 kHz sine wave
Signal-to-Noise and Distortion (SINAD)	61	dB min	See the Terminology section
Total Harmonic Distortion (THD)	−72	dB max	See the Terminology section
Peak Harmonic or Spurious Noise (SFDR)	−74	dB max	See the Terminology section
Intermodulation Distortion (IMD)			fa = 29.1 kHz, fb = 29.9 kHz; see the Terminology section
Second-Order Terms	−83	dB typ	
Third-Order Terms	−83	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	40	ps typ	
Full Power Bandwidth	3.2	MHz typ	@ 3 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
	1.9	MHz typ	@ 3 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
	750	kHz typ	@ 0.1 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
	450	kHz typ	@ 0.1 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
DC ACCURACY			Maximum specifications apply as typical figures when V_{DD} = 1.6 V
Resolution	10	Bits	
Integral Nonlinearity	±0.5	LSB max	See the Terminology section
Differential Nonlinearity	±0.5	LSB max	Guaranteed no missed codes to 10 bits; see the Terminology section
Offset Error	±0.2	LSB max	See the Terminology section
Gain Error	±0.2	LSB max	See the Terminology section
Total Unadjusted Error (TUE)	±1	LSB max	See the Terminology section
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DD}	V min	1.6 V ≤ V_{DD} < 2.7 V
	2	V min	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.2 × V_{DD}	V max	1.6 V ≤ V_{DD} < 1.8 V
	0.3 × V_{DD}	V max	1.8 V ≤ V_{DD} < 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 20 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}	10	pF max	Sample tested at 25°C to ensure compliance
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 1.6 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance	10	pF max	Sample tested at 25°C to ensure compliance
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	3.52	µs max	12 SCLK cycles with SCLK at 3.4 MHz
Throughput Rate	275	kSPS max	See the Serial Interface section

Parameter	B Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	1.6/3.6	V min/max	
I_{DD}			Digital inputs = 0 V or V_{DD}
Normal Mode (Operational)	210	μA max	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
	170	μA max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
	140	μA max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
Power-Down Mode	0.1	μA max	SCLK on or off, typically 8 nA
Power Dissipation			See the Power Consumption section
Normal Mode (Operational)	0.63	mW max	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
	0.42	mW max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
	0.25	mW max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
Power-Down Mode	0.3	μW max	V_{DD} = 3 V

AD7468

V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS, unless otherwise noted. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. The temperature range for the B version is −40°C to +85°C.

Table 3.

Parameter	B Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			Maximum/minimum specifications apply as typical figures when V_{DD} = 1.6 V, f_{IN} = 30 kHz sine wave
Signal-to-Noise and Distortion (SINAD)	49	dB min	See the Terminology section
Total Harmonic Distortion (THD)	−66	dB max	See the Terminology section
Peak Harmonic or Spurious Noise (SFDR)	−66	dB max	See the Terminology section
Intermodulation Distortion (IMD)			fa = 29.1 kHz, fb = 29.9 kHz; see the Terminology section
Second-Order Terms	−77	dB typ	
Third-Order Terms	−77	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	40	ps typ	
Full Power Bandwidth	3.2	MHz typ	@ 3 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
	1.9	MHz typ	@ 3 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
	750	kHz typ	@ 0.1 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
	450	kHz typ	@ 0.1 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
DC ACCURACY			Maximum specifications apply as typical figures when V_{DD} = 1.6 V
Resolution	8	Bits	
Integral Nonlinearity	±0.2	LSB max	See the Terminology section
Differential Nonlinearity	±0.2	LSB max	Guaranteed no missed codes to 8 bits; see the Terminology section
Offset Error	±0.1	LSB max	See the Terminology section
Gain Error	±0.1	LSB max	See the Terminology section
Total Unadjusted Error (TUE)	±0.3	LSB max	See the Terminology section
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DD}	V min	1.6 V ≤ V_{DD} < 2.7 V
	2	V min	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.2 × V_{DD}	V max	1.6 V ≤ V_{DD} < 1.8 V
	0.3 × V_{DD}	V max	1.8 V ≤ V_{DD} < 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 20 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}	10	pF max	Sample tested at 25°C to ensure compliance
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 1.6 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance	10	pF max	Sample tested at 25°C to ensure compliance
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	2.94	µs max	10 SCLK cycles with SCLK at 3.4 MHz
Throughput Rate	320	kSPS max	See the Serial Interface section

Parameter	B Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	1.6/3.6	V min/max	
I_{DD}			Digital inputs = 0 V or V_{DD}
Normal Mode (Operational)	190	μA max	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
	155	μA max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
	120	μA max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
Power-Down Mode	0.1	μA max	SCLK on or off, typically 8 nA
Power Dissipation			See the Power Consumption section
Normal Mode (Operational)	0.57	mW max	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
	0.4	mW max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
	0.2	mW max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
Power-Down Mode	0.3	μW max	V_{DD} = 3 V

TIMING SPECIFICATIONS

For all devices, V_{DD} = 1.6 V to 3.6 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.4 V.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	3.4	MHz max	Mark/space ratio for the SCLK input is 40/60 to 60/40.
	10	kHz min	1.6 V ≤ V_{DD} ≤ 3 V; minimum f_{SCLK} at which specifications are guaranteed.
	20	kHz min	V_{DD} = 3.3 V; minimum f_{SCLK} at which specifications are guaranteed.
	150	kHz min	V_{DD} = 3.6 V; minimum f_{SCLK} at which specifications are guaranteed.
$t_{CONVERT}$	16 × t_{SCLK}		AD7466.
	12 × t_{SCLK}		AD7467.
	10 × t_{SCLK}		AD7468.
Acquisition Time			Acquisition time/power-up time from power-down. See the Terminology section. The acquisition time is the time required for the part to acquire a full-scale step input value within ±1 LSB or a 30 kHz ac input value within ±0.5 LSB.
	780	ns max	V_{DD} = 1.6 V.
	640	ns max	1.8 V ≤ V_{DD} ≤ 3.6 V.
t_{QUIET}	10	ns min	Minimum quiet time required between bus relinquish and the start of the next conversion.
t_1	10	ns min	Minimum $\overline{CS}$ pulse width.
t_2	55	ns min	$\overline{CS}$ to SCLK setup time. If V_{DD} = 1.6 V and f_{SCLK} = 3.4 MHz, t_2 has to be 192 ns minimum in order to meet the maximum figure for the acquisition time.
t_3	55	ns max	Delay from $\overline{CS}$ until SDATA is three-state disabled. Measured with the load circuit in Figure 2 and defined as the time required for the output to cross the V_{IH} or V_{IL} voltage.
t_4	140	ns max	Data access time after SCLK falling edge. Measured with the load circuit in Figure 2 and defined as the time required for the output to cross the V_{IH} or V_{IL} voltage.
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width.
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width.
t_7	10	ns min	SCLK to data valid hold time. Measured with the load circuit in Figure 2 and defined as the time required for the output to cross the V_{IH} or V_{IL} voltage.
t_8	60	ns max	SCLK falling edge to SDATA three-state. t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics, is the true bus relinquish time of the part, and is independent of the bus loading.
	7	ns min	SCLK falling edge to SDATA three-state.

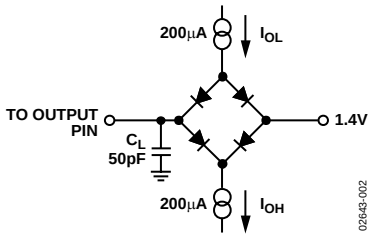


Figure 2. Load Circuit for Digital Output Timing Specifications

TIMING EXAMPLES

Figure 3 shows some of the timing parameters from Table 4 in the Timing Specifications section.

Timing Example 1

As shown in Figure 3, f_{SCLK} = 3.4 MHz and a throughput of 100 kSPS gives a cycle time of $t_{CONVERT} + t_8 + t_{QUIET}$ = 10 µs. Assuming V_{DD} = 1.8 V, $t_{CONVERT} = t_2 + 15(1/f_{SCLK})$ = 55 ns + 4.41 µs = 4.46 µs, and t_8 = 60 ns maximum, then t_{QUIET} = 5.48 µs, which satisfies the requirement of 10 ns for t_{QUIET}. The part is fully powered up and the signal is fully acquired at Point A. This means that the acquisition/power-up time is $t_2 + 2(1/f_{SCLK})$ = 55 ns + 588 ns = 643 ns, satisfying the maximum requirement of 640 ns for the power-up time.

Timing Example 2

The AD7466 can also operate with slower clock frequencies. As shown in Figure 3, assuming V_{DD} = 1.8 V, f_{SCLK} = 2 MHz, and a throughput of 50 kSPS gives a cycle time of $t_{CONVERT} + t_8 + t_{QUIET}$ = 20 µs. With $t_{CONVERT} = t_2 + 15(1/f_{SCLK})$ = 55 ns + 7.5 µs = 7.55 µs, and t_8 = 60 ns maximum, this leaves t_{QUIET} to be 12.39 µs, which satisfies the requirement of 10 ns for t_{QUIET}. The part is fully powered up and the signal is fully acquired at Point A, which means the acquisition/power-up time is $t_2 + 2(1/f_{SCLK})$ = 55 ns + 1 µs = 1.05 µs, satisfying the maximum requirement of 640 ns for the power-up time. In this example and with other slower clock values, the part is fully powered up and the signal already acquired before the third SCLK falling edge; however, the track-and-hold does not go into hold mode until that point. In this example, the part can be powered up and the signal can be fully acquired at approximately Point B in Figure 3.

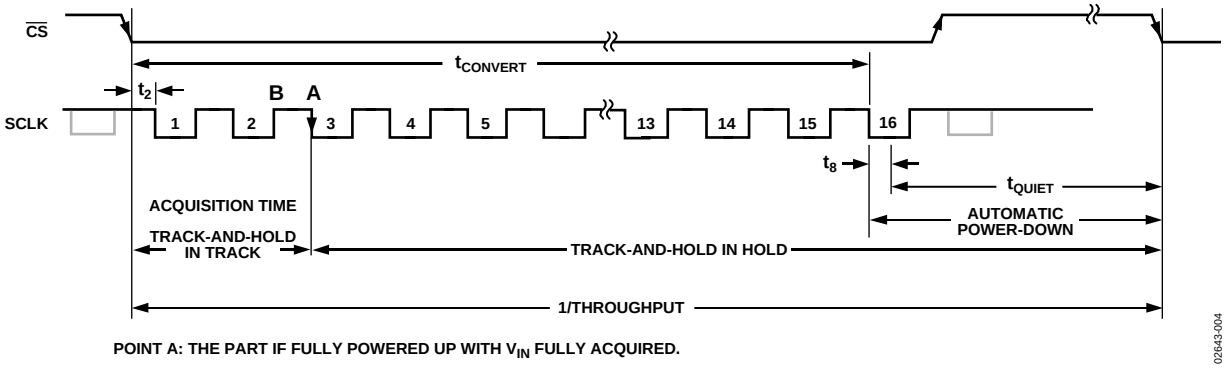


Figure 3. AD7466 Serial Interface Timing Diagram Example

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to any Pin Except Supplies	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-23 Package	
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W
MSOP Package	
θ_{JA} Thermal Impedance	205.9°C/W
θ_{JC} Thermal Impedance	43.74°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

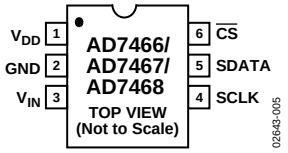


Figure 4. SOT-23 Pin Configuration

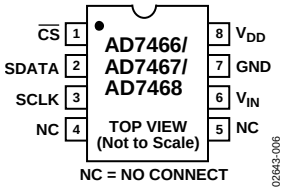


Figure 5. MSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
SOT-23	**MSOP**	**Mnemonic**	**Description**
6	1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the devices and frames the serial data transfer.
1	8	V_{DD}	Power Supply Input. The V_{DD} range for the devices is from 1.6 V to 3.6 V.
2	7	GND	Analog Ground. Ground reference point for all circuitry on the devices. All analog input signals should be referred to this GND voltage.
3	6	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
5	2	SDATA	Data Out. Logic output. The conversion result from the AD7466/AD7467/AD7468 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7466 consists of four leading zeros followed by the 12 bits of conversion data, provided MSB first. The data stream from the AD7467 consists of four leading zeros followed by the 10 bits of conversion data, provided MSB first. The data stream from the AD7468 consists of four leading zeros followed by the 8 bits of conversion data, provided MSB first.
4	3	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the parts. This clock input is also used as the clock source for the conversion process of the parts.
	4, 5	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

DYNAMIC PERFORMANCE CURVES

Figure 6, Figure 7, and Figure 8 show typical FFT plots for the AD7466, AD7467, and AD7468, respectively, at a 100 kSPS sample rate and a 30 kHz input tone.

Figure 9 shows the signal-to-noise and distortion ratio performance vs. input frequency for various supply voltages while sampling at 100 kSPS with an SCLK frequency of 3.4 MHz for the AD7466.

Figure 10 shows the signal-to-noise ratio (SNR) performance vs. input frequency for various supply voltages while sampling at 100 kSPS with an SCLK frequency of 3.4 MHz for the AD7466.

Figure 11 shows the total harmonic distortion (THD) vs. analog input signal frequency for various supply voltages while sampling at 100 kSPS with an SCLK frequency of 3.4 MHz for the AD7466.

Figure 12 shows the THD vs. analog input frequency for different source impedances with a supply voltage of 2.7 V, an SCLK frequency of 3.4 MHz, and sampling at a rate of 100 kSPS for the AD7466 (see the Analog Input section).

DC ACCURACY CURVES

Figure 13 and Figure 14 show typical INL and DNL performance for the AD7466.

POWER REQUIREMENT CURVES

Figure 15 shows the supply current vs. supply voltage for the AD7466 at −40°C, +25°C, and +85°C, with SCLK frequency of 3.4 MHz and a sampling rate of 100 kSPS.

Figure 16 shows the maximum current vs. supply voltage for the AD7466 with different SCLK frequencies.

Figure 17 shows the shutdown current vs. supply voltage.

Figure 18 shows the power consumption vs. throughput rate for the AD7466 with an SCLK of 3.4 MHz and different supply voltages. See the Power Consumption section for more details.

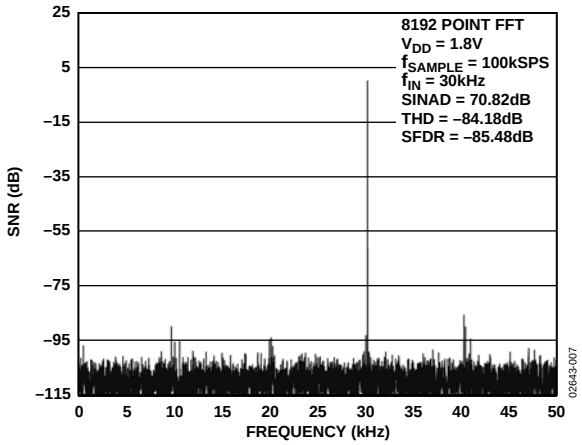


Figure 6. AD7466 Dynamic Performance at 100 kSPS

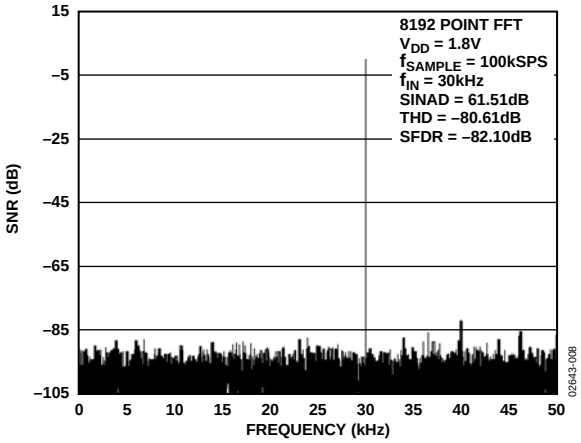


Figure 7. AD7467 Dynamic Performance at 100 kSPS

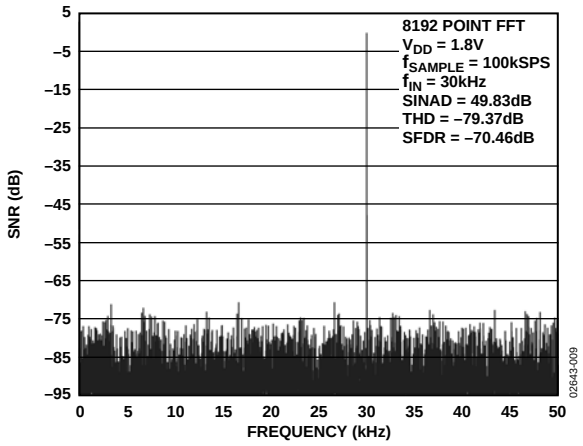


Figure 8. AD7468 Dynamic Performance at 100 kSPS

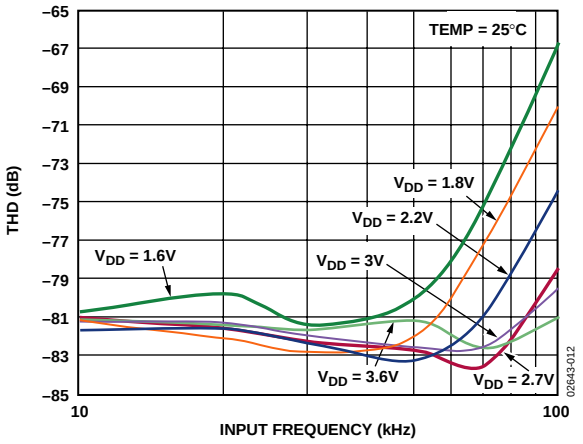


Figure 11. AD7466 THD vs. Analog Input Frequency at 100 kSPS for Various Supply Voltages

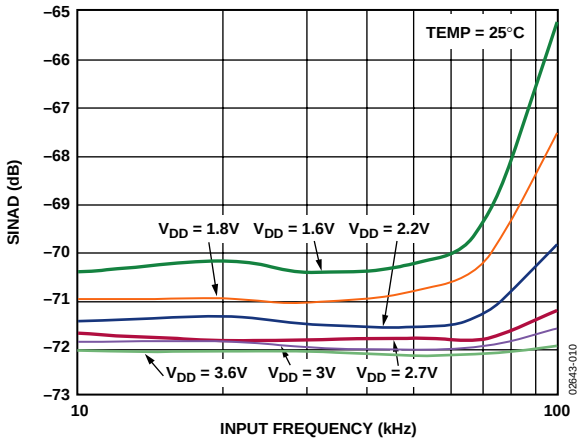


Figure 9. AD7466 SINAD vs. Analog Input Frequency at 100 kSPS for Various Supply Voltages

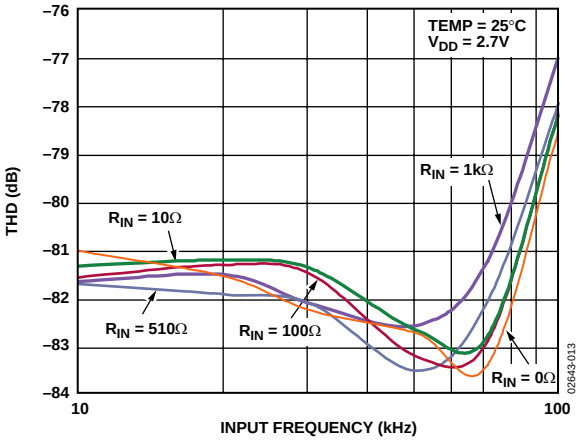


Figure 12. AD7466 THD vs. Analog Input Frequency for Various Source Impedances

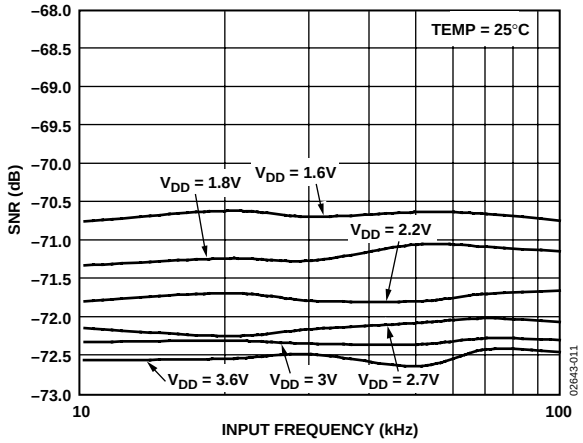


Figure 10. AD7466 SNR vs. Analog Input Frequency at 100 kSPS for Various Supply Voltages

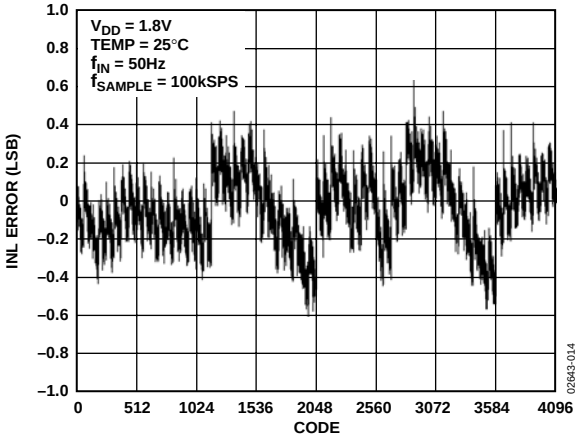


Figure 13. AD7466 INL Performance

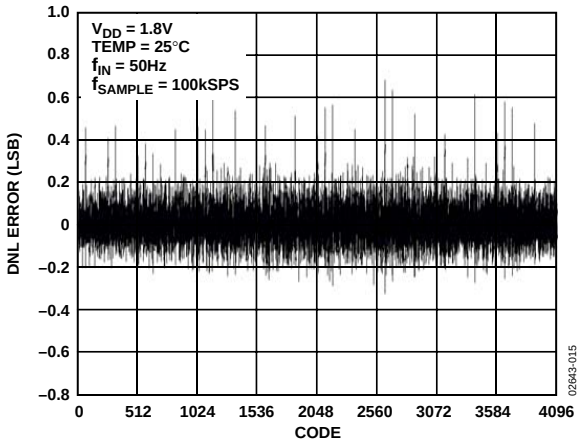


Figure 14. AD7466 DNL Performance

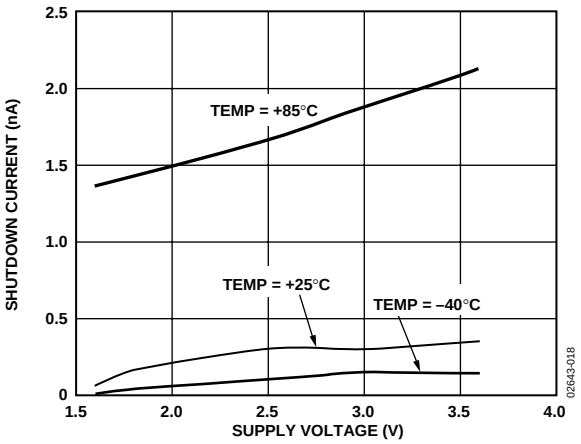


Figure 17. Shutdown Current vs. Supply Voltage

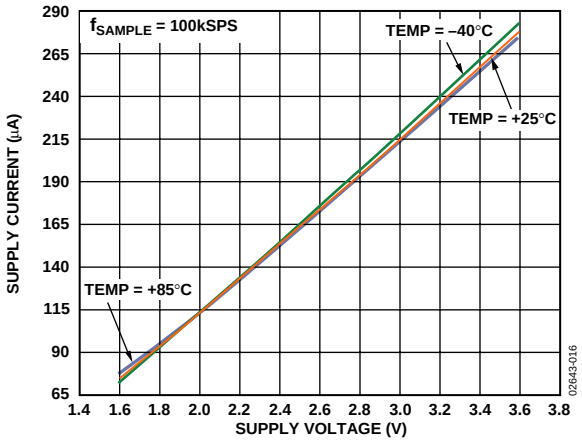


Figure 15. AD7466 Supply Current vs. Supply Voltage, SCLK 3.4 MHz

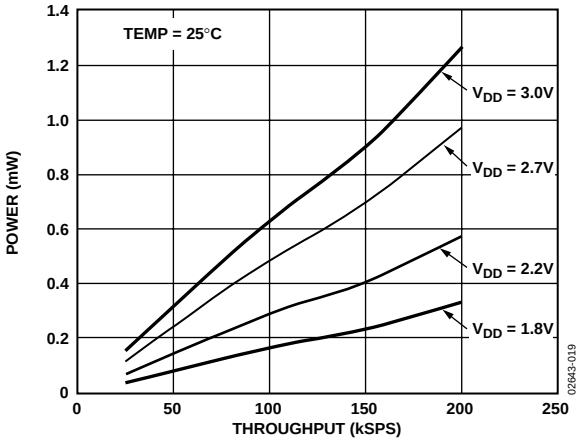


Figure 18. AD7466 Power Consumption vs. Throughput Rate, SCLK 3.4 MHz

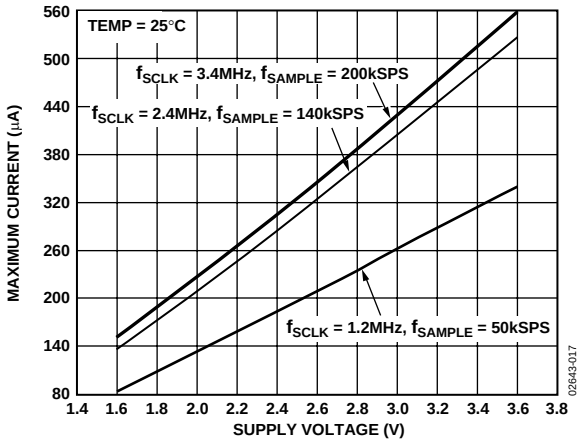


Figure 16. AD7466 Maximum Current vs. Supply Voltage for Different SCLK Frequencies

TERMINOLOGY

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7466/AD7467/AD7468, the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (that is, AGND + 1 LSB).

Gain Error
The deviation of the last code transition (111 . . . 110) to (111…111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The time required for the part to acquire a full-scale step input value within ±1 LSB, or a 30 kHz ac input value within ±0.5 LSB. The AD7466/AD7467/AD7468 enter track mode on the $\overline{CS}$ falling edge, and return to hold mode on the third SCLK falling edge. The parts remain in hold mode until the following $\overline{CS}$ falling edge. See Figure 3 and the Serial Interface section for more details.

Signal-to-Noise Ratio (SNR)
The measured ratio of signal to noise at the output of the ADC. The signal is the rms value of the sine wave input. Noise is the rms quantization error within the Nyquist bandwidth ($f_S/2$). The rms value of the sine wave is half of its peak-to-peak value divided by √2, and the rms value for the quantization noise is q/√12. The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

For an ideal N-bit converter, the SNR is defined as

$$SNR = 6.02\ N + 1.76\ \text{db}$$

Thus, for a 12-bit converter, it is 74 dB; for a 10-bit converter, it is 62 dB; and for an 8-bit converter, it is 50 dB.

However, in practice, various error sources in the ADCs cause the measured SNR to be less than the theoretical value. These errors occur due to integral and differential nonlinearities, internal ac noise sources, and so on.

Signal-to-Noise and Distortion Ratio (SINAD)
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics, but excluding dc.

Total Unadjusted Error (TUE)
A comprehensive specification that includes gain error, linearity error, and offset error.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7466/AD7467/AD7468, it is defined as

$$THD\,(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
The ratio of the rms value of the next-largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7466/AD7467/AD7468 are tested using the CCIF standard where two input frequencies are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dB.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7466/AD7467/AD7468 are fast, micropower, 12-bit, 10-bit, and 8-bit ADCs, respectively. The parts can be operated from a 1.6 V to 3.6 V supply. When operated from any supply voltage within this range, the AD7466/AD7467/AD7468 are capable of throughput rates of 200 kSPS when provided with a 3.4 MHz clock.

The AD7466/AD7467/AD7468 provide the user with an on-chip track-and-hold, an ADC, and a serial interface housed in a tiny 6-lead SOT-23 or an 8-lead MSOP package, which offer the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part, but also provides the clock source for the successive approximation ADC. The analog input range is 0 V to V_{DD}. An external reference is not required for the ADC, and there is no on-chip reference. The reference for the AD7466/AD7467/AD7468 is derived from the power supply, thus giving the widest possible dynamic input range.

The AD7466/AD7467/AD7468 also feature an automatic power-down mode to allow power savings between conversions. The power-down feature is implemented across the standard serial interface, as described in the Normal Mode section.

CONVERTER OPERATION

The AD7466/AD7467/AD7468 are successive approximation analog-to-digital converters based around a charge redistribution DAC. Figure 19 and Figure 20 show simplified schematics of the ADC. Figure 19 shows the ADCs during the acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

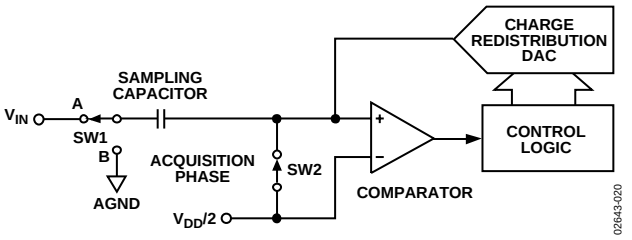


Figure 19. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 20, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 21 shows the ADC transfer function.

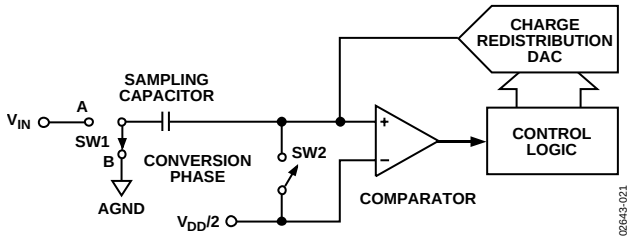


Figure 20. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7466/AD7467/AD7468 is straight binary. The designed code transitions occur at successive integer LSB values; that is, 1 LSB, 2 LSB, and so on. The LSB size for the devices is as follows:

$V_{DD}/4096$ for the AD7466

$V_{DD}/1024$ for the AD7467

$V_{DD}/256$ for the AD7468

The ideal transfer characteristics for the devices are shown in Figure 21.

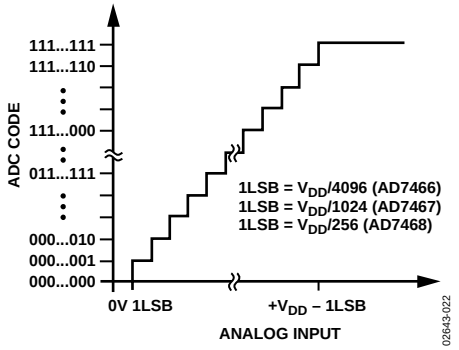


Figure 21. AD7466/AD7467/AD7468 Transfer Characteristics

TYPICAL CONNECTION DIAGRAM

Figure 22 shows a typical connection diagram for the devices. V_{REF} is taken internally from V_{DD} and, therefore, V_{DD} should be well decoupled. This provides an analog input range of 0 V to V_{DD}.

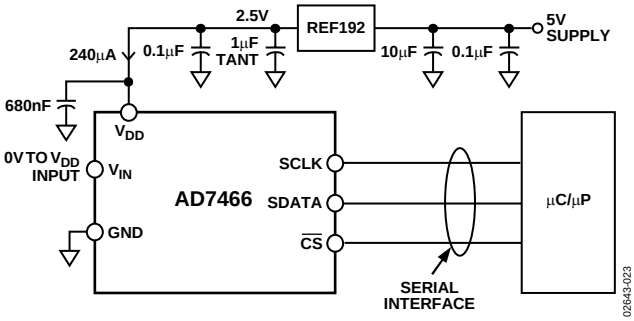


Figure 22. REF192 as Power Supply to AD7466

The conversion result consists of four leading zeros followed by the MSB of the 12-bit, 10-bit, or 8-bit result from the AD7466, AD7467, or AD7468, respectively. See the Serial Interface section. Alternatively, because the supply current required by the AD7466/AD7467/AD7468 is so low, a precision reference can be used as the supply source to the devices.

The REF19x series devices are precision micropower, low drop-out voltage references. For the AD7466/AD7467/AD7468 voltage range operation, the REF193, REF192, and REF191 can be used to supply the required voltage to the ADC, delivering 3 V, 2.5 V, and 2.048 V, respectively (see Figure 22). This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at a value other than 3 V or 2.5 V (for example, 5 V). The REF19x outputs a steady voltage to the AD7466/AD7467/AD7468. If the low dropout REF192 is used when the AD7466 is converting at a rate of 100 kSPS, the REF192 needs to supply a maximum of 240 μA to the AD7466. The load regulation of the REF192 is typically 10 ppm/mA (REF192, V_S = 5 V), which results in an error of 2.4 ppm (6 μV) for the 240 μA drawn from it. This corresponds to a 0.0098 LSB error for the AD7466 with V_{DD} = 2.5 V from the REF192. For applications where power consumption is important, the automatic power-down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See the Normal Mode section.

Table 7 provides some typical performance data with various references used as a V_{DD} source under the same setup conditions. The ADR318, for instance, is a 1.8 V band gap voltage reference. Its tiny footprint, low power consumption, and additional shutdown capability make the ADR318 ideal for battery-powered applications.

Table 7. AD7466 Performance for Voltage Reference IC

Reference Tied to V_{DD}	AD7466 SNR Performance (dB)
ADR318 @ 1.8 V	70.73
ADR370 @ 2.048 V	70.72
ADR421 @ 2.5 V	71.13
ADR423 @ 3 V	71.44

ANALOG INPUT

An equivalent circuit of the AD7466/AD7467/AD7468 analog input structure is shown in Figure 23. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This causes these diodes to become forward-biased and to start conducting current into the substrate. Capacitor C1 in Figure 23 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 200 Ω. Capacitor C2 is the ADC sampling capacitor with a typical capacitance of 20 pF.

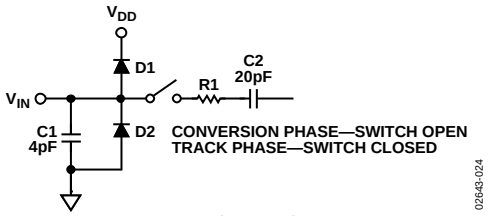


Figure 23. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal by using a band-pass filter on the relevant analog input pin is recommended. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This might necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

Table 8 provides typical performance data for various op amps used as the input buffer under constant setup conditions.

Table 8. AD7466 Performance for Input Buffers

Op Amp in the Input Buffer	AD7466 SNR Performance (dB) 30 kHz Input, V_{DD} = 1.8 V
AD8510	70.75
AD8610	71.45
AD797	71.42

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 12 shows a graph of THD vs. analog input signal frequency for different source impedances when using a supply voltage of 2.7 V and sampling at a rate of 100 kSPS.

DIGITAL INPUTS

The digital inputs applied to the AD7466/AD7467/AD7468 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog input. For example, if the AD7466/AD7467/AD7468 are operated with a V_{DD} of 3 V, 5 V logic levels could be used on the digital inputs. However, the data output on SDATA still has 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK is applied before V_{DD}, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V is applied prior to V_{DD}.

NORMAL MODE

The AD7466/AD7467/AD7468 automatically enter power-down at the end of each conversion. This mode of operation is designed to provide flexible power management options and to optimize the power dissipation/throughput rate ratio for low power application requirements. Figure 24 shows the general operation of the AD7466/AD7467/AD7468. On the $\overline{CS}$ falling edge, the part begins to power up and the track-and-hold, which was in hold while the part was in power-down, goes into track mode. The conversion is also initiated at this point. On the third SCLK falling edge after the $\overline{CS}$ falling edge, the track-and-hold returns to hold mode.

For the AD7466, 16 serial clock cycles are required to complete the conversion and access the complete conversion result. The AD7466 automatically enters power-down mode on the 16th SCLK falling edge.

For the AD7467, 14 serial clock cycles are required to complete the conversion and access the complete conversion result. The AD7467 automatically enters power-down mode on the 14th SCLK falling edge.

For the AD7468, 12 serial clock cycles are required to complete the conversion and access the complete conversion result.

The AD7468 automatically enters power-down mode on the 12th SCLK falling edge.

The AD7466 also enters power-down mode if $\overline{CS}$ is brought high any time before the 16th SCLK falling edge. The conversion that was initiated by the $\overline{CS}$ falling edge terminates and SDATA goes back into three-state. This also applies for the AD7467 and AD7468; if $\overline{CS}$ is brought high before the conversion is complete (the 14th SCLK falling edge for the AD7467, and the 12th SCLK falling edge for the AD7468), the part enters power-down, the conversion terminates, and SDATA goes back into three-state.

Although $\overline{CS}$ can idle high or low between conversions, bringing $\overline{CS}$ high once the conversion is complete is recommended to save power.

When supplies are first applied to the devices, a dummy conversion should be performed to ensure that the parts are in power-down mode, the track-and-hold is in hold mode, and SDATA is in three-state.

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed, by bringing $\overline{CS}$ low again.

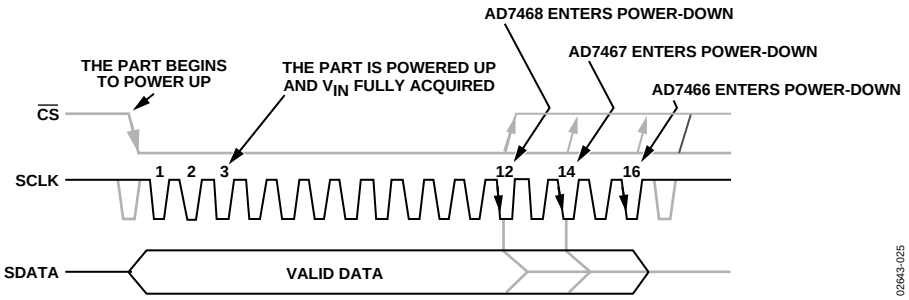


Figure 24. Normal Mode Operation

POWER CONSUMPTION

The AD7466/AD7467/AD7468 automatically enter power-down mode at the end of each conversion or if $\overline{CS}$ is brought high before the conversion is finished.

When the AD7466/AD7467/AD7468 are in power-down mode, all the analog circuitry is powered down and the current consumption is typically 8 nA.

To achieve the lowest power dissipation, there are some considerations the user should keep in mind.

The conversion time is determined by the serial clock frequency; the faster the SCLK frequency, the shorter the conversion time. This implies that as the frequency increases, the part dissipates power for a shorter period of time when the conversion is taking place, and it remains in power-down mode for a longer percentage of the cycle time or throughput rate.

Figure 26 shows two AD7466s running with two different SCLK frequencies, SCLK A and SCLK B, with SCLK A having the higher SCLK frequency. For the same throughput rate, the AD7466 using SCLK A has a shorter conversion time than the AD7466 using SCLK B, and it remains in power-down mode longer. The current consumption in power-down mode is very low; thus, the average power consumption is greatly reduced.

This reduced power consumption can be seen in Figure 25, which shows the supply current vs. SCLK frequency for various supply voltages at a throughput rate of 100 kSPS. For a fixed throughput rate, the supply current (average current) drops as the SCLK frequency increases because the part is in power-down mode most of the time. It can also be seen that, for a lower supply voltage, the supply current drops accordingly.

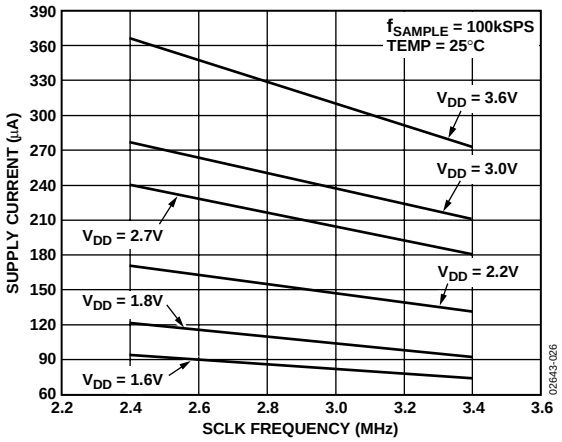


Figure 25. Supply Current vs. SCLK Frequency for a Fixed Throughput Rate and Different Supply Voltages

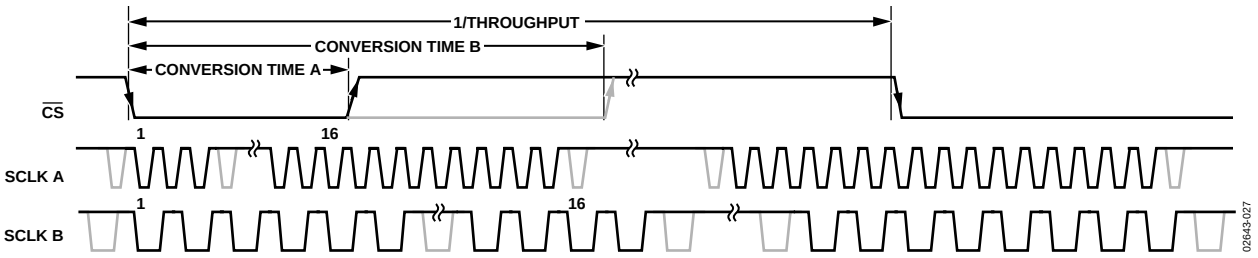


Figure 26. Conversion Time Comparison for Different SCLK Frequencies and a Fixed Throughput Rate

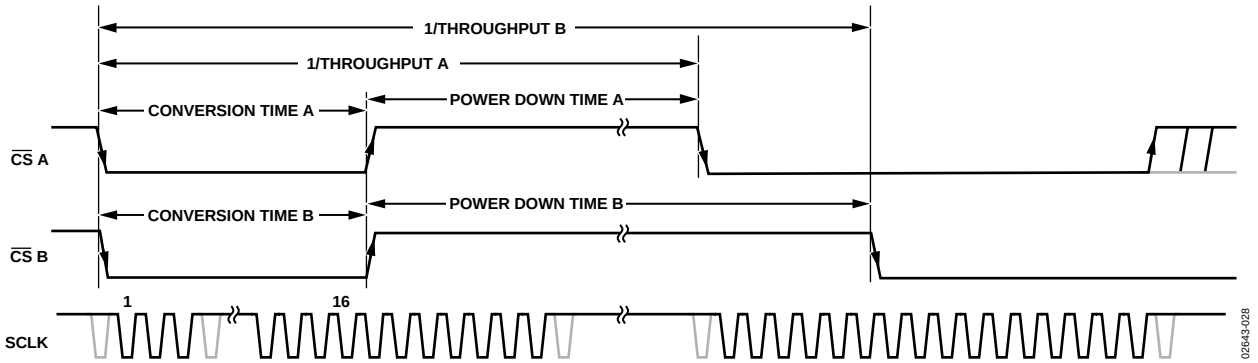


Figure 27. Conversion Time vs. Power-Down Time for a Fixed SCLK Frequency and Different Throughput Rates

Figure 18 shows power consumption vs. throughput rate for a 3.4 MHz SCLK frequency. In this case, the conversion time is the same for all cases because the SCLK frequency is a fixed parameter. Low throughput rates lead to lower current consumptions, with a higher percentage of the time in power-down mode. Figure 27 shows two AD7466s running with the same SCLK frequency, but at different throughput rates. The A throughput rate is higher than the B throughput rate. The slower the throughput rate, the longer the period of time the part is in power-down mode, and the average power consumption drops accordingly.

Figure 28 shows the power vs. throughput rate for different supply voltages and SCLK frequencies. For this plot, all the elements regarding power consumption that were explained previously (the influence of the SCLK frequency, the influence of the throughput rate, and the influence of the supply voltage) are taken into consideration.

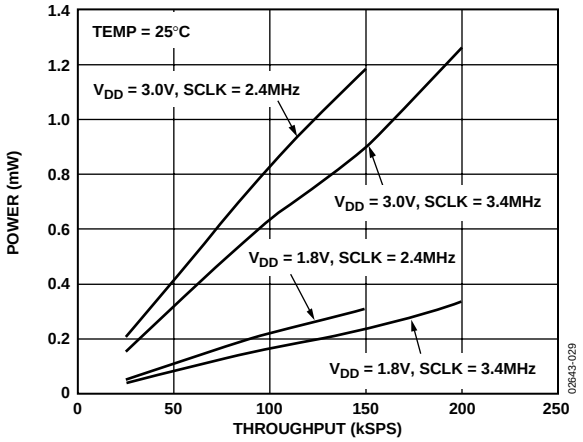


Figure 28. Power vs. Throughput Rate for Different SCLK and Supply Voltages

The following examples show calculations for the information in this section.

Power Consumption Example 1

This example shows that, for a fixed throughput rate, as the SCLK frequency increases, the average power consumption drops. From Figure 26, for SCLK A = 3.4 MHz, SCLK B = 1.2 MHz, and a throughput rate of 50 kSPS, which gives a cycle time of 20 µs, the following values can be obtained:

Conversion Time A = 16 × (1/*SCLK A*) = 4.7 µs (23.5% of the cycle time)

Power-Down Time A = (1/*Throughput*) − *Conversion Time A* = 20 µs − 4.7 µs = 15.3 µs (76.5% of the cycle time)

Conversion Time B = 16 × (1/*SCLK B*) = 13 µs (65% of the cycle time)

Power-Down Time B = (1/*Throughput*) − *Conversion Time B* = 20 µs − 13 µs = 7 µs (35% of the cycle time)

The average power consumption includes the power dissipated when the part is converting and the power dissipated when the part is in power-down mode. The average power dissipated during conversion is calculated as the percentage of the cycle time spent when converting, multiplied by the maximum current during conversion. The average power dissipated in power-down mode is calculated as the percentage of cycle time spent in power-down mode, multiplied by the current figure for power-down mode. In order to obtain the value for the average power, these terms must be multiplied by the voltage.

Considering the maximum current for each SCLK frequency for V_{DD} = 1.8 V,

Power Consumption A = ((4.7/20) × 186 µA + (15.3/20) × 100 nA) × 1.8 V = (43.71 + 0.076) µA × 1.8 V = 78.8 µW = 0.07 mW

Power Consumption B = ((13/20) × 108 µA + (7/20) × 100 nA) × 1.8 V = (70.2 + 0.035) µA × 1.8 V = 126.42 µW = 0.126 mW

It can be concluded that for a fixed throughput rate, the average power consumption drops as the SCLK frequency increases.

Power Consumption Example 2

This example shows that, for a fixed SCLK frequency, as the throughput rate decreases, the average power consumption drops. From Figure 27, for SCLK = 3.4 MHz, Throughput A = 100 kSPS (which gives a cycle time of 10 µs), and Throughput B = 50 kSPS (which gives a cycle time of 20 µs), the following values can be obtained:

Conversion Time A = 16 × (1/*SCLK*) = 4.7 µs (47% of the cycle time for a throughput of 100 kSPS)

Power-Down Time A = (1/*Throughput A*) − *Conversion Time A* = 10 µs − 4.7 µs = 5.3 µs (53% of the cycle time)

Conversion Time B = 16 × (1/*SCLK*) = 4.7 µs (23.5% of the cycle time for a throughput of 50 kSPS)

Power-Down Time B = (1/*Throughput B*) − *Conversion Time B* = 20 µs − 4.7 µs = 15.3 µs (76.5% of the cycle time)

The average power consumption is calculated as explained in Power Consumption Example 1, considering the maximum current for a 3.4 MHz SCLK frequency for V_{DD} = 1.8 V.

Power Consumption A = ((4.7/10) × 186 µA + (5.3/10) × 100 nA) × 1.8 V= (87.42 + 0.053) µA × 1.8 V = 157.4 µW = 0.157 mW

Power Consumption B = ((4.7/20) × 186 µA + (15.3/20) × 100 nA) × 1.8 V = (43.7 + 0.076) µA × 1.8 V = 78.79 µW = 0.078 mW

It can be concluded that for a fixed SCLK frequency, the average power consumption drops as the throughput rate decreases.

SERIAL INTERFACE

Figure 29, Figure 30, and Figure 31 show the timing diagrams for serial interfacing to the AD7466/AD7467/AD7468. The serial clock provides the conversion clock and controls the transfer of information from the ADC during a conversion.

The part begins to power up on the $\overline{CS}$ falling edge. The falling edge of $\overline{CS}$ puts the track-and-hold into track mode and takes the bus out of three-state. The conversion is also initiated at this point. On the third SCLK falling edge after the $\overline{CS}$ falling edge, the part should be powered up fully at Point B, as shown in Figure 29, and the track-and-hold returns to hold.

For the AD7466, the SDATA line goes back into three-state and the part enters power-down on the 16th SCLK falling edge. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs elapse, the conversion terminates, the SDATA line goes back into three-state, and the part enters power-down; otherwise SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 29. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7466.

For the AD7467, the 14th SCLK falling edge causes the SDATA line to go back into three-state, and the part enters power-down. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs elapse, the conversion terminates, the SDATA line goes back into three-state, and the AD7467 enters power-down; otherwise SDATA returns to three-state on the 14th SCLK falling edge, as shown in Figure 30. Fourteen serial clock cycles are required to perform the conversion process and to access data from the AD7467.

For the AD7468, the 12th SCLK falling edge causes the SDATA line to go back into three-state, and the part enters power-down. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs elapse, the conversion terminates, the SDATA line goes back into three-state, and the AD7468 enters power-down; otherwise SDATA returns to three-state on the 12th SCLK falling edge, as shown in Figure 31. Twelve serial clock cycles are required to perform the conversion process and to access data from the AD7468.

$\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero; thus, the first clock falling edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. For the AD7466, the final bit in the data transfer is valid on the 16th SCLK falling edge, having been clocked out on the previous (15th) SCLK falling edge.

In applications with a slow SCLK, it is possible to read in data on each SCLK rising edge. In such a case, the first falling edge of SCLK after the $\overline{CS}$ falling edge clocks out the second leading zero and can be read in the following rising edge. If the first SCLK edge after the $\overline{CS}$ falling edge is a falling edge, the first leading zero that was clocked out when $\overline{CS}$ went low is missed, unless it is not read on the first SCLK falling edge. The 15th falling edge of SCLK clocks out the last bit, and it can be read in the following rising SCLK edge.

If the first SCLK edge after the $\overline{CS}$ falling edge is a rising edge, $\overline{CS}$ clocks out the first leading zero, and it can be read on the SCLK rising edge. The next SCLK falling edge clocks out the second leading zero, and it can be read on the following rising edge.

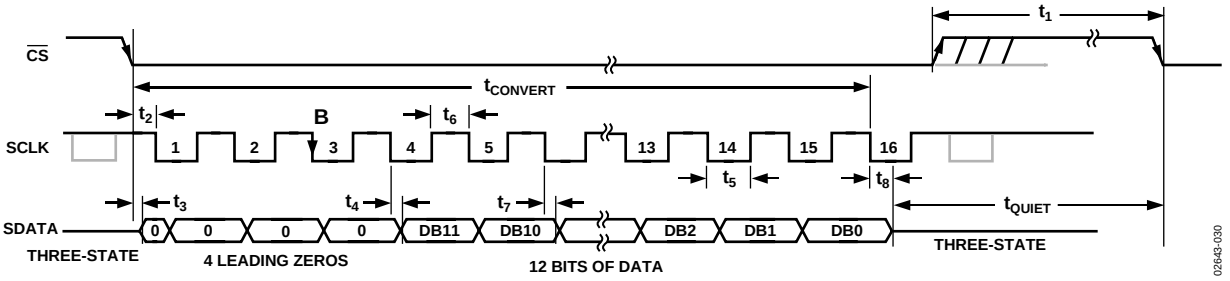


Figure 29. AD7466 Serial Interface Timing Diagram

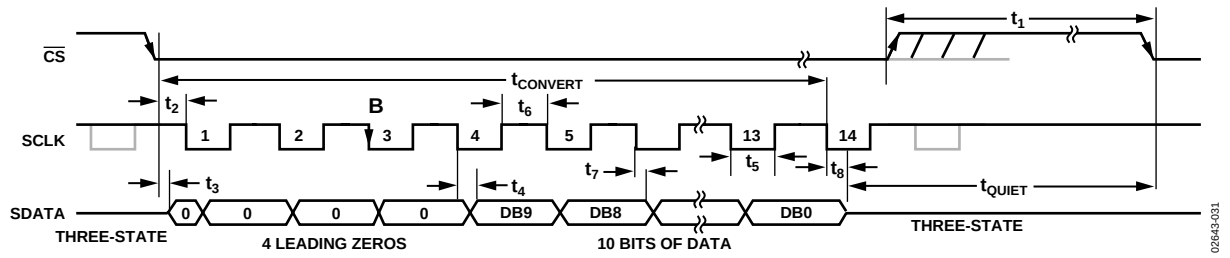


Figure 30. AD7467 Serial Interface Timing Diagram

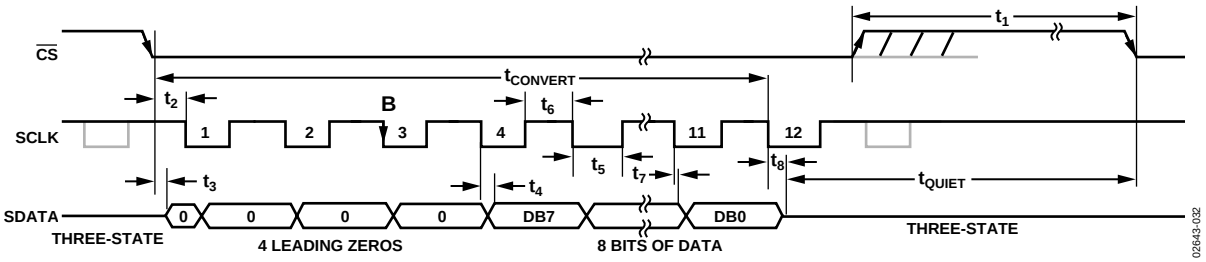


Figure 31. AD7468 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7466/AD7467/AD7468 allows the parts to be connected directly to many different microprocessors. This section explains how to interface the AD7466/AD7467/AD7468 with some of the more common microcontroller and DSP serial interface protocols.

AD7466/AD7467/AD7468 to TMS320C541 Interface

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7466/AD7467/AD7468. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD74xx devices, without requiring any glue logic. The serial port of the TMS320C541 is set up to operate in burst mode (FSM = 1 in the serial port control register, SPC) with internal CLKX (MCM = 1 in the SPC register) and internal frame signal (TXM = 1 in the SPC register), so both pins are configured as outputs. For the AD7466, the word length should be set to 16 bits (FO = 0 in the SPC register). The standard synchronous serial port interface in this DSP allows only frames with a word length of 16 bits or 8 bits. Therefore, for the AD7467 and AD7468 where 14 and 12 bits are required, the FO bit also would be set up to 16 bits. In these cases, the user should keep in mind that the last 2 bits and 4 bits for the AD7467 and AD7468, respectively, are invalid data as the SDATA line goes back into three-state on the 14th and 12th SCLK falling edge.

To summarize, the values in the SPC register are FO = 0, FSM = 1, MCM = 1, and TXM = 1.

Figure 32 shows the connection diagram. For signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provide equidistant sampling.

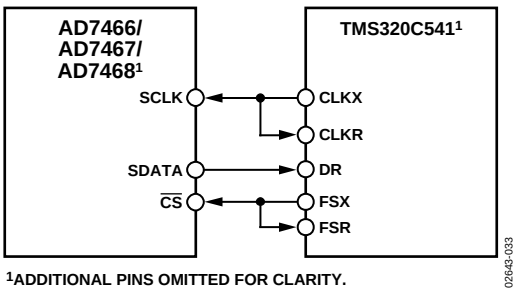


Figure 32. Interfacing to the TMS320C541

AD7466/AD7467/AD7468 to ADSP-218x Interface

The ADSP-218x family of DSPs is interfaced directly to the AD7466/AD7467/AD7468 without any glue logic. The SPORT control register must be set up as described in Table 9.

Table 9. SPORT Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternate framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right-justify data
ISCLK = 1	Internal serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	Sets up RFS as an input
ITFS = 1	Sets up TFS as an output
SLEN = 1111	16 bits for the AD7466
SLEN = 1101	14 bits for the AD7467
SLEN = 1011	12 bits for the AD7468

The connection diagram in Figure 33 shows how the ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode, and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling might not be achieved.

The timer registers, for example, are loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and, therefore, the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK goes high, low, and high again before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data can be transmitted, or it can wait until the next clock edge.

For example, the ADSP-2181 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, an SCLK of 2 MHz is obtained, and eight master clock periods elapse for every SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs occur between interrupts and, subsequently, between transmit instructions. This situation results in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling is implemented by the DSP.

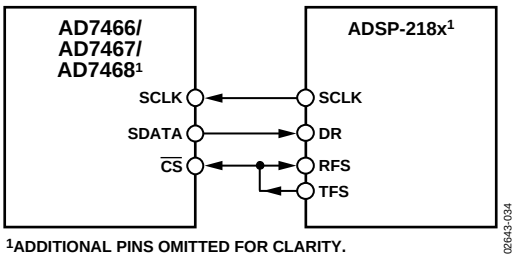


Figure 33. Interfacing to the ADSP-218x

AD7466/AD7467/AD7468 to DSP563xx Interface

The connection diagram in Figure 34 shows how the AD7466/AD7467/AD7468 can be connected to the synchronous serial interface (SSI) of the DSP563xx family of DSPs from Motorola. The SSI is operated in synchronous mode and normal mode (SYN = 1 and MOD = 0 in Control Register B, CRB) with an internally generated word frame sync for both Tx and Rx (Bit FSL1 = 0 and Bit FSL0 = 0 in the CRB register). Set the word length in Control Register A (CRA) to 16 by setting Bits WL2 = 0, WL1 = 1, and WL0 = 0 for the AD7466. The word length for the AD7468 can be set to 12 bits (WL2 = 0, WL1 = 0, and WL0 = 1). This DSP does not offer the option for a 14-bit word length, so the AD7467 word length is set up to 16 bits like the AD7466 word length. In this case, the user should keep in mind that the last two bits are invalid data because the SDATA goes back into three-state on the 14th SCLK falling edge.

The frame sync polarity bit (FSP) in the CRB register can be set to 1, which means the frame goes low and a conversion starts. Likewise, by means of Bits SCD2, SCKD, and SHFD in the CRB register, it is established that Pin SC2 (the frame sync signal) and Pin SCK in the serial port are configured as outputs, and the most significant bit (MSB) is shifted first. To summarize,

MOD = 0
SYN = 1
WL2, WL1, WL0 depend on the word length
FSL1 = 0, FSL0 = 0
FSP = 1, negative frame sync
SCD2 = 1
SCKD = 1
SHFD = 0

For signal processing applications, it is imperative that the frame synchronization signal from the DSP563xx provides equidistant sampling.

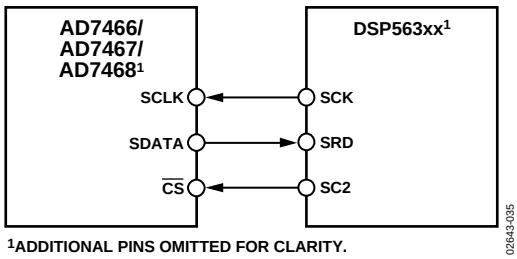


Figure 34. Interfacing to the DSP563xx

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7466/AD7467/AD7468 should be designed such that the analog and digital sections are separated and confined to certain areas. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined at only one place. If the devices are in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7466/AD7467/AD7468.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7466/AD7467/AD7468 to avoid noise coupling. The power supply lines to the devices should use as large a trace as possible to provide low impedance paths and to reduce the effects of glitches on the power-supply line. Fast switching signals, like clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough on the board. A microstrip technique is the best choice, but is not always possible with a double-sided board. With this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

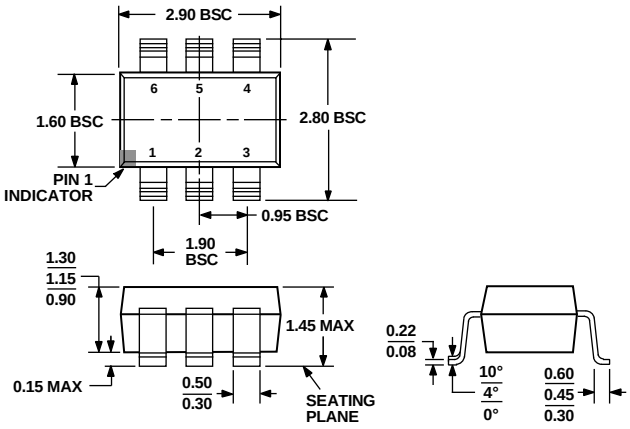
Good decoupling is also very important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. All digital supplies should have a 0.1 µF ceramic disc capacitor to DGND. To achieve the best performance from these decoupling components, the user should keep the distance between the decoupling capacitor and the V_{DD} and GND pins to a minimum, with short track lengths connecting the respective pins.

EVALUATING THE PERFORMANCE OF THE AD7466 AND AD7467

The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via an evaluation board controller. To evaluate the ac and dc performance of the AD7466 and AD7467, the evaluation board controller can be used in conjunction with the AD7466/AD7467CB evaluation board and other Analog Devices evaluation boards ending in the CB designator.

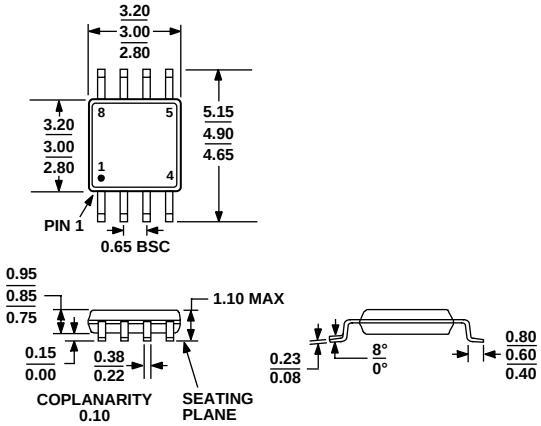
The software allows the user to perform ac tests (fast Fourier transform) and dc tests (histogram of codes) on the AD7466 and AD7467. See the data sheet in the evaluation board package for more information.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 35. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Description	Package Option	Branding
AD7466BRT-REEL7	−40°C to +85°C	±1.5 max	6-Lead SOT-23	RJ-6	CLB
AD7466BRT-R2	−40°C to +85°C	±1.5 max	6-Lead SOT-23	RJ-6	CLB
AD7466BRTZ-REEL[2]	−40°C to +85°C	±1.5 max	6-Lead SOT-23	RJ-6	C2T
AD7466BRTZ-REEL7[2]	−40°C to +85°C	±1.5 max	6-Lead SOT-23	RJ-6	C2T
AD7466BRTZ-R2[2]	−40°C to +85°C	±1.5 max	6-Lead SOT-23	RJ-6	C2T
AD7466BRM	−40°C to +85°C	±1.5 max	8-Lead MSOP	RM-8	CLB
AD7466BRM-REEL	−40°C to +85°C	±1.5 max	8-Lead MSOP	RM-8	CLB
AD7466BRM-REEL7	−40°C to +85°C	±1.5 max	8-Lead MSOP	RM-8	CLB
AD7466BRMZ[2]	−40°C to +85°C	±1.5 max	8-Lead MSOP	RM-8	CLB#
AD7466BRMZ-REEL[2]	−40°C to +85°C	±1.5 max	8-Lead MSOP	RM-8	CLB#
AD7466BRMZ-REEL7[2]	−40°C to +85°C	±1.5 max	8-Lead MSOP	RM-8	CLB#
AD7467BRT-REEL	−40°C to +85°C	±0.5 max	6-Lead SOT-23	RJ-6	CMB
AD7467BRT-REEL7	−40°C to +85°C	±0.5 max	6-Lead SOT-23	RJ-6	CMB
AD7467BRT-R2	−40°C to +85°C	±0.5 max	6-Lead SOT-23	RJ-6	CMB
AD7467BRTZ-REEL[2]	−40°C to +85°C	±0.5 max	6-Lead SOT-23	RJ-6	CMB#
AD7467BRTZ-REEL7[2]	−40°C to +85°C	±0.5 max	6-Lead SOT-23	RJ-6	CMB#
AD7467BRTZ-R2[2]	−40°C to +85°C	±0.5 max	6-Lead SOT-23	RJ-6	CMB#
AD7467BRM	−40°C to +85°C	±0.5 max	8-Lead MSOP	RM-8	CMB
AD7467BRM-REEL	−40°C to +85°C	±0.5 max	8-Lead MSOP	RM-8	CMB
AD7467BRM-REEL7	−40°C to +85°C	±0.5 max	8-Lead MSOP	RM-8	CMB
AD7467BRMZ[2]	−40°C to +85°C	±0.5 max	8-Lead MSOP	RM-8	CMU
AD7468BRT-REEL	−40°C to +85°C	±0.2 max	6-Lead SOT-23	RJ-6	CNB
AD7468BRT-REEL7	−40°C to +85°C	±0.2 max	6-Lead SOT-23	RJ-6	CNB
AD7468BRT-R2	−40°C to +85°C	±0.2 max	6-Lead SOT-23	RJ-6	CNB
AD7468BRTZ-REEL[2]	−40°C to +85°C	±0.2 max	6-Lead SOT-23	RJ-6	CNU#
AD7468BRTZ-REEL7[2]	−40°C to +85°C	±0.2 max	6-Lead SOT-23	RJ-6	CNU#
AD7468BRM	−40°C to +85°C	±0.2 max	8-Lead MSOP	RM-8	CNB
AD7468BRM-REEL	−40°C to +85°C	±0.2 max	8-Lead MSOP	RM-8	CNB
AD7468BRM-REEL7	−40°C to +85°C	±0.2 max	8-Lead MSOP	RM-8	CNB
AD7468BRMZ[2]	−40°C to +85°C	±0.2 max	8-Lead MSOP	RM-8	CNU#
AD7468BRMZ-REEL[2]	−40°C to +85°C	±0.2 max	8-Lead MSOP	RM-8	CNU#
AD7468BRMZ-REEL7[2]	−40°C to +85°C	±0.2 max	8-Lead MSOP	RM-8	CNU#
EVAL-AD7466CB[3]			Evaluation Board		
EVAL-AD7467CB[3]			Evaluation Board		
EVAL-CONTROL BRD2[4]			Control Board		

[1] Linearity error refers to integral nonlinearity.
[2] Z = RoHS Compliant Part, # denotes lead-free product may be top or bottom marked.
[3] This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[4] This board is a complete unit that allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designator. For a complete evaluation kit, order a particular ADC evaluation board (such as EVAL-AD7466CB), the EVAL-CONTROL BRD2, and a 12 V ac transformer. See relevant evaluation board data sheets for more information.

NOTES