SPECIFICATIONS

V_{DD} = 7.5 V to 30 V, V_{SS} = 0 V, D_{VCC} = A_{VCC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.25 V, T_A = -40°C to 105°C, unless otherwise noted

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY [Vin(0) to Vin(6)][2]					
Resolution	12			Bits	No Missing Codes
Integral Nonlinearity			±1	LSB	
Differential Nonlinearity			±1	LSB	
Offset Error		1		LSB	
Offset Error Drift		3		ppm/°C	
Offset Error Match		1		LSB	
Gain Error		1		LSB	
Gain Error Drift		2		ppm/°C	
Gain Error Match		1		LSB	
ADC Unadjusted Error[3,4]		0.05	0.1	%	-40°C to 85°C
		0.08	0.3	%	-40°C to 105°C
Total Unadjusted Error[5,6]		0.07	0.2	%	-40°C to 85°C
		0.1	0.5	%	-40°C to 105°C
ANALOG INPUTS [Vin(0) to Vin(6)]					
Pseudo Differential Input Voltage					
Vin(n) – Vin(n-1)	1V		$2V_{REF}$	V	
Absolute Input Voltage	V_{CM} - V_{REF}		V_{CM} + V_{REF}	V	
Common Mode Input Voltage	0.5		27.5	V	
DC Leakage Current		±70		nA	$\overline{\text{CNVST}}$ pulse every 100ms
Input Capacitance		15		pF	When in track
		3		pF	When in hold
DC ACCURACY [VT1 to VT6][2]					
Resolution	12			Bits	No Missing Codes
Integral Nonlinearity			±1	LSB	
Differential Nonlinearity			±1	LSB	
Offset Error		2		LSB	
Offset Error Drift		2		ppm/°C	
Offset Error Match		2		LSB	
Gain Error		2		LSB	
Gain Error Drift		1.2		ppm/°C	
Gain Error Match		2		LSB	
ADC Unadjusted Error[7]		0.1	0.2	%	-40°C to 85°C
		0.16	0.6	%	-40°C to 105°C
Total Unadjusted Error[8]		0.15	0.4	%	-40°C to 85°C
		0.2	1	%	-40°C to 105°C
ANALOG INPUTS (VT1 to VT6)					
Input Voltage Range	0		$2V_{REF}$	V	
Leakage Current		±70		nA	$\overline{\text{CNVST}}$ pulse every 100ms
Input Capacitance		15		pF	When in track
		3		pF	When in hold
DYNAMIC PERFORMANCE					
Common Mode Rejection Ratio [CMRR]		-75		dB	Up to 10kHz ripple frequency

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE					
Reference Voltage	2.495	2.5	2.505	V	V_{REF} @ 25°C
Reference Temperature Coefficient		±3	±15	ppm/°C	-40 °C to +85 °C
Output Voltage Hysteresis		50		ppm	-40 °C to +85 °C
Long Term Drift		100		ppm/1000 Hours	
Line Regulation		±15		ppm/V	AVDD =7.5V
Turn-On Settling Time		10		ms	V_{REF} = 10uF , C_{REF} = 100nF
REGULATOR OUTPUT					
Input Voltage Range	7.5		30	V	
Output Voltage V_{REG}	4.75	5	5.25	V	
Output Current[9]	5			mA	
Line Regulation		0.4		mV/V	
Load Regulation		2.5		mV/mA	
Output Noise Voltage		700		uV	
Internal Short Protection Limit		20		mA	For a 10 Ohm short
CELL BALANCING OUTPUTS[10]					
Output High Voltage, V_{OH}	4	5	5.25	V	For a 80pF load, I_{SOURCE} = 40 nA
Output Low Voltage, V_{OL}	0			V	
CB1 Output ramp up time[11]		5		us	For a 80pF load
CB1 Output ramp down time[12]		50		ns	For a 80pF load
CB2-CB6 Output ramp up time[11]		350		us	For a 80pF load
CB2-CB6 Output ramp down time[12]		10		us	For a 80pF load
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.4	V	
Input Current, I_{IN}			±1	µA	
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} * 0.9			V	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance		5		pF	
Output Coding	Straight natural binary				
POWER REQUIREMENTS					
V_{DD}	7.5		30	V	
I_{DD} During Conversion		7	10	mA	V_{DD} = 30 V
I_{DD} During Data Readback		5	8	mA	V_{DD} = 30 V
I_{DD} During Cell Balancing		4.5	6	mA	V_{DD} = 30 V
I_{DD} Software Powerdown		1.8	2.5	mA	V_{DD} = 30 V
I_{DD} Full Powerdown Mode			4	µA	V_{DD} = 30 V
POWER DISSIPATION					
During Conversion			300	mW	V_{DD} = 30 V
During Data Readback			240	mW	V_{DD} = 30 V
During Cell Balancing			180	mW	V_{DD} = 30 V
Software Powerdown			75	mW	V_{DD} = 30 V
Full Powerdown Mode			120	µW	V_{DD} = 30 V

[1] Temperature range is −40°C to +105°C.
[2] For dc accuracy specifications, the LSB size for cell voltage measurements is ($2V_{REF}$-1V)/4096, the LSB size for temperature measurements is $2V_{REF}$/4096.
[3] ADC Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the Vin0 to Vin6 input channels.
[4] The conversion accuracy during Cell Balancing is decreased due to the activation of the Cell Balance circuitry. The ADC Unadjusted Error will increase from 0.1% to 0.4% within the -40°C to 85°C temperature range.
[5] Total Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the Vin0 to Vin6 input channels as well as the temperature coefficient of the 2.5V reference.
[6] The conversion accuracy during Cell Balancing is decreased due to the activation of the Cell Balance circuitry. The Total Unadjusted Error will increase from 0.2% to 0.8% within the -40°C to 85°C temperature range.
[7] ADC Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the VT input channels.
[8] Total Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the VT input channels as well as the temperature coefficient of the 2.5V reference.
[9] This spec outlines the regulator output current which is available for external use, that is, it does not include the regulator current already being used by the AD7280.
[10] CB output can be set to 0V or 5V with respect to negative terminal of cell being balanced.
[11] The CB1 to CB6 output ramp up times are defined from the rising edge of the CS command until the CB output exceeds 4V with respect to negative terminal of cell being balanced.
[12] The CB1 to CB6 output ramp down times are defined from the rising edge of the CS command until the CB output falls below 50mV with respect to negative terminal of cell being balanced.

TIMING SPECIFICATIONS

V_{DD} = 7.5 V to 30 V, V_{SS} = 0 V, D_{VCC} = A_{VCC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.25 V, T_A = -40°C to 105°C, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
	2.7 V ≤ V_{DRIVE} < 4.75 V	**4.75 V ≤ V_{DRIVE} ≤ 5.25 V**		
t_{CONV}	610	610	ns max	ADC Conversion time
t_{DELAY}	200	200	ns typ	Propogation delay between adjacent parts on the Daisy Chain
	250	250	ns max	
t_{WAIT}	5	5	µs min	Time required between the end of conversions and beginning to read back the conversion results
f_{SCLK}	10	10	kHz min	Frequency of serial read clock
	1	1	MHz max	
t_{QUIET}	200	200	ns min	Minimum quiet time required between the end of serial read and the start of the next conversion
t_1	400	400	ns min	Minimum $\overline{CONVST}$ low pulse
t_2	10	10	ns min	$\overline{CS}$ falling edge to SCLK rising edge
t_3	10	10	ns max	Delay from $\overline{CS}$ falling edge until SDO is three-state disabled
t_4	5	5	ns min	SDI setup time prior to SCLK falling edge
t_5	3	3	ns min	SDI hold time after SCLK falling edge
t_6[2]	20	14	ns max	Data access time after SCLK falling edge
t_7	7	7	ns min	SCLK to data valid hold time
t_8	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK high pulse width
t_9	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK low pulse width
t_{10}[3]	10	10	ns min	$\overline{CS}$ rising edge to SCLK rising edge
t_{11}	10	10	ns max	$\overline{CS}$ rising edge to SDO high impedance

[1] Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.
[2] The time required for the output to cross 0.4 V or 2.4 V.
[3] t_{10} applies when using a continuous SCLK.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +33 V
V_{SS} to AGND	−0.3 V to +0.3 V
Vin0 to Vin5 Voltage to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Vin6 Voltage to AGND	V_{DD} −0.3 V to V_{DD} + 1 V
CB1 Output to AGND	−0.3 V to DV_{CC} + 0.3 V
CB2 to CB6 Output to AGND	−0.3 V to V_{DD} + 0.3 V
VT1 to VT6 Voltage to AGND	−0.3 V to AV_{CC} + 0.3 V
AV_{CC} to AGND, DGND	−0.3 V to +7 V
DV_{CC} to AV_{CC}	−0.3 V to +0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to DV_{CC}+0.3 V
AGND to DGND	−0.3 V to +0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LQFP Package	
θ_{JA} Thermal Impedance	76.2°C/W
θ_{JC} Thermal Impedance	17°C/W
LFCSP Package	
θ_{JA} Thermal Impedance	54°C/W
θ_{JC} Thermal Impedance	15°C/W
Pb-free Temperature, Soldering Reflow	260(+0)°C
ESD	2kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

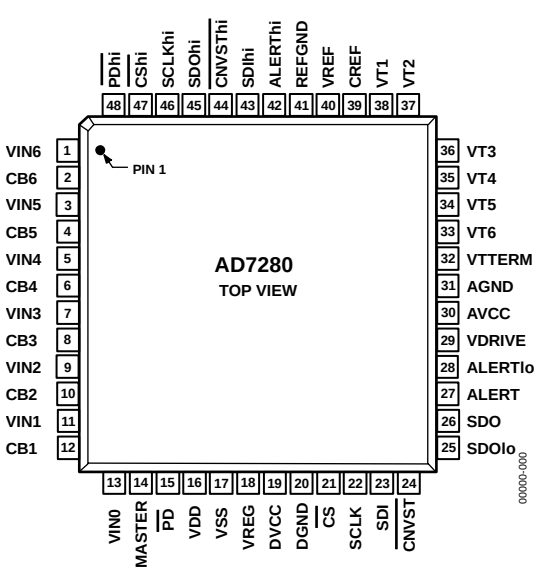


Figure 2.

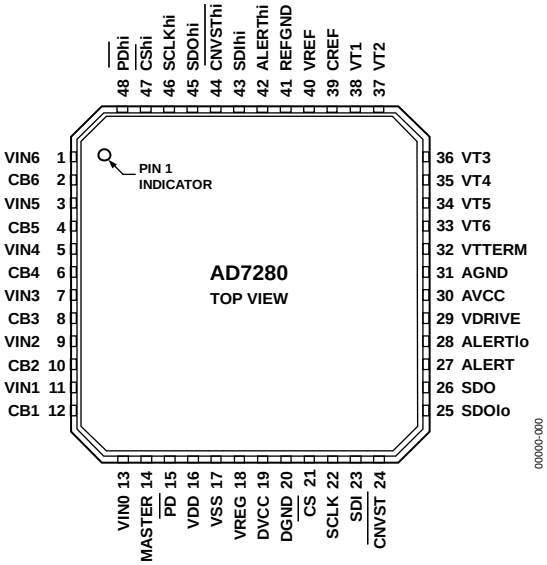


Figure 3.

Table 4.

Pin No.	*Mnemonic*	*Description*
1, 3, 5, 7, 9, 11, 13	Vin6 to Vin0	Analog Input 0 to Analog Input 6. Analog input 0 should be connected to the base of the series connected battery cells. Analog Input 1 should be connected to the top of cell 1, Analog Input 2 should be connected to the top of cell 2, etc. The Analog Inputs are multiplexed into the on-chip track-and-hold allowing the potential across each cell to be measured.
2, 4, 6, 8, 10, 12	CB6 to CB1	Cell Balance Outputs. These provide a voltage output which can be used to supply the gate drives of a cell balancing transistor network. Each CB(n) output provides a 5V voltage output referenced to the absolute voltage of Cell(n-1).
14	MASTER	Voltage Input. In an application with 2 or more AD7280s Daisy Chained the MASTER pin of the AD7280 connected directly to the DSP or uP should be connected to the V_{DD} supply pin through a 10kOhm resistor. The MASTER pin on the remaining AD7280s in the application should be tied to their respective V_{SS} supply pins through 10kOhm resistors.
15	$\overline{PD}$	Power down Input. This input is used to power down the AD7280. When acting as master the $\overline{PD}$ input is supplied from the DSP/uP. When acting as a slave on the Daisy Chain the $\overline{PD}$ input should be connected to the $\overline{PDhi}$ output of the AD7280 immediately below it in potential in the Daisy Chain.
16	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the high voltage analog input structure AD7280. The supply must be greater than a minimum voltage of 7.5 V. In an application monitoring the cell voltages of up to 6 series connected battery cells the supply voltage may be supplied directly from the cell with the highest potential. The maximum voltage which can be applied between V_{DD} and V_{SS} is 30V. Place 10 µF and 100 nF decoupling capacitors on the V_{DD} pin.
17	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the high voltage analog input structure of the AD7280. This input should be at the same potential as the AGND voltage.
18	V_{REG}	Analog Voltage output, 5V. The internally generated V_{REG} voltage, which provides the supply voltage for the ADC core, is available on this pin for use external to the AD7280. Place 10 µF and 100 nF decoupling capacitors on the V_{REG} pin.
19	DV_{CC}	Digital Supply Voltage, 4.75 V to 5.25 V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together, to ensure that the voltage difference between them never exceeds 0.3 V even on a transient basis. This supply should be decoupled to DGND. Place 100 nF decoupling capacitors on the DV_{CC} pin. The DV_{CC} supply pin should be connected to the V_{REG} output
20	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7280. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.

21	$\overline{CS}$	Chip select Input. When acting as a master, that is the Master pin of the AD7280 is connected to V_{DD}, the $\overline{CS}$ input is used to frame the input and output data on the SPI. The $\overline{CS}$ input also frames the input and output data on the Daisy Chain Interface when the MASTER input of the AD7280 is connected to V_{SS}.
22	SCLK	Serial Clock Input. When acting as master the SCLK input is supplied from the DSP/uP. When acting as a slave on the Daisy Chain this input should be connected to the SCLKhi output of the AD7280 immediately below it in potential in the Daisy Chain.
23	SDI	Serial Data Input. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7280 on the falling edge of SCLK. When acting as master this is the data input of the SPI interface. When acting as a slave on the Daisy Chain this input acepts data from the SDOhi output of the AD7280 immediately below it in potential in the Daisy Chain.
24	$\overline{CNVST}$	Convert Start Input. The conversion is initiated on the falling edge of CONVST. When acting as master the $\overline{CNVST}$ pulse is supplied from the DSP/uP. When acting as a slave on the Daisy Chain this input should be connected to the $\overline{CNVST}$hi output of the AD7280 immediately below it in potential in the Daisy Chain. This input can also be tied to V_{CC} and the conversion initiated through the serial interface.
25	SDOlo	Serial Data Output in Daisy Chain mode. When configured as a slave device this output should be connected to the SDIhi input of the AD7280 immediately below it in potential on the Daisy Chain. The data from each AD7280 in the Daisy Chain will be passed through the SDOlo outputs and SDIhi inputs of each AD7280 in the chain and supplied to the uP/DSP through the SDO output of the master AD7280. When configured as a master device it is recommended that this output, which is not required in slave mode, be connected to V_{SS} either directly or through a pull-down 1kOhm resistor.
26	SDO	Serial Data Output. The conversion output data or the register output data is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the SCLK input, and 32 SCLKs are required to access the data. The data is provided MSB first. In a Daisy Chain application the SDO output of the master AD7280 should be connected to the uP/DSP. The SDO outputs of the remaining AD7280s in the chain should be terminated to V_{SS} through a 1kΩ resistor. The data from each AD7280 in the Daisy Chain will be passed through the SDOlo outputs and SDIhi inputs of each AD7280 in the chain and supplied to the uP/DSP through the SDO output of the master AD7280. 32 SCLKs are required for each AD7280 in the chain to access the data.
27	ALERT	Digital Output. Flag to indicate over voltage, under voltage, over temperature or under temperature. The ALERT output of the master AD7280 should be connected to the uP/DSP. The ALERT outputs of the remaining AD7280s in the chain should be be terminated to V_{SS} through a 1kΩ resistor.
28	ALERTlo	Alert Output in Daisy Chain mode. The alert signal from each AD7280 in the Daisy Chain will be passed through the ALERTlo outputs and ALERThi inputs of each AD7280 in the chain and supplied to the uP/DSP through the ALERT output of the master AD7280. When configured as a slave device this output should be connected to the ALERThi input of the AD7280 immediately below it in potential on the Daisy Chain. When configured as a master device it is recommended that this output, which is not required in slave mode, be connected to V_{SS} either directly or through a pull-down 1kOhm resistor.
29	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage range on this pin is 2.7 V to 5.25 V and may be different to the voltage at AV_{CC} and DV_{CC}, but should never exceed either by more than 0.3 V.
30	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the ADC core. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together, to ensure that the voltage difference between them never exceeds 0.3 V even on a transient basis. This supply should be decoupled to AGND. Place 100 nF decoupling capacitors on the AV_{CC} pin. The AV_{CC} supply pin should be externally connected to the V_{REG} output.
31	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7280. This input should be at the same potential as the base of the series connected battery cells. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
32	VT_{TERM}	Thermistor termination resistor input.
33 to 38	VT6 to VT1	Voltage temperature input from potential divider with thermistor.
39	C_{REF}	A 100 nF decoupling capacitor to REFGND should be placed on this pin.
40	V_{REF}	Reference Output. The on-chip reference is availble on this pin for use external to the AD7280. The nominal internal reference voltage is 2.5V, which appears at the pin. A 10 μF decoupling capacitor to REFGND is recommended on this pin.
41	REFGND	Reference Ground. This is the ground reference point for the internal bandgap reference circuitry on the AD7280. The REFGND voltage should be at the same potential as the AGND voltage.
42	ALERThi	Alert Input in Daisy Chain mode. Flag to indicate over voltage, under voltage, over temperature or under temperature in Daisy Chain mode. The alert signal from each AD7280 in the Daisy Chain will be passed through the ALERTlo outputs and ALERThi inputs of each AD7280 in the chain and supplied to the uP/DSP through the ALERT output of the master AD7280. This input should be connected to the ALERTlo output of the AD7280 immediately above it in potential on the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD} through a 1kOhm resistor.

43	SDIhi	Serial Data Input in Daisy Chain mode. The data from each AD7280 in the Daisy Chain will be passed through the SDOlo outputs and SDIhi inputs of each AD7280 in the chain and supplied to the uP/DSP through the SDO output of the master AD7280. This input should be connected to the SDOlo output of the AD7280 immediately above it in potential on the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD} through a 1kOhm resistor.
44	$\overline{\text{CNVSThi}}$	Conversion Start Output in Daisy Chain mode. The convert start signal from the uP/DSP supplied to the $\overline{\text{CNVST}}$ input of the Master AD7280 is passed through each AD7280 by means of the $\overline{\text{CNVST}}$ input and the $\overline{\text{CNVSThi}}$ output. This output should be connected to the $\overline{\text{CNVST}}$ pin of the AD7280 immediately above it in potential on the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD}.
45	SDOhi	Serial Data Output in Daisy Chain mode. The Serial Data input from the uP/DSP supplied to the SDI input of the Master AD7280 is passed through each AD7280 by means of the SDI input and the SDOhi output. This output should be connected to the SDI input of the AD7280 immediately above it in potential on the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD}.
46	SCLKhi	Serial Clock Output in Daisy Chain mode. The clock signal from the uP/DSP supplied to the SCLK input of the Master AD7280 is passed through each AD7280 by means of the SCLK input and the SCLKhi output. This output should be connected to the SCLK input of the AD7280 immediately above it in potential in the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD}.
47	$\overline{\text{CShi}}$	Chip select Output in Daisy Chain mode. The chip select signal from the uP/DSP supplied to the $\overline{\text{CS}}$ input of the Master AD7280 is passed through each AD7280 by means of the $\overline{\text{CS}}$ input and the $\overline{\text{CShi}}$ output. This output should be connected to the $\overline{\text{CS}}$ input of the AD7280 immediately above it in potential on the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD}.
48	$\overline{\text{PDhi}}$	Power down Output in Daisy Chain mode. The power down signal from the uP/DSP supplied to the $\overline{\text{PD}}$ input of the Master AD7280 is passed through each AD7280 by means of the $\overline{\text{PD}}$ input and the $\overline{\text{PDhi}}$ output. This output should be connected to the $\overline{\text{PD}}$ pin of the AD7280 immediately above it in potential on the Daisy Chain. When this pin is unused,it is recommended that it is connected to V_{DD}.

TERMINOLOGY

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Code Error
This applies to straight binary output coding. It is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal, that is, AGND +1 LSB for VT1 to VT6 and 1V + AGND +1 LSB for Vin0 to Vin6.

Gain Error
This applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is $2 \times V_{REF} - 1$ LSB) after adjusting for the offset error.

ADC Unadjusted Error
ADC Unadjusted Error includes integral nonlinearity errors, offset and gain errors of the ADC and measurement channel.

Total Unadjusted Error (TUE)
This is the maximum deviation of the output code from the ideal. Total Unadjusted Error includes integral nonlinearity errors, offset and gain errors and reference drift.

Offset Error Match
This is the difference in zero code error across all 6 channels.

Gain Error Match
The difference in gain error across all 6 channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of a conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±½ LSB.

Common Mode Rejection Ration (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV sine wave applied to the common-mode voltage of the Vin(n) and Vin(n-1) frequency, f_S, as

$$CMRR\ (\text{dB}) = 10 \log (Pf/Pf_S)$$

where Pf is the power at frequency f in the ADC output, and Pf_S is the power at frequency f_S in the ADC output.

Power Supply Rejection Ration (PSRR)
Variations in power supply affect the full-scale transition but not the converter's linearity. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C using the following equation:

$$TCV_{REF}\,(ppm/°C) = \frac{V_{REF}\,(Max) - V_{REF}\,(Min)}{V_{REF}\,(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = Maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(Min)$ = Minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(25°C)$ = V_{REF} at +25°C
T_{MAX} = +85°C
T_{MIN} = −40°C

Output Voltage Hysteresis

Output voltage hysteresis, or thermal hysteresis, is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

T_HYS+ = +25°C to T_{MAX} to +25°C
$T\_HYS–$ = +25°C to T_{MIN} to +25°C

It is expressed in ppm using the following equation:

$$V_{HYS}\,(ppm) = \left| \frac{V_{REF}\,(25°C) - V_{REF}\,(T\_HYS)}{V_{REF}\,(25°C)} \right| \times 10^6$$

where:
$V_{REF}(25°C)$ = V_{REF} at 25°C
$V_{REF}(T\_HYS)$ = Maximum change of V_{REF} at T_HYS+ or T_HYS–.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7280 is a Lithium Ion battery monitoring chip with the ability to monitor the voltage and temperature of 6 series connected battery cells. The AD7280 also provides an interface which can be used to control transistors for cell balancing.

The V_{DD} and V_{SS} supplies required by the AD7280 can be taken from the upper and lower voltages of the series connected battery cells. An internal V_{REG} rail is generated from the supply voltage which provides power for the ADC and the internal interface circuitry. This V_{REG} voltage is available on an output pin for use external to the AD7280.

The AD7280 consists of a high voltage input multiplexer, a low voltage input multiplexer and a 12 bit ADC. The high voltage multiplexer allows up to 6 series connected Lithium Ion battery cells to be measured. The low voltage multiplexer allows the temperature of each cell to be measured. A single $\overline{\text{CNVST}}$ signal is required to initiate conversions on all 12 channels, that is 6 voltage and 6 temperature channels. Alternatively the conversion can be initiated through the rising edge of $\overline{\text{CS}}$ on the SPI interface. Each conversion result is stored in a results register (See Register section). On power-up, the $\overline{\text{CNVST}}$ signal is the default option, this can be changed by writing to the CONTROL register. The default sequence of conversions completed following the $\overline{\text{CNVST}}$ signal, or software convert start, is all 6 voltage channels followed by all 6 temperature channels. Two further conversion sequences may be selected by the user, 6 voltage channels followed by 3 temperature channels or just 6 voltage channels. The conversion sequence may be selected by writing to the CONTROL register.

Each voltage and temperature measurement requires a minimum of 1us to acquire and complete a conversion. Depending on the external components connected to the analog inputs of the AD7280 additional acquisition time may be required. A higher acquisition time may be selected through the CONTROL register. For increased accuracy in a noisy environment the user may also select the averaging option through the CONTROL register. This option allows the user to complete 2, 4 or 8 averages on each cell voltage and cell temperature measurement. The averaged conversion results are stored in the results registers. On power-up the default combined acquisition and conversion time will be 1us, with the averaging register set to zero, that is, a single conversion per channel.

The results of the voltage and temperature conversions are read back via the 4 wire Serial Peripheral Interface. The SPI interface is also used to write to and read data from the internal registers.

The AD7280 features an ALERT function which is triggered if the voltage conversion results or the temperature conversion results exceed the maximum and minimum voltage thresholds selected by the user. The threshold levels are selected by writing to the internal registers.

The AD7280 provides 6 analog output voltages which can be used to control external transistors as part of a cell balancing circuit. Each Cell Balance output provides a 0V or 5V voltage, with respect to the potential on base of each individual cell, which can be applied to the gate of the external cell balancing transistors.

The AD7280 features a daisy chain interface. Individual AD7280s can monitor the cell voltages and temperatures of 6 cells, a chain of AD7280s can be used to monitor the cell voltages and temperatures of a larger number of cells. The conversion data from each AD7280 in the chain passes to the system controller via a single standard serial interface. Control data can similarly be passed via the standard serial interface up the chain to each individual AD7280s

The AD7280 includes an on-chip 2.5V reference. The reference voltage is available for use external to the AD7280.

CONVERTER OPERATION

The AD7280 consists of a high voltage input multiplexer, a low voltage input multiplexer and a 12 bit ADC.

The high voltage multiplexer selects which pair of analog inputs, Vin0 to Vin6, are to be converted. The voltage of each individual cell is measured by converting the difference between adjacent analog inputs, that is, Vin1 – Vin0, Vin2 – Vin1, etc. This is illustrated in Figure 4 and Figure 5. The conversion results for each cell may be accessed after the programmed conversion sequence is complete.

The second multiplexer selects which voltage temperature input, VT1 to VT6, is to be converted. The conversion results for each cell may be accessed after the programmed conversion sequence is complete.

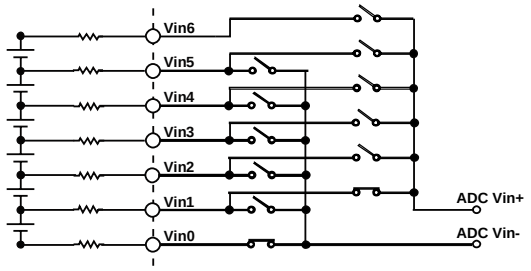


Figure 4. MUX Configuration During Vin1-Vin0 Sampling

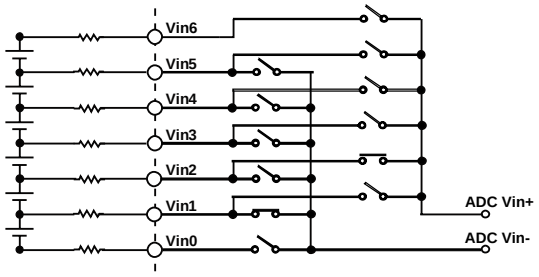


Figure 5. MUX Configuration During Vin2-Vin1 Sampling

The ADC is a 12-bit successive approximation analog-to-digital converter. The converter is composed of a comparator, SAR, some control logic and 2 capacitive DACs. Figure 6 shows a simplified schematic of the converter. During the acquisition phase switches SW1, SW2 and SW3 are closed. The sampling capacitor array acquires the signal on the input during this phase.

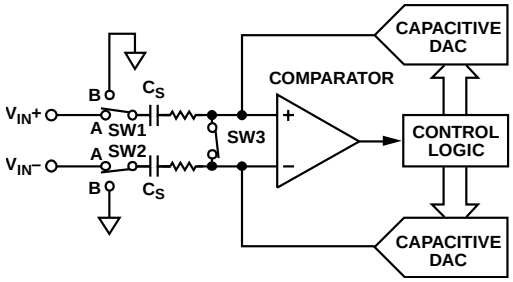


Figure 6. ADC Configuration During Acquisition Phase

When the ADC starts a conversion (Figure 7), SW3 opens and SW1 and SW2 move to position B, causing the comparator to become unbalanced. The control logic and capacitive DACs are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. This output code is then stored in the appropriate register for the input that has been converted.

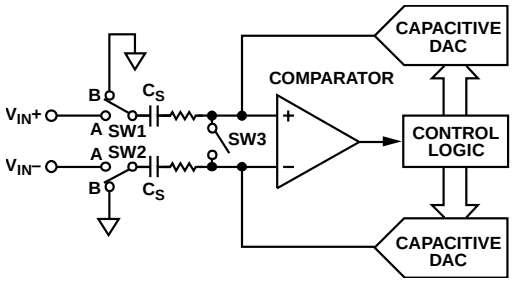


Figure 7. ADC Configuration During Conversion Phase

ANALOG INPUT STRUCTURE

Figure 8 shows the equivalent circuit of the analog input structure of the AD7280. The two diodes provide ESD protection. The resistors are lumped components made up of the on-resistance of the input multiplexer and the track-and-hold switch. The value of these resistors is typically about 300Ω. Capacitor C1 can primarily be attributed to pin capacitance while Capacitor C2 is the sampling capacitor of the ADC. The total lumped capacitance of C1 and C2 is approximately 13 pF.

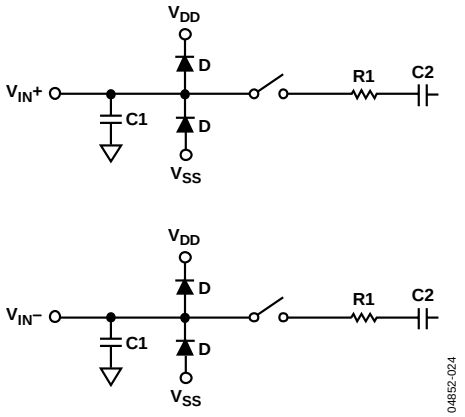


Figure 8. Equivalent Analog Input Circuit

TRANSFER FUNCTION

The output coding of the AD7280 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on whether the voltage or temperature inputs are being measured. The analog input range of the voltage inputs is 1V to 5V, the analog input range of the temperature inputs is 0V to 5V. The ideal transfer characteristic is shown in Figure 9.

Table 5. LSB Sizes for Each Analog Input Range

Selected inputs	Input Range	Full-Scale Range	LSB Size
Voltage	1 V to 5 V	4 V/4096	976 μV
Temperature	0 V to 5 V	5 V/4096	1.22 mV

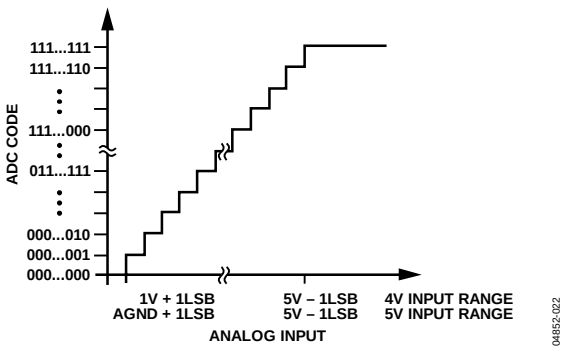


Figure 9. Transfer Characteristic

TYPICAL CONNECTION DIAGRAMS

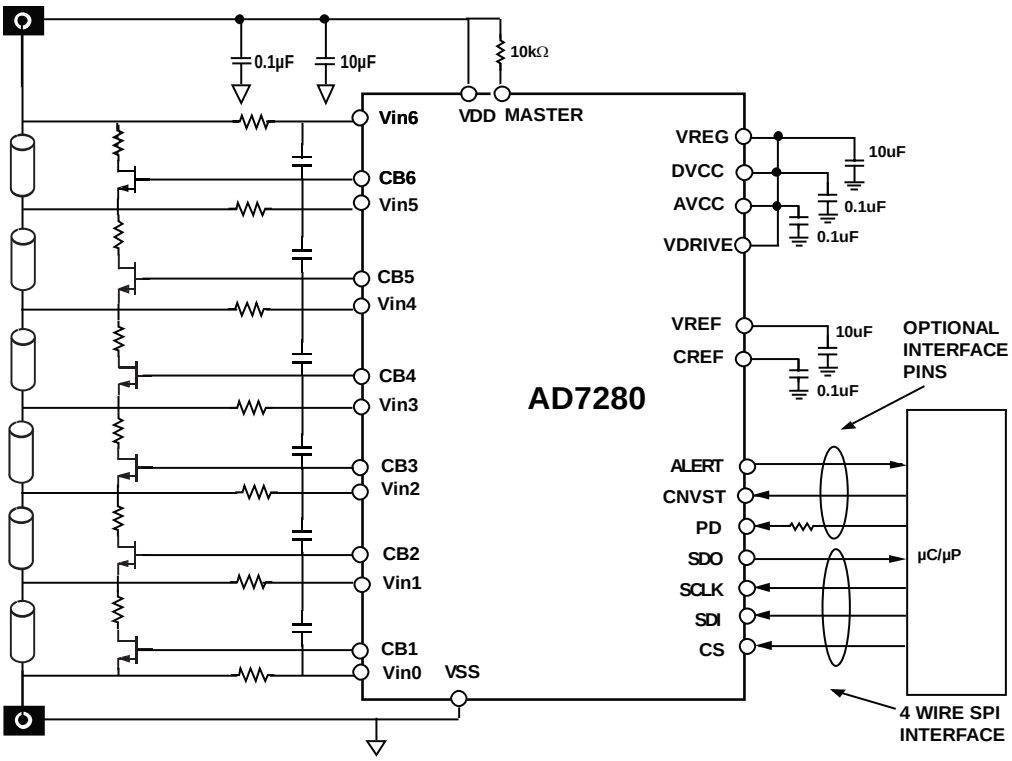


Figure 10. AD7280 Configuration Diagram for 6 Battery Cells

The AD7280 can be used to monitor 6 battery cells connected in series. A typical configuration for a 6 cell battery monitoring application is shown in Figure 10. Lithium Ion Battery applications require a significant number of individual cells to provide the required output voltage. Individual AD7280s can monitor the cell voltages and temperatures of 6 series connected cells. The Daisy Chain Interface of the AD7280 allows each individual AD7280 to communicate with another AD7280 immediately above or below it. The daisy chain interface allows the AD7280s to be electrically connected to the battery management chip, as shown in Figure 11 without the need for individual isolation between each AD7280.

Daisy Chain Connection Diagram

As shown in Figure 11 external diodes have been included on the V_{DD} supply to each AD7280 and on each Daisy Chain signal between adjacent AD7280s. These diodes, in combination with the 10kΩ series resistors on the analog inputs, are recommended to prevent damage to the AD7280 in the event of an open circuit in the battery stack.

It is also recommended that a zener diode be placed across the supplies of each AD7280 as shown in Figure 11. This will prevent an over voltage across the supplies of each AD7280 during the initial connection of the daisychain of AD7280s to the battery stack. A voltage rating of 33V is suggested for this zener diode but lower values may also be used to suit the application.

When using a chain of AD7280s it is also recommended that a 100kOhm series resistor is placed on the PD input. This is recommended to limit current into the PD pin in the event that the uP/DSP or isolators are connected before the supplies of the master AD7280.

Please refer to the Daisy Chain Interface Section for a more detailed description of the Daisy Chain Interface.

In an application which includes a safety mechanism, designed to open circuit the Battery Stack, additional isolation will be required between the AD7280 above the break point and the battery management chip.

EMC Considerations

In addition to the standard decoupling capacitors, C2n and C3n, as shown in Figure 11, it is also recommended that an option for additional capacitors, C1n and C4n, be included in the circuit to increase immunity to Electromagnetic Interference. These capacitors, placed on either side of the V_{DD} protection diode, would be used to decouple the V_{DD} supply of each AD7280 with respect to system ground, that is, the ground of the master AD7280 in the daisychain.

It is recommended that ferrite beads be included on the battery

connections to the V_{DD} and V_{SS} supplies. It is also recommended that pull-down resistors should be used on the ALERT and SDO outputs on each of the slave parts in the AD7280 daisychain.

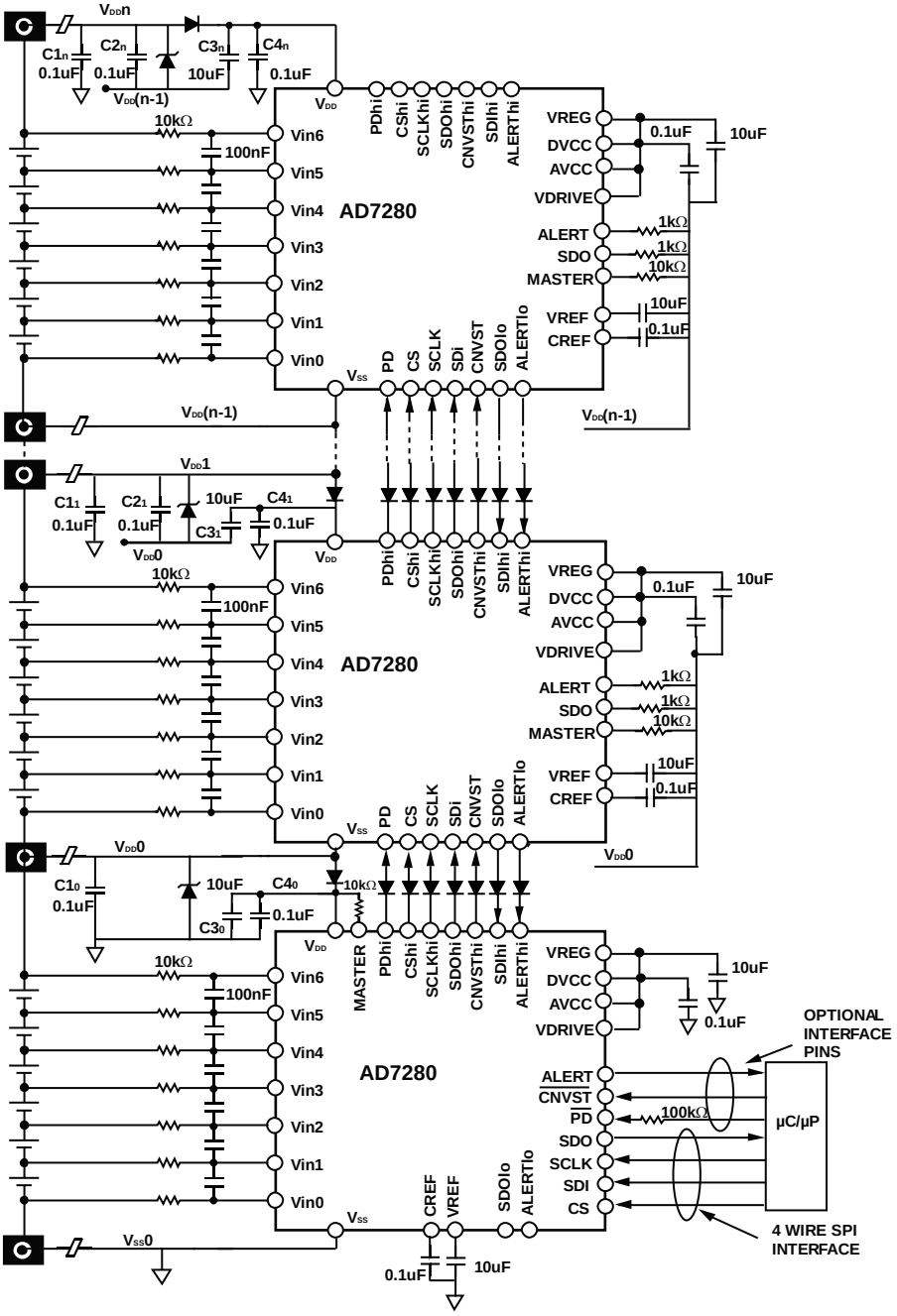


Figure 11. AD7280 Daisy Chain Configuration

V_{DRIVE}

The AD7280 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, in the recommended configuration the AD7280 is operated with a V_{CC} of 5 V, however the V_{DRIVE} pin could be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors.

REFERENCE

The internal reference is temperature compensated to 2.5 V ± 5 mV. The reference is trimmed to provide a typical drift of 3 ppm/°C. The internal reference circuitry consists of a 1.2 V band gap reference and a reference buffer. The AD7280 internal

reference is available at the V_{REF} pin. The V_{REF} pin should be decoupled to REFGND using a 10 µF, or greater, ceramic capacitor. The C_{REF} pin should be decoupled to REFGND using a 0.1 µF, or greater, ceramic capacitor. The internal reference is capable of driving an external load of up to 10kOhms.

CONVERTING CELL VOLTAGES AND TEMPERATURES

A conversion may be initiated on the AD7280 using either the $\overline{CNVST}$ input or the serial interface. A single $\overline{CNVST}$ signal is required to initiate conversions on all 12 channels, that is 6 voltage and 6 temperature channels. Alternatively the conversion can be initiated through the rising edge of $\overline{CS}$ on the SPI interface.

When using the $\overline{CNVST}$ input the falling edge of $\overline{CNVST}$ places the track and hold on the voltage inputs Vin6 and Vin5, that is across Cell 6, into hold mode and initiates the conversion. At the end of the first conversion the AD7280 generates an internal End of Conversion signal. This internal EOC will select the next cell voltage inputs for measurement though the multiplexer, that is, Vin5 and Vin4. The track-and-hold circuit will acquire the new input voltage and a second internal convert start signal is generated which places the track-and-hold into hold mode and initiates the conversion. This process is repeated until all the selected voltage and temperature cell inputs have been converted. Please refer to Figure 12 and Figure 13. Note, once all selected conversions have been completed voltage inputs Vin6 and Vin5 are again selected through the multiplexer and the voltage across Cell 6 is acquired in preparation for the next conversion request.

By setting bits D15 and D14 in the control register the voltage and temperature cells to be converted are selected. There are four options available.

Table 6. Voltage and Temperature Cell Selection

D15 to D14	Voltage inputs	Temperature Inputs
00	1 to 6	1 to 6
01	1 to 6	1, 3 & 5
10	1 to 6	None
11	ADC Self Test	None

Each voltage and temperature conversion requires a minimum of 1us to acquire and convert the cell voltage or temperature voltage input. For example, when D15 and D14 are set to zero the falling edge of $\overline{CNVST}$ will trigger a series of 12 conversions. This will require a minimum of 12µs to convert all selected measurements. If no temperature conversions are required then Bits D15 and D14 would be set to 10. In this case the conversion request will trigger a series of 6 conversions, requiring a minimum of 6µs.

Following the completion of all requested conversions the results may be read back from either a single device or from all devices in a daisychain by use of the SPI and Daisychain interfaces. More information on this may be found in the Serial Interface and Daisy Chain Interface sections. As shown in Figure 13, a wait time, t_{WAIT}, is required between the completion of conversions and the start of readback. This time is required to synchronise between the high speed conversion clock and the lower speed clock used for all other AD7280 operations. The maximum value of t_{WAIT} is 5µs.

Track-and-Hold

The track-and-hold on the analog input of the AD7280 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy.

Following a completed conversion the AD7280 enters its tracking mode. The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. This in turn will depend on the input impedance and any external components placed on the analog inputs. The default acquisition time of the AD7280 on initial power up is 400 ns. This can be increased in steps of 400ns to 1.6 us to provide flexibility in selecting external components on the analog inputs. The acquisition time is selected by writing to bits D6 and D5 in the CONTROL register.

It should also be noted once the acquisition time is reconfigured 90µs should be allowed before performing any conversions. This time should be allowed between writing to the CONTROL register to change the acquisition time and initiating the first conversion. In the case of conversions which are being initiated by the rising edge of the $\overline{CS}$ pin, this will require 2 separate write commands to the CONTROL register. The first to configure the AD7280 for the required acquisition time, the second, following a delay of 90µs, to initiate the conversion on the rising edge of $\overline{CS}$.

Table 7.Analog Input Acquisition Time.

D6 to D5	Acquisition Time
00	400 ns
01	800 ns
10	1.2 µs
11	1.6 µs

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R)\ C)$$

where:
C is the sampling capacitance, the value of the sampling capacitor, 13pF
R is the resistance seen by the track-and-hold amplifier looking at the input, 300Ω.
R_{SOURCE} should include any extra source impedance on the analog input.

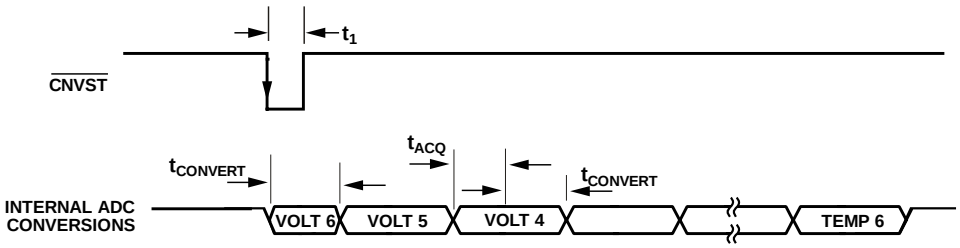


Figure 12. ADC conversions on the AD7280

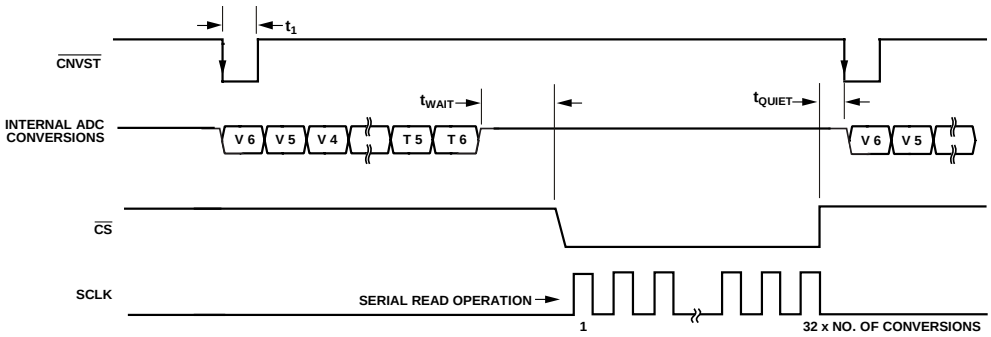


Figure 13. ADC conversions & Readback on the AD7280

Converting Cell Voltages and Temperatures with a chain of AD7280s

The AD7280 provides a daisy chain interface which allows up to 20 parts to be stacked without the need for individual isolation. One feature of this daisychain interface is the ability to initiate conversions on all parts in the daisychain stack with a single conversion start command. The conversion can be initiated through a single $\overline{\text{CNVST}}$ pulse or through the rising edge of $\overline{\text{CS}}$ on the SPI interface. The convert start command is transferred up the daisychain, from the master device, to each AD7280 in turn. The delay time between each AD7280 is t_{DELAY}, as outlined in Figure 14. The maximum delay between the start of conversions on the master AD7280 and the last AD7280 device in the chain can be determined by multiplying t_{DELAY} by the number ofAD7280s in the daisychain. The total conversion time for all cell voltage and temperature conversions can be calculated using the following equation:

$$Total\ Conversion\ time = ((t_{ACQ} + t_{CONV}) \times (\#\text{conversions per part}) - t_{ACQ} + (\#\text{parts} \times t_{DELAY})$$

Where

t_{ACQ} is the analog input acquisition time of the AD7280 as outlined in Table 7

t_{CONV} is the conversion time of the AD7280 as outlined in Table 2

#conversions per part is 6, 9 or 12 as outlined in Table 6.

#parts is the number of AD7280s in the daisychain

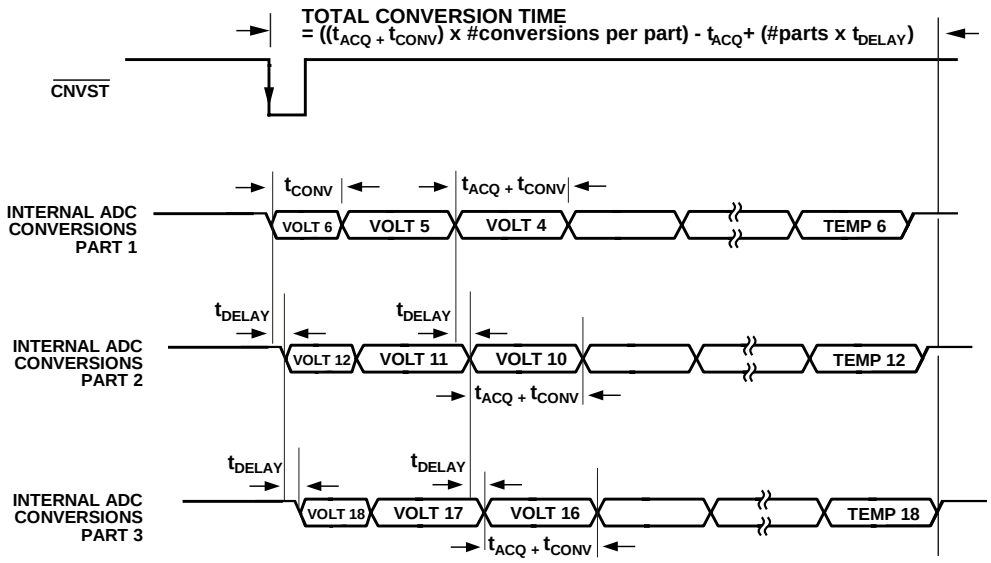


Figure 14. ADC conversions & Readback on a chain of 3 AD7280s

Suggested External Component Configurations on Analog Inputs

As outlined in the Track-and –Hold section the acquisition time of the AD7280 is selected by the status of bits D6 and D5 in the CONTROL register. This provides flexibility in selecting external components on the analog inputs. Included below are two suggested configurations for placing external components on the analog inputs to the AD7280.

Combined LP filter and Current Limiting Resistors

Please refer to Figure 15.

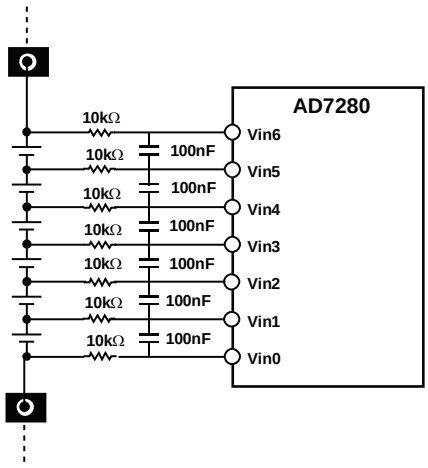


Figure 15. External Series Resistance & Shunt Capacitance

The 10kΩ resistor in series with the inputs provides protection to the analog inputs in the event of an over-voltage or under-voltage on those inputs. The 100nF capacitor across the pseudo differential inputs acts as a low pass filter in conjunction with the 10kΩ resistor. The cut off frequency of the low pass filter is 318Hz. Using these external components the default acquisition time of 400 ns may be used, which will allow a combined acquisition and conversion time of 1µs.

Current Limiting Resistors

Please refer to Figure 16.

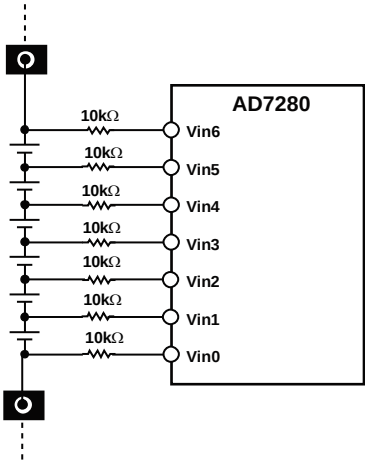


Figure 16. External Series Resistance

The 10kΩ resistor in series with the inputs provides protection to the analog inputs in the event of an over-voltage or under-voltage on those inputs. Using these external components an acquisition time of 1.6 µs should be used, which will allow a combined acquisition and conversion time of 2.2µs.

SELF TEST CONVERSION

A self-test conversion may be initiated on the AD7280 which allows the operation of the ADC to be verified. The self-test conversion is completed on the internal 1.2V bandgap reference voltage. The self-test conversion may be initiated on either a single AD7280 or on all AD7280s in the battery stack

simultaneously. The conversion results may be read back though the read protocols defined in the Register map section.

The self-test conversion may also be used to verify the operation of the ALERT outputs as described in the ALERT Output section.

CONVERSION AVERAGING

The AD7280 includes an option where the acquisition and conversion of each cell input may be repeated with an averaged conversion result being stored in the individual register. The averaged conversion result may then be read back through the SPI interface in the same manner as a standard conversion result. The AD7280 may be programmed, through bits D10 and D9 of the CONTROL register, to complete 1, 2, 4 or 8 conversions. The default on power up is a single conversion.

Selection of the 2, 4, or 8 average options, through the CONTROL register, will cause the control sequence of both the high voltage and low voltages input multiplexers to be reconfigured to allow the additional acquisitions and conversions to be completed. In each case the requested number of conversions will be completed on each channel before beginning to acquire and convert on the next channel in sequence. For example, if an average of 2 conversions is requested the new sequence will be voltage channel 6, voltage channel 6, voltage channel 5, voltage channel 5, voltage channel 4 etc.

It should also be noted once the high voltage multiplexors are reconfigured, 90µs should be allowed before performing any conversions. This time should be allowed between writing to the CONTROL register to select averaging and initiating the first conversion. In the case of conversions which are being initiated by the rising edge of the $\overline{CS}$ pin, this will require 2 separate write commands to the CONTROL register. The first to configure the AD7280 for the required the required averaging, the second, following a delay of 90µs, to initiate the conversion on the rising edge of $\overline{CS}$.

CONVERSION OF LESS THAN 6 VOLTAGE CELLS

The AD7280 provides 6 input channels for Battery Cell voltage measurement. The AD7280 may also be used in applications which require less than 6 voltage measurements. In these applications care should be taken to ensure that the sum of the individual cell voltages will still exceed the minimum V_{DD} supply voltage. For this reason it is recommended that the minimum number of battery cells connected to each AD7280 is 4. Care should also be taken to ensure that the voltage on the Vin6 inputs is always greater than or equal to the voltage on the V_{DD} supply pin. This design requirement is in place to allow the use of a diode on the V_{DD} supply pin of the AD7280 which provides protection in the event of an open circuit in the battery stack. Even if a protection diode is not being used in the application the Vin6 input voltage must be greater than or equal to the V_{DD} supply voltage. An example of the battery connections to the AD7280 in a 4 cell battery monitoring application is shown in Figure 17.

Regardless of how many cell measurements are required in the user application the AD7280 will acquire and convert the voltages on all 6 voltage input channels. The conversion data on all 6 channels will be supplied to the DSP/uP using the SPI /Daisy Chain interfaces. The user should then ignore the conversion data which is not required in their application. If using the Alert function the user should program the Alert register to ensure that the shorted out channels do not incorrectly trigger an Alert output. Please refer to ALERT Output section.

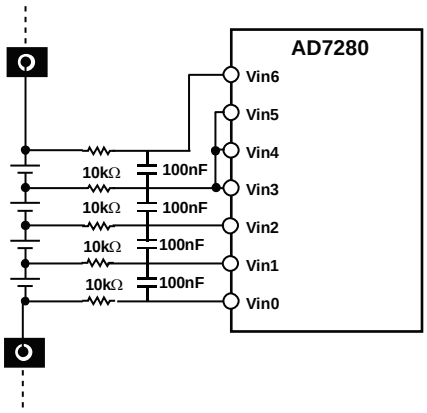


Figure 17. Typical connections for a 4 cell application

CELL TEMPERATURE INPUTS

The AD7280 provides 6 single ended analog inputs, VT1 to VT6, to the ADC which may be used to convert the voltage output of a thermistor temperature measurement circuit. In the event that no temperature measurements are required, or that individual cell temperature measurements are not required the VT inputs may be used to convert any other 0 V to 5 V input signal.

The AD7280 may be programmed to complete conversions on all 6 temperature channels, on 3 temperature channels (VT1, VT3 & VT5) or on none of the temperature input channels. The number of conversions is programmed through bits D15 and D14 of the CONTROL register. The number of conversions results supplied by the AD7280 for read back by the DSP/uP is programmed through bits D13 and D12 of the CONTROL register. In an application where the ALERT function is being used but only one or two temperature inputs are required the AD7280 should first be programmed to complete and readback only 3 temperature conversions, by setting bits D15 and D13 of the CONTROL register to 0, and bits D14 and D12 to 1. VT Channels VT5 and VT3 may be removed from the Alert detection by writing to bits D1 and D0 of the ALERT register. Please refer to ALERT Output section.

Thermistor Termination Input

In the event that thermistors circuits are being used to measure each individual cell temperature the Thermistors Termination pin, VT_{TERM}, may be used to the terminate the thermistor inputs for each cell temperature measurement. This reduces the termination resistor requirement from 6 resistors to 1. Bit D3 in the CONTROL register should be set to 1 when using the VT_{TERM} input.

It should be noted that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280 is set to its highest value, that is, 1.6µs. The acquisition time is configured by setting bits D6 and D5 of the CONTROL register as outlined in Table 7.

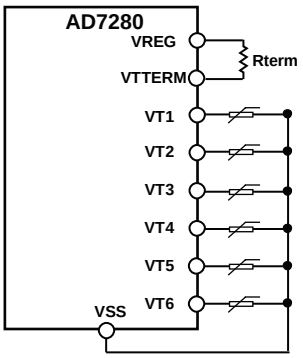


Figure 18. Typical Circuit using the Thermistor Termination Resistor

In the example shown the termination resistor is placed between the source voltage and the thermistor in the thermistor circuit. The VT_{TERM} input may be used to terminate the thermistor inputs to either high or low voltage of the Thermistor circuit.

POWER REQUIREMENTS

The current consumed by the AD7280 in normal operation, that is when not in powerdown mode, is dependent on the mode in which the part is being operated. In a typical Lithium Ion battery monitoring application there are 3 distinct modes of operation. These can be described as follows:

- Voltage and Temperature Conversion
- AD7280 Configuration & Data Readback
- Cell Balancing

The AD7280 consumes its highest level of current while converting voltage and/or temperature inputs to digital outputs. Depending on the configuration of the AD7280 the conversion time can be as little as 6us. As outlined in Table 1 the typical current required by the AD7280 during conversion is 7mA.

When configuring the chain of AD7280s or when reading back the voltage and/or temperature conversion results from a chain of AD7280s the current required for each AD7280 is typically 4mA, as outlined in Table 1. The time required to read back the voltage conversions results from 96 Lithium Ion cells will depend on the speed of the interface clock used, that is SCLK, but it can be as low as 3.2ms.

The typical current consumed by the AD7280 when the cell balancing outputs are switched on is 4.5mA. The duration of the Cell Balance outputs on time is defined by the user.

When the AD7280 is not being used in any of the above modes of operation it is recommended that the AD7280 be powered down, as outlined below. This will significantly reduce the current draw by each AD7280 on the chain which will avoid unnecessary draining of the Lithium Ion cells.

POWER DOWN

The AD7280 provides a number of powerdown options. These may be described as follows:

- Full Powerdown (Hardware)
- Software Powerdown

The AD7280 may be placed into full powerdown mode, which requires only 4uA max current, by taking the $\overline{PD}$ pin low. The falling edge of the $\overline{PD}$ pin will power down all analog and digital circuitry. The AD7280 includes a digital filter on the $\overline{PD}$ pin which prevents the power down being initiated by noise or glitches on the hardware $\overline{PD}$ pin. A hardware power down will not be initiated until the $\overline{PD}$ pin has been held low for approximately 150µs. Similarly the AD7280 will not be taken out of powerdown mode until the $\overline{PD}$ pin has been held high for approximately 5µs.

The AD7280 may be placed into Software Power down mode, which requires only 1.8mA of current by setting bit D8 in the CONTROL register through the serial interface. When the AD7280 is powered down through the serial interface the regulator, the reference and the daisy chain circuitry stay powered up but the remaining analog and digital circuitry is powered down. This is necessary to ensure that the signal to power on the part, or series of parts, is correctly received.

The AD7280 offers a PD TIMER register which allows the user to program a set time after which the AD7280 will go into power down. This will act as a time delay between the falling edge of the $\overline{PD}$ input, or the setting of bit D8 in the CONTROL register, and the AD7280 powering down. The PD Timer can be set to a value between 0 and 39 minutes, with a resolution of 75 seconds. The user should first write to the PD TIMER register, to define the desired delay. Any subsequent falling edge on the $\overline{PD}$ input or setting of bit D8 the CONTROL register, will start the PD timer and after the programmed time will place the AD7280 into powerdown. The default value of the PD TIMER

register on power up is 0h.

POWER UP TIME

As outlined in the Power Down section a full power down of the AD7280, that is, an active low on the $\overline{PD}$ input, will power down all analog and digital circuitry. The recommended power up time for the internal reference, when decoupled with a 10µF capacitor, is 10ms. It is recommended that no conversions be completed until the 10ms power up time has elapsed as it may result in inaccurate data.

CELL BALANCING OUTPUTS

The AD7280 provides 6 CB outputs which can be used to drive the gate of external transistors as part of a cell balancing circuit. Each CB output may be set to provide either a 0V or 5V output with respect to the absolute amplitude of the negative terminal of the battery cell which is being balanced. For example, the CB6 output will provide a 0V or 5V output with respect to the voltage on the Vin5 analog input. The CB outputs are set by writing to the CELL BALANCE register. The default value of the CELL BALANCE register on power up is 0h.

In an application which daisychains a number of AD7280s together it is recommended that series resistors be placed between the CB outputs of the AD7280 and the gates of the external Cell Balancing transistors. These are recommended to protect the AD7280s in the event that the external cell balancing transistors are damaged during the initial connection of the monitoring circuitry to the battery stack.

An example of how this could occur would be a connection sequence which first provides the system ground, that is the ground supply to the master AD7280 on the daisychain, followed by a connection from any of the battery cells at a potential high enough to exceed the V_{GS} of the cell balancing transistor, for example 40V. If these two connections are the only battery connections made in the system then this will result in 40V being applied to one of the Vin pins of the AD7280, which is also connected to the source input of one of the cell balancing transistors. However, because no power has been supplied to the V_{DD} pin of the AD7280 all the CB outputs will be 0V. This will result in a reverse voltage of 40V across the V_{GS} of the external transistor which may damage the device.

In the event that the external transistor is damaged, the AD7280 may be protected by the use of 10kOhm series resistors on each of the CB output pins. Consideration should also be given to the protection of these external transistors during the initial connection of the monitoring circuitry to the battery stack.

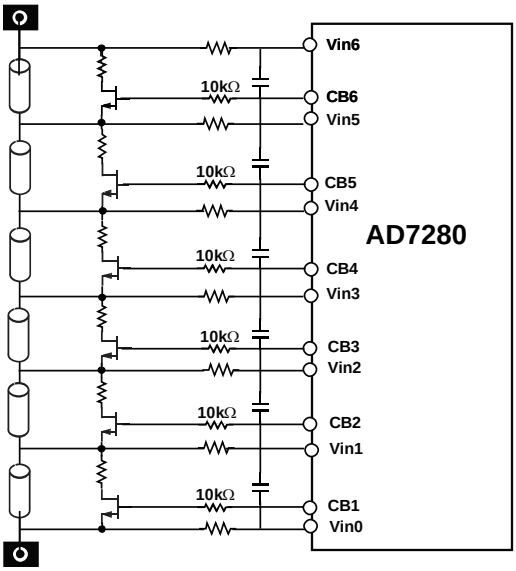


Figure 19. Cell Balancing Configuration

The AD7280 offers 6 Cell Balance timer registers which allow the on-time of each CB output to be programmed. These are referred to as the CB TIMER registers. The CB timers can be set to a value between 0 and 39 minutes. The resolution of the CB Timer is 75 seconds. At the end of the programmed CB Time the 6 CB outputs will return to their default state of 0V. The default value of the CB TIMER registers on power up is 0h.

As noted in the Power Down section a power down timer may be programmed to allow cell balancing to occur for a set time before powering down the AD7280. If no power down timer has been set, that is if the PD TIMER register is at its default value of 0h, then a falling edge on the PD pin, or the setting of bit D8 in the CONTROL register to 1, will switch off the CB outputs and power down the AD7280. If a power down time has been set the CB outputs will be powered down when the programmed power down timer has elapsed and the AD7280 is powered down.

ALERT OUTPUT

The Alert output on the AD7280 may be used to indicate if any of the following faults have occurred:

- Over-Voltage
- Under-Voltage
- Over-Temperature
- Under-Temperature

Following each completed conversion the cell voltage and temperature measurement results are compared to the fault thresholds. The fault thresholds can be set by writing to the OVER VOLTAGE. UNDER VOLTAGE, OVER TEMP and UNDER TEMP registers. An ALERT output is generated if the cell voltage or temperature results are outside the programmed fault thresholds.

The Alert output can be defined as a static or a dynamic output, this is set by writing to the ALERT register. The static Alert output is a high signal which is pulled low in the event of an over or under voltage or temperature. The dynamic Alert is a square wave which can be programmed to a frequency of 100Hz or 1kHz. The Alert output may be used as part of a daisy chain in which case the AD7280 at the top of the chain, that is furthest away from the DSP/µP should be programmed to generate the initial Alert output and each AD7280 in the chain will either pass that output through or pull the Alert signal low to indicate that there is a fault with that particular device. At the end of the daisy chain the master AD7280, that is the AD7280 which is connected to the DSP/µP will take the Alert signal from the chain and pass it, in standard digital voltage format to the DSP/µP. The functionality of the fault detection circuit, which generates the Alert output, may be programmed through bits D7 to D4 of the ALERT register.

As outlined previously (See Conversion of less thAn 6 Voltage cells) some applications may require less than 6 voltage measurements. As shown in Figure 17 it is recommended that the channels which are not being used on the AD7280 be shorted to the channel below them. To prevent the incorrect triggering of the Alert output in this application the AD7280 allows the user to select up to 2 voltage channels which may be taken out of the fault detection circuit. This may be programmed through bits D3 and D2 of the ALERT register.

Table 8.ALERT Register settings

D7 to D6	D5 to D4	D3 to D0	AD7280 Action
00	XX	XXXX	No Alert signal generated or passed [Default]
01	XX	XXXX	Generates static [High] Alert signal to be passed down the Daisy Chain
10	00	XXXX	Generates 100Hz Square wave Alert signal to be passed down the Daisy Chain
10	01	XXXX	Generates 1kHz Square wave Alert signal to be passed down the Daisy Chain
10	10	XXXX	Reserved
10	11	XXXX	Reserved
11	XX	XXXX	Passes Alert signal from AD7280 at higher potential in Daisy Chain
D7 to D4	**D3 to D2**	**D1 to D0**	**AD7280 Action**
XXXX	00	XX	Includes all 6 Voltage channels in Alert detection [Default]
XXXX	01	XX	Removes Vin5 from Alert detection
XXXX	10	XX	Removes Vin5 & Vin4 from Alert detection
XXXX	11	XX	Reserved
XXXX	XX	00	Includes all 6 Temperature channels in Alert detection [Default]
XXXX	XX	01	Removes VT5 from Alert detection
XXXX	XX	10	Removes VT5 & VT3 from Alert detection

The operation of the ALERT output can be verified by initiating a Self-Test conversion. The self-test conversion will convert a known voltage, 1.2V, which will trigger an ALERT output if the under voltage fault threshold is higher than 1.2V. To test the ALERT output the self-test should be initiated on the AD7280 furthest away from the DSP/µP. This allows the ALERT path through each AD7280 to be verified. The remaining AD7280s in the battery stack should be placed into software powerdown to ensure that only the part which is converting the self-test voltage may generate an ALERT output.

REGISTER MAP

Table 9.

Register Name	Register Address	Register Data	Read/Write Register
CELL VOLTAGE 1	0h	D11 to D0	Read Only
CELL VOLTAGE 2	1h	D11 to D0	Read Only
CELL VOLTAGE 3	2h	D11 to D0	Read Only
CELL VOLTAGE 4	3h	D11 to D0	Read Only
CELL VOLTAGE 5	4h	D11 to D0	Read Only
CELL VOLTAGE 6	5h	D11 to D0	Read Only
CELL TEMP 1	6h	D11 to D0	Read Only
CELL TEMP 2	7h	D11 to D0	Read Only
CELL TEMP 3	8h	D11 to D0	Read Only
CELL TEMP 4	9h	D11 to D0	Read Only
CELL TEMP 5	Ah	D11 to D0	Read Only
CELL TEMP 6	Bh	D11 to D0	Read Only
SELF TEST	Ch	D11 to D0	Read Only
CONTROL	Dh	D15 to D8	Read/Write
	Eh	D7 to D0	Read/Write
OVER VOLTAGE	Fh	D7 to D0	Read/Write
UNDER VOLTAGE	10h	D7 to D0	Read/Write
OVER TEMP	11h	D7 to D0	Read/Write
UNDER TEMP	12h	D7 to D0	Read/Write
ALERT	13h	D7 to D0	Read/Write
CELL BALANCE	14h	D7 to D0	Read/Write
CB TIMER 1	15h	D7 to D0	Read/Write
CB TIMER 2	16h	D7 to D0	Read/Write
CB TIMER 3	17h	D7 to D0	Read/Write
CB TIMER 4	18h	D7 to D0	Read/Write
CB TIMER 5	19h	D7 to D0	Read/Write
CB TIMER 6	1Ah	D7 to D0	Read/Write
PD TIMER	1Bh	D7 to D0	Read/Write
READ	1Ch	D7 to D0	Read/Write
CONTROL 3	1Dh	D7 to D0	Read/Write

CELL VOLTAGE REGISTERS

Table 10. 12-Bit Registers

0h to 5h	D11 to D0	Read/Write

The CELL VOLTAGE registers store the conversion result from each cell input. The conversion result is in 12-bit natural binary format.

CELL TEMPERATURE REGISTERS

Table 11. 12-Bit Register

6h to Bh	D11 to D0	Read/Write

The CELL TEMP registers store the conversion result from each temperature input. The conversion result is in 12-bit natural binary format.

SELF-TEST REGISTER

Table 12. 12-Bit Register

Ch	D11 to D0	Read/Write

The SELF-TEST register stores the conversion result of the ADC self-test. A self-test conversion is initiated by setting bits D15 and D14 of the CONTROL register to 11. The user should then pulse the CNVST input or complete a software convert start through the $\overline{CS}$ input. The conversion result is in 12-bit natural binary format.

CONTROL REGISTER

Table 13. 16-Bit Register

Dh	D15 to D8	Read/Write
Eh	D7 to D0	Read/Write

The CONTROL register is a 16-bit register that sets the AD7280 Control modes.

Table 14. 16-Bit Register

D15 to D14	Select Conversion Inputs
	00 = 6 Voltage & 6 Temp [default]
	01 = 6 Voltage & Temp 1,3 &5
	10 = 6 Voltage only
	11 = ADC Self Test
D13 to D12	Read Conversion Results
	00 = 6 Voltage & 6 Temp [default]
	01 = 6 Voltage & Temp 1,3 &5
	10 = 6 Voltage only
	11 = No Read operation
D11	Conversion Start Format
	0 = Falling edge of CNVST input [default]
	1 = Rising edge of CS
D10 to D9	Conversion Averaging
	00 = Single Conversion only [default]
	01 = Average by 2
	10 = Average by 4
	11 = Average by 8
D8	Powerdown format
	0 = Falling edge of $\overline{PD}$ input [default]
	1 = Software PD
D7	Software Reset
	0 = Bring out of Reset [default]
	1= Reset AD7280
D6 to D5	Set Acquisition Tme
	00 = Acquisition time 400ns [default]
	01 = Acquisition time 800ns
	10 = Acquisition time 1.2us
	11 = Acquisition time 1.6us
D4	Reserved; set to 1
D3	Thermistor Termination Resistor
	0 = Function not in use [default]
	1 = Termination resistor connected
D2	Lock Device Address
	0 = Does not lock to new Device Address. Contiues to operate with Device Address 0h. [default]
	1 = Part locks to new Devices Address it is presented with.

D1	Increment Device Address 0 = Does not increment the Device Address when transferring data up the Daisychain. 1 = Increments the Device Address when transferring data up the Daisychain [default]
D0	Daisychain Register Readback 0 = Function not in use 1 = Set Daisychain for Register Readback [default]

Select Conversion Inputs

Bits D15 and D14 of the CONTROL register determine which cell voltages and temperatures are converted following a $\overline{\text{CNVST}}$ pulse or the setting of the CNVST bit, D11, in the CONTROL register. The default value of D15 and D14 on power up are 00.

Read Conversion Results

Bits D13 and D12 of the CONTROL register determine which cell voltages and temperatures conversion results are supplied to the serial or Daisychain data outputs pins for readback. The default value of D15 and D14 on power up are 00.

Conversion Start Format

The AD7280 offers two methods of initiating a conversion, the hardware $\overline{\text{CNVST}}$ pin or the software $\overline{\text{CS}}$ input. Bit D11 of the CONTROL register determines whether a conversion is initiated on the falling edge of the $\overline{\text{CNVST}}$ input or on the rising edge of the CS input. The default format on power up is the $\overline{\text{CNVST}}$ pin. When using the rising edge of CS to initiate conversions it should be noted that bit D11 is reset to 0 following the initiation of conversions.

Conversion Averaging

Bits D10 and D9 of the CONTROL register determines the number of conversions completed on each input with the average result being stored in the Result registers. The default value of the Conversion Averaging bits is 00, that is, no averaging.

Powerdown Format

Bit D8 of the CONTROL register allows the AD7280 be placed into a software powerdown. Please refer to the Power Down section for more details. The default format on power up is powerdown through the $\overline{\text{PD}}$ pin.

Software Reset

Bit D7 of the CONTROL register allows the user to initiate a software Reset of the AD7280. Two write commands are required to complete the reset operation. Bit D7 must be set high to put the AD7280 into Reset. Bit D7 must then be set low to bring the AD7280 out of Reset.

Select Acquisition Time

Bits D6 and D5 of the CONTROL register determine the Acquisition time of the ADC. Please refer to the Track-and-Hold section for further detail. The default value of the Conversion time setting is 00.

Table 15.Analog Input Acquisition Time.

D6 to D5	Acquisition Time
00	400 ns
01	800 ns
10	1.2 µs
11	1.6 µs

Thermistor Termination Resistor

Bit D3 of the CONTROL register should be set if the user wishes to use a single thermistor termination resistor on the VT_{TERM} pin. It should be noted that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280 is set to its highest value, that is, 1.6µs.

Lock Devices Address

Bit D2 of the CONTROL register is used in conjunction with bit D1 to allow individual Device Addresses for each AD7280 in the daisychain to be defined and locked to the part. Bit D1 is used to generate the individual Device Addresses which are presented to each AD7280 in the daisychain in the form of a write command. When bit D2 is set high the AD7280 locks to the Device Address which is has been presented with. This new Device Address is used for all subsequent CRC calculations. When bit D2 is reset low the Device Address of the AD7280 is not locked. In this case a Device Address of 0h will be used for CRC calculations.

Increment Device Address

Bit D1 of the CONTROL register determines whether the AD7280 increments the Device Address it receives as part of a write command when transferring that command up the daisychain. When bit D1 is set to 1 the Device Address is incremented as the command is passed up the chain. This mode of operation is used on initial power up and following a reset operation to allow individual Device Addresses for each AD7280 in the daisychain stack to be defined, When D1 is reset to 0 no change is made to the Device Address as the command is passed up the chain.

Daisychain Register Readback

Bit D0 of the CONTROL register enables the readback of individual registers from each AD7280 is a daisychain. When bit D0 is set high the application of sufficient clocks will allow the data stored in the register address identified by the READ register to be shifted out of each AD7280 in turn. This data will be passed down the daisychain and read back by the DSP/µP. When bit D0 is reset low daisychain read is disabled. Repeated read requests when D0 is low will result in the repeated readback of an individual register from a single device.

OVER VOLTAGE REGISTER

Table 16. 8-Bit Register

Fh	D7 to D0	Read/Write

The OVERVOLTAGE THRESHOLD register determines the high voltage threshold of the AD7280. Cell voltage conversions which exceed the Over Voltage threshold trigger the ALERT output. The AD7280 allows the user to set the Over Voltage threshold to a value between 1V and 5V. The resolution of the Over Voltage threshold is 8-bits, that is, 16mV. The default value of the Over Voltage threshold on power up is FFh.

UNDER VOLTAGE REGISTER

Table 17. 8-Bit Register

10h	D7 to D0	Read/Write

The UNDER VOLTAGE THRESHOLD register determines the low voltage threshold of the AD7280. Cell voltage conversions lower than the Under Voltage threshold trigger the ALERT output. The AD7280 allows the user to set the Under Voltage threshold to a value between 1V and 5V. The resolution of the Under Voltage threshold is 8-bits, that is, 16mV. The default value of the Under Voltage threshold on power up is 00h.

OVER TEMP REGISTER

Table 18. 8-Bit Register

11h	D7 to D0	Read/Write

The OVER TEMP THRESHOLD register determines the high temperature threshold of the AD7280. Cell temperature conversions which exceed the Over Temp threshold trigger the ALERT output. The AD7280 allows the user to set the Over Temperature threshold to a value between 0V and 5V. The resolution of the Over Temperature threshold is 8-bits, that is, 19mV. The default value of the Over Voltage threshold on power up is FFh.

UNDER TEMP REGISTER

Table 19. 8-Bit Register

12h	D7 to D0	Read/Write

The UNDER TEMP THRESHOLD register determines the low temperature threshold of the AD7280. Cell temperature conversions lower than the Under Voltage threshold trigger the ALERT output. The AD7280 allows the user to set the Under Temperature threshold to a value between 0V and 5V. The resolution of the Under Voltage threshold is 8-bits, that is, 19mV. The default value of the Under Voltage threshold on power up is 00h.

ALERT REGISTER

Table 20. 8-Bit Register

13h	D7 to D0	Read/Write

The ALERT register determines the configuration of the ALERT function. The ALERT can be configured to be a static or dynamic signal. The static signal is a high signal which is pulled low to indicate that an over/under voltage or over/under temperature has occurred. The dynamic signal is a square wave, the frequency of which can be set to either 100Hz or 1kHz. When a number of AD7280s are operating in daisy chain mode the ALERT configuration is set on the AD7280 furthest away from the uP or DSP only. The ALERT registers on the remaining AD7280s in the chain should be programmed to pass the ALERT signal through the chain. Each of these parts will pass the static or dynamic ALERT signal through the chain or pull the signal low to indicate that an over/under voltage or over/under temperature has occurred.

Table 21.ALERT Register settings

D7 to D6	D5 to D4	D3 to D0	AD7280 Action
00	XX	XXXX	No Alert signal generated or passed [Default]
01	XX	XXXX	Generates static [High] Alert signal to be passed down the Daisy Chain
10	00	XXXX	Generates 100Hz Square wave Alert signal to be passed down the Daisy Chain
10	01	XXXX	Generates 1kHz Square wave Alert signal to be passed down the Daisy Chain
10	10	XXXX	Reserved
10	11	XXXX	Reserved
11	XX	XXXX	Passes Alert signal from AD7280 at higher potential in Daisy Chain
D7 to D4	**D3 to D2**	**D1 to D0**	**AD7280 Action**
XXXX	00	XX	Includes all 6 Voltage channels in Alert detection [Default]
XXXX	01	XX	Removes Vin5 from Alert detection
XXXX	10	XX	Removes Vin5 & Vin4 from Alert detection
XXXX	11	XX	Reserved
XXXX	XX	00	Includes all 6 Temperature channels in Alert detection [Default]
XXXX	XX	01	Removes VT5 from Alert detection
XXXX	XX	10	Removes VT5 & VT3 from Alert detection

CELL BALANCE REGISTER

Table 22. 8-Bit Register

14h	D7 to D0	Read/Write

The CELL BALANCE register determines the status of the 6 Cell Balance outputs. The six CB outputs are set by writing to bits D7 to D2 of the Cell Balance register. The default value of the Cell Balance register on power up is 0h.

Table 23. Cell Balance register settings

D7	Set CB6 output 0 = output off

	1 = output on
D6	Set CB5 output
	0 = output off
	1 = output on
D5	Set CB4 output
	0 = output off
	1 = output on
D4	Set CB3 output
	0 = output off
	1 = output on
D3	Set CB3 output
	0 = output off
	1 = output on
D2	Set CB1 output
	0 = output off
	1 = output on
D1-D0	Reserved, set to 0

CB TIMER REGISTERS

Table 24. 8-Bit Register

15h to 1Ah	D7 to D0	Read/Write

The CB TIMER registers allows the user to program individual ON times for each of the Cell Balance outputs. The AD7280 allows the user to set the CB Timer to a value between 0 and 39 minutes. The resolution of the CB Timer is 75 seconds. The default value of the CB TIMER registers on power up is 0h.

Table 25. CB Timer register settings

D7-D3	5-bit binary code to set CB timer to value between 0 and 39 minutes
D2-D0	Reserved, set to 0

PD TIMER REGISTER

Table 26. 8-Bit Register

1Bh	D7 to D0	Read/Write

The PD TIMER register determines the elapsed time before the AD7280 is automatically powered down. The AD7280 allows the user to set the PD Timer to a value between 0 and 39 minutes. The resolution of the PD Timer is 75 seconds. When using the PD timer in conjunction with the CB timers the value programmed to the PD Timer should exceed that programmed to the CB Timer by at least 1 minute. The default value of the PD TIMER registers on power up is 0h.

Table 27. PD Timer register settings

D7-D3	5-bit binary code to set PD timer to value between 0 and 39 minutes
D2-D0	Reserved, set to 0

READ REGISTER

Table 28. 8-Bit Register

1Ch	D7 to D0	Read/Write

The READ register, in conjunction with bits D13 and D12 of the CONTROL register and bit D12 of the write operation define the read operations of the AD7280. To read back a single register from the AD7280 the register address should be first written to the Read register. To read back a series of conversion results from the AD7280 an address of 0h should be written to the Read register. The default value of the READ register on power up is 0h.

Table 29. Read register settings

D7-D2	6-bit binary address for the register to be read
D1-D0	Reserved, set to 0

CONTROL 3 REGISTER

Table 30. 8-Bit Register

1Dh	D7 to D0	Read/Write

The CONTROL 3 register allows the user to gate the input signal from the $\overline{\text{CNVST}}$ pin. This will hold the internal $\overline{\text{CNVST}}$ signal high regardless of any external noise or glitches on the $\overline{\text{CNVST}}$ pin. This may be used in noisy environments to prevent incorrect initiation of conversions. The default value of the CONTROL 3 register on power up is 0h.

Table 31. Read register settings

D7-D1	Reserved, set to 0
D0	0 = Function not in use
	1 = $\overline{\text{CNVST}}$ input gated

SERIAL INTERFACE

The AD7280's serial interface consists of four signals; $\overline{CS}$, SCLK, SDIN and SDOUT. The SDIN line is used for transferring data into the on chip registers while the SDOUT line is used for reading the conversion results from the ADCs. SCLK is the serial clock input for the device, and all data transfers, either on SDIN or on SDOUT, take place with respect to SCLK. Data is clocked into the AD7280 on the SCLK falling edge. Data is clocked out of the AD7280 on the SCLK rising edge. The $\overline{CS}$, input is used to frame the serial data being transferred to or from the device. $\overline{CS}$, can also be used to initiate the sequence of conversions.

Figure 20 shows the timing diagram for the serial interface of the AD7280. Please refer to the Daisy Chain Interface section for further information on the Daisy Chain Interface.

WRITING TO THE AD7280

In a Li-Ion Battery Monitoring application up to 20 AD7280's may be daisy chained together to allow up to 120 individual Li-Ion cell voltages to be monitored. Each write operation must therefore include Device Address and Register Address in addition to the data to be written. An additional identifier bit is also required when addressing all AD7280s in the Daisy Chain. The AD7280 SPI Interface, in combination with the Daisy Chain Interface, allows any register in the 20 x AD7280 stack to be updated using one 32-bit write cycle. The 32-bit write sequence is outlined in Table 32.

Device Address

The Device Address is a 5-bit address which allows each individual AD7280 in battery monitoring stack to be uniquely identified. On initial power up each AD7280 is configured with a default address of 0h. A simple sequence of commands, outlined in the Addressing the AD7280 section, allows each AD7280 to recognize it's unique in the stack. This devices address can be then locked to the AD7280 and will be used in subsequent read and write commands. The Device Address is written to and read from the AD7280 stack in reverse order, that is, LSB first.

Register Address

The register map for the AD7280 is outlined in Table 9. Each Register Address is 6-bit address and is used when writing to or reading from the on chip registers of the AD7280.

Register Data

When issuing a write command to a part in the stack of AD7280 devices the data to be written is an 8-bit word. As outlined in Table 9, all Read/Write registers are 8 bits wide. More details on the correct settings for each register may be found in the Register map section.

Address All Parts

The AD7280 allows write commands to be issued simultaneously to all devices on the daisychain, as well as write commands to individual AD7280s. A write to all devices on the daisychain is completed by setting the 'Address All Parts' bit, D12, of the write command to 1. When issuing a Write All command the Device Address should be set to 0h. This is also the Device Address to be used calculating the 8-bit CRC for transmission with the Write All command.

8-bit CRC

The AD7280 includes an 8-bit Cyclic Redundancy Check on all Write commands to either individual parts or to a chain of devices. An AD7280 which receives an invalid CRC in the Write command will not execute the command. The CRC on the write command is calculated based on bits D31 to D11 of the Write command. This includes the Device Address, the Register Address, the Data to be written, the Address All Parts bit and bit D11. Further information on the CRC is outlined in Cyclic Redundancy Check section.

READING FROM THE AD7280

There are two different types of read operation for the AD7280.

- Conversion Results Read
- Register Data Read

The data returned from a conversion result read operation includes the Device Address, the Channel Address, a Write Acknowledgement bit and the 8-bit CRC information in addition to the 12-bits of conversion data. The data returned from a Register Data read operation includes the Device Address, the Register Address, a Write Acknowledgement bit and the 8-bit CRC information in addition to the 8-bits of register data. The 32-bit Read cycle for a Conversion Result Read is outlined in Table 33. The 32-bit Read cycle for a Register Data Read is outlined in Table 34.

The AD7280 SPI Interface, in combination with the Daisy Chain Interface, allows the conversion results of any AD7280 in the 20 x AD7280 stack to be read back using an N x 32-bit read cycle, where N is defined by the number of conversions completed on that part, that is 12, 9 or 6 (Please refer to Table 6).

Device Address

The Device Address is a 5-bit address which allows each individual AD7280 in battery monitoring stack to be uniquely identified. On initial power up each AD7280 is configured with a default address of 0h. A simple sequence of commands, outlined in the Addressing the AD7280 section, allows each AD7280 to recognize it's unique in the stack. This device address can be then locked to the AD7280 and will be used in subsequent read and write commands. The Device Address is written to and read from the AD7280 stack in reverse order, that is, LSB first.

Channel Address

The Channel Address allows each individual Voltage and Temperature result to be uniquely identified. Each Channel Address is 4-bits wide. The address for each channel is detailed in the register map for the AD7280, Table 9.

Register Address

The register map for the AD7280 is outlined in Table 9. Each Register Address is 6-bit address and is used when writing to or reading from the on chip registers of the AD7280.

Conversion Data

The 12-bit conversion result from the Voltage inputs, the Temperature inputs or the ADC Self-test conversion.

Register Data

The 8-bit register data which was requested in a previous write command.

Write Acknowledgement bit

As indicated above (Writing to the AD7280), an 8-bit CRC is included in the Write command transmitted to the AD7280. This is calculated based on bits D31 to D11. A CRC check is completed before the write command is executed on the device. Using the same CRC algorithm the AD7280 calculates the CRC and compares it to that which was received by the part in the transmitted write command. If the two CRC values match the command is executed and the Write Acknowledgment bit in the subsequent transmission of data from the device is set. If the transmitted and calculated CRC do not match the write command will not be executed and the Write Acknowledgement bit will not be asserted, that is, it will be zero. For examples on the use of the Write Acknowledgment bit please refer to the Write Acknowledgement section.

8-bit CRC

The AD7280 includes an 8-bit Cyclic Redundancy Check on all data read back from the device, that is both Conversion result reads and register data reads. When reading back conversion data from the AD7280 the 8-bit CRC will include the Device address, the Channel Address, the Conversion Data and the Write Acknowledge bit. When reading back register data from the AD7280 the 8-bit CRC will include the Device address, the Register Address, the Register Data, two reserved zero-bits and the Write Acknowledge bit. In both cases the CRC is generated on bits D31 to D10 of the 32-bit read cycle, and is transmitted using bits D9 to D2 of the same read cycle. Further information on the CRC is outlined in Cyclic Redundancy Check section.

Table 32. 32-Bit Write Cycle

Device Address[1]	Register Address	Register Data	Address All Parts	Reserved [Zero-bit]	8-bit CRC	Reserved [Zero-bits]
D31-D27	D26-D21	D20- D13	D12	D11	D10-D3	D2-D0

Table 33. 32-Bit Read Conversion result Cycle

Device Address[2]	Channel Address	Conversion Data	Write Acknowledge	8-bit CRC	Reserved [Zero-bits]
D31-D27	D26-D23	D22-D11	D10	D9-D2	D1-D0

Table 34. 32-Bit Read Register Data Cycle

Device Address[2]	Register Address	Register Data	Zero	Write Acknowledge	8-bit CRC	Reserved [Zero-bits]
D31-D27	D26-D21	D20-D13	D12-D11	D10	D9-D2	D1-D0

[1] Device Address should be written LSB first. For example, to address the second device on the stack, that is, the first slave device, the sequence of bits input to the AD7280 should be 10000. The Register Address, Data bits and CRC bits are input MSB first.
[2] Device Address is read out LSB first. The Register Address, Channel Address, all Data bits and CRC bits are read out MSB first.

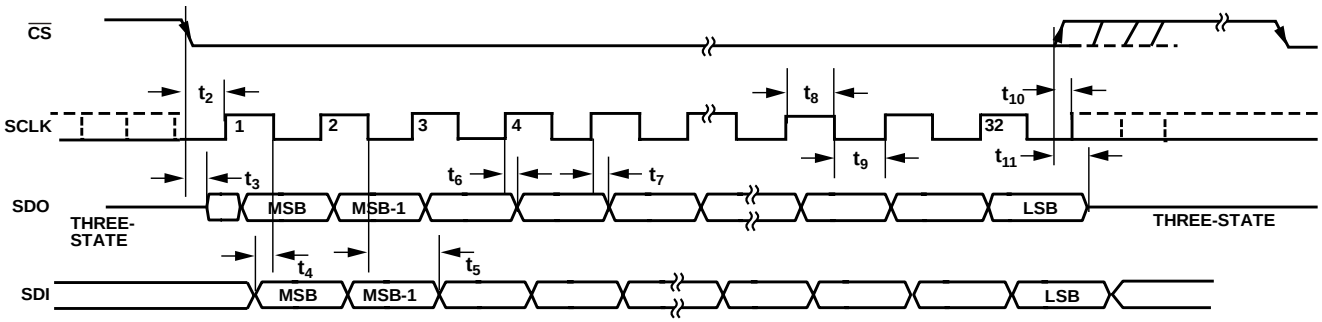


Figure 20. Serial Interface Timing Diagram

ADDRESSING THE AD7280

In any application using a chain of AD7280's the Device Address corresponds to the position of the individual AD7280 in the chain with respect to the device acting as Daisy Chain Master, that is the device connected directly to the DSP/µP. For example, in an application which uses 16 AD7280's to monitor 96 channels the device acting as Daisy Chain Master should be addressed with a Device Address of 00000, the 16th AD7280 in the chain should be addressed with a Device Address of 01111. This device address must be written to the part LSB first as outlined in Table 32.

On initial power up, when coming out of powerdown and following a reset operation all AD7280s in the Daisychain will default to a Device Address of 0h. The following sequence of commands should be followed to allow each AD7280 in the daisychain to recognize its unique position in the chain. It should be noted that the following sequence will allow Device Addresses on all parts in the chain to be configured and confirmed through daisychain readback. A subset of these commands may also be used to simply configure the Device Addresses without readback confirmation.

- A single Write All command should be sent to all devices in the chain to write the address of Control Register 2, Eh, to the Read register on all devices.
- A second Write All command should be sent to all devices in the chain to assert the Lock Device Address bit, D2, to de-assert the Increment Device Address bit, D1, and to assert the Daisychain Register Read bit, D0.
- To verify that all AD7280s in chain have received and locked their unique Device Address a Daisychain Register Read should now be requested from all devices. This may be done by continuing to apply sets of 32 SCLKs framed by CS until the Control register 2 of each device in the daisychain has been read back. The user should confirm that all device addresses are in sequence.

To write to the same register on all AD7280's in the stack, bit D12, the address all bit, in the 32-bit write cycle should be set high. This will result in the 8-bit register data, bits D20-D13, being written to the same register address on all parts. The Device address, bits D32-D27, should be set to 0 when writing to all parts in the stack and this device address should be used in the CRC calculation, see the Cyclic Redundancy Check section for more information. For example, when initiating a conversion using the rising edge of $\overline{CS}$, on all AD7280s in the stack the following 32 bit write sequence must be written to the device:

- Device address bits D31-D27 should be set to 0.
- Register address bits D26-D21 should be set to Dh to address the Control register.
- Register data bits D20-D13 should be set to the required settings for conversions/readback with bit D11 set to 1 in order to initiate conversions on the rising edge of $\overline{CS}$.
- Bit D12 should be set to 1 to address all parts in the stack.
- The result of the CRC calculation should be filled into bits D10-D3,

This will initiate a conversion on the rising edge of $\overline{CS}$, on all AD7280s in the stack.

WRITE ACKNOWLEDGEMENT

The AD7280 SPI interface allows the user to write and read data to and from the AD7280 at the same time, that is, as the device is reading in one command it can provide output data on the SDOUT pin in the same read/write cycle.

On all writes to the AD7280, the device will internally perform a CRC calculation on the received data, bits D31 to D11, and it will verify this CRC against that transmitted by the DSP/uP. If there is a difference between the CRC generated internally and that received from the DSP/uP, the AD7280 will not perform the write operation. If a subsequent 32 SCLK cycles framed by a $\overline{CS}$ pulse are applied to the AD7280, bit D10, the Write Acknowledgement bit on SDOUT will indicate to the processor if the last write to the device was successful (the Write

Acknowledgement bit will be set if the write was successful). The Write Acknowledgement bit is included in the 8-bit CRC on the read cycle.

An example of how this could be used when writing to and configuring a stack of AD7280 devices would be as follows; this example sets the over-voltage thresholds on all devices in the stack containing 16 AD7280s:

- Execute a write all command to set register address Fh (Over Voltage register) to the desired over voltage threshold level
- Apply a further 16 sets of 32 SCLKs, each framed by $\overline{CS}$ to the master device
- A total of 17 sets of 32 SCLK frames have now been applied to the device. The data read back from the master device on the second 32 SCLK frame will include the Write Acknowledgement bit for the Over Voltage register write to the master device. The data read back from the master device on the third 32 SCLK from will include the Write Acknowledgement bit for the Over Voltage register write to the first slave device in the stack and so on.

It should be noted that by adding an additional step of writing to the Read register on all devices in the stack first and pointing to the register being written to ensures that the data provided back from the stack of AD7280s includes this register data. In this way, the CRC generated by the AD7280 and sent with the data already includes the data you have previously written to that register.

CYCLIC REDUNDANCY CHECK

The AD7280 32-bit SPI interface includes an 8-bit Cyclic Redundancy Check (CRC) on the read and write cycles. This CRC may be used to detect any alteration in the data during transmission to and from the AD7280. The principle of a cyclic redundancy check is that the data to be transmitted is divided by a fixed polynomial, the remainder of this mathematical operation is then attached to the data and forms part of the transmission. At the receiving end the same mathematical operation should be completed on the data received. This will confirm that the data received is the same as the data which was originally transmitted.

The polynomial used by the AD7280 to calculate the CRC bits is $x^8 + x^5 + x^3 + x^2 + x + 1$. The division is implemented using the digital circuit outlined in Figure 21.

Write Operation CRC

For writes to the AD7280, the CRC will need to be computed in the DSP/uP and sent as part of the write command. The CRC must be computed on bits D31 to D11 of the write command, that is, the device address, the register address, the data to be written, the address all parts bit and bit D11 which is a reserved zero input bit. The data is divided by the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ and the 8 bit remainder, following the division, becomes the CRC bits, CRC[7] to CRC[0]. Note, if the user is addressing all parts in the stack of AD7280s (by asserting the Address All Parts bit D12), the CRC must be computed using a device address of 0h and the data written to the device must have a device address of 0h. The AD7280 will perform the same CRC calculation on bits D31 to D11 received by AD7280 and it will verify this CRC against that transmitted by the DSP/uP. If there is a difference between the CRC generated within the AD7280 and that received from the DSP/uP, the AD7280 will not perform the write operation. To allow the user to verify that the command has been received and implemented by the AD7280s in the stack, a Write Acknowledgement bit is also included in the 32-bit read cycles. For more information of the Write Acknowledgment bit, see the Write Acknowledgement section.

Read Operation CRC

For reads from the AD7280, the 8-bit CRC is generated by the AD7280 based on bits D31 to D10 of the 32 bit read cycle and is transmitted using bits D9 to D2 of the same read cycle. When reading back conversion data from the AD7280, the 8-bit CRC will include the device address, the channel address, the conversion data and the write acknowledgement bit. When reading back register data from the AD7280 the 8-bit CRC will include the device address, the register address, the register data, two reserved zero bits and the write acknowledgement bit. The data received is divided by the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ and the 8 bit remainder, following the division, becomes the CRC bits, CRC[7] to CRC[0]. The user can compare the CRC bits calculated, with the CRC that was received from the AD7280 to check if there was any alteration in the data that was transmitted by the AD7280.

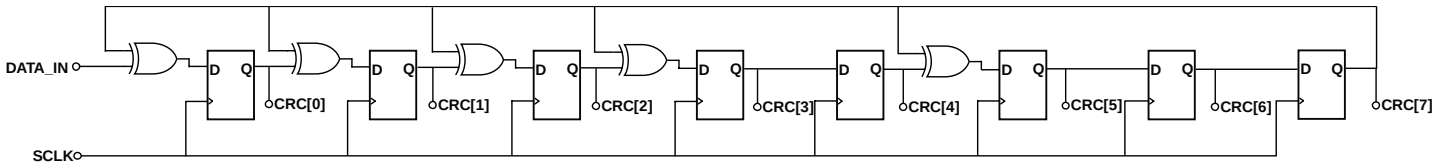


Figure 21. CRC Implementation

CRC Pseudo Code

The following pseudo code may be used to calculate the CRC. First, the following variables need to be declared:

Num_Bits – The number of data bits that will be used to calculate the CRC result, 21 for a data write to the AD7280 and 22 for a data read from the AD7280.

i – Integer variable.

xor_1, xor_2, xor_3, xor_4, xor_5 – Integer varibles. These are the outputs of the XOR gates starting with the leftmost XOR gate in the circuit implementation in Figure 21.

data_in – Data bits that the CRC will be calculated on. D31 to D11 for a write operation and D31 to D10 for a read operation. This data supplies the input to the first XOR gate.

CRC_0, CRC_1, CRC_2, CRC_3, CRC_4, CRC_5, CRC_6, CRC_7 – Integer variables. The outputs of the shift registers starting at the leftmost shift register in the circuit implementation in Figure 21.

With the exception of data_in, all variables should be initialised to zero. The following code will then implement the CRC calculation as outlined in Figure 21 above.

```
for (i=Num_Bits; i>=0; i--)
        {
        xor_5 = CRC_4 ^ CRC_7;
        xor_4 = CRC_2 ^ CRC_7;
        xor_3 = CRC_1 ^ CRC_7;
        xor_2 = CRC_0 ^ CRC_7;
        xor_1 = data_in[i] ^ CRC_7;

        CRC_7 = CRC_6;
        CRC_6 = CRC_5;
        CRC_5 = xor_5;
        CRC_4 = CRC_3;
        CRC_3 = xor_4;
        CRC_2 = xor_3;
        CRC_1 = xor_2;
        CRC_0 = xor_1;
        }
```

CRC Calculation Example 1:

Writing data to the high byte of the Control Register of device 0 in the stack, that is, the lowest device in the stack.

The CRC is computed in the DSP/uP on bits D31 to D11, that is, the device address, the register address, the data to be written to the register, the address all parts bit and the reserved 0.

Device Address: 00000 (5'h0)

Register Address: 001101 (6'hD)

Data: 00001100 (8'hC)

Address all bits: 0 (1'h0)

Reserved 0: 0 (1'h0)

The data input to the CRC algorithm is therefore 000000011010000110000 (21'h3430). Following the completion of the calculation, the value of CRC_7 to CRC_0 is 01010001 (8'h51). The data that is sent to the AD7280 for this serial write is therefore:

0000 0001 1010 0001 1000 0010 1000 1000 (32'h1A18288)

CRC Calculation Example 2:

Writing data to the high byte of the Control Register of device address 17 in the stack.

The CRC is computed in the DSP/uP on bits D31 to D11 i.e. the device address, the register address, the data to be written to the register, the address all parts bit and the reserved 0.

Device Address (written LSB first): 10001 (5'h11)

Register Address: 001101 (6'hD)

Data: 00001100 (8'hC)

Address all bits: 0 (1'h0)

Reserved 0: 0 (1'h0)

The data input to the CRC algorithm is therefore 100010011010000110000 (21'h113430). Following the completion of the calculation, the value of CRC_7 to CRC_0 is 10011101 (8'h9D). The data that is sent to the AD7280 for this serial write is therefore:

1000 1001 1010 0001 1000 0100 1110 1000 (32'h89A184E8)

CRC Calculation Example 3:

Reading the data from the low byte of the Control Register of device 0 in the stack, that is, the lowest device in the stack.

The CRC is computed in the AD7280 on bits D31 to D10, that is, the device address, the register address, the register data, two reserved zero bits and the write acknowledgement bit. The calculated CRC is sent along with bits D31 to D10 to the DSP/uP.

The data received from the AD7280 is as follows:

0000 0001 1100 0010 1000 0110 0110 1000 (32'h1C28668)

Device Address: 00000 (5'h0)

Register Address: 001110 (6'hE)

Register Data: 00010100 (8'h14)

Reserved 0's: 0 (2'h0)

Write Acknowledgement: 1 (1'h1)

CRC: 10011010 (8'h9A)

The CRC bits are computed again in the DSP/uP on bits D31 to D10 of the data that is read back from the AD7280. The data input to the CRC algorithm is therefore 0000000111000010100001 (22'h70A1). Following the completion of the calculation, the value of CRC_7 to CRC_0 is 10011010 (8'h9A). This result matches the CRC that was sent from the AD7280 so this transmission of data is valid.

CRC Calculation Example 4:

Reading the conversion result from channel Vin3 on device 1 in the stack.

The CRC is computed in the AD7280 on bits D31 to D13, that is, the device address, the channel address, the conversion data, and the write acknowledgement bit. The calculated CRC is sent along with bits D31 to D10 to the DSP/uP.

The data received from the AD7280 is as follows:

1000 0001 0100 1100 1101 0101 0001 1000 (32'h814CD518)

Device Address (read LSB first): 10000 (5'h10)

Channel Address: 0010 (4'h2)

Conversion Data: 100110011010 (12'h99A)

Write Acknowledgement: 1 (1'h1)

CRC: 01000110 (8'h46)

The CRC bits are computed again in the DSP/uP on bits D31 to D10 of the data that is read back from the AD7280. The data input to the CRC algorithm is therefore 1000000101001100110101 (22'h205335). Following the completion of the calculation, the value of CRC_7 to CRC_0 is 01000110 (8'h46). This result matches the CRC that was sent from the AD7280 so this transmission of data is valid.

DAISY CHAIN INTERFACE

In a Li-Ion Battery Monitoring application up to 20 AD7280's may be daisy chained together to allow up to 120 individual Li-Ion cell voltages to be monitored. Each AD7280 is capable of monitoring up to 6 Li-Ion cells and is powered from the top and bottom voltage of the 6 Li-Ion cells. As a result the supply voltages of each AD7280 are offset by up to 30V from adjacent AD7280's in the chain. For this reason a standard Serial Interface Daisy Chain method cannot be used.

The AD7280 includes a Daisy Chain Interface separate to the standard SPI interface. This Daisy Chain interface allows each AD7280 in the chain to relay data to and from adjacent AD7280's. In addition to the standard 4 wire SPI the AD7280 serial interface include 3 optional interface pins, ALERT, $\overline{\text{CNVST}}$ and $\overline{\text{PD}}$.

Each input and output pin on the 7 wire interface requires at least one additional I/O for the Daisy Chain Interface, that is, to allow the information to be passed to an AD7280 operating at a higher supply voltage. The SDO and ALERT outputs will also require a further daisy chain pin to allow the information to be passed to an AD7280 operating at a lower supply voltage. The remaining 5 interface pins, $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{CNVST}}$ and $\overline{\text{PD}}$ do not require additional pins to pass information to a AD7280 operating at a lower voltage as each of these input pins can operate as both SPI inputs or Daisy Chain inputs. Their functionality is defined by the state of the Master pin.

The MASTER pin on the AD7280 at the base of the Daisy Chain should be set high, tied to V_{DD} supply, to ensure that this device interfaces to the DSP or µProcessor using the standard Serial Interface. The MASTER pin on the remaining AD7280s in the Daisy Chain should each be connected to their respective V_{SS} pins which disable the serial interface pins on those devices. This allows the $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{CNVST}}$ and $\overline{\text{PD}}$ inputs, in addition to the SDOlo and ALERTlo outputs, to pass signals to and from an AD7280 operating at a lower potential.

As explained in the Serial Interface section only one 32-bit write cycle is required to write to any register in the 20 x AD7280 stack. To read back the conversion data from all channels monitoring the battery stack requires only a (32 x N)-bit read cycle where N is the number of channels in the battery stack. Note: this is the default read configuration on power up. If the settings of the Read or control registers have been changed then additional write cycles may be required. The recommended SCLK frequency to ensure correct operation of the Daisy Chain Interface is 1MHz. With a 1MHz SCLK it will take ~3.2 ms to read back the voltage conversions on 96 channels.

It should be noted that when reading from a single device in a stack of AD7280s, in some cases the SCLK frequency will need to be lower than 1MHz in order to read back the register data from parts up the chain of AD7280s. This is due to the propagation delay between adjacent parts on the daisychain, see t_{DELAY} in Table 2. This delay does not apply if the part is reading registers or conversion data from the part in daisychain mode, that is, the max SCLK of 1MHz can always be used in daisychain mode.

When reading back both register and conversion data from the device using the daisychain readback mode, the SDI line must not just idle high or low but must be set up to address and write to either the top device in the chain or address and write to a part higher than the top device in the chain and set the Address All Parts bit to 0. A recommendation would be to write to the top available address, that is, address 31 and set the Address All Parts bit to 0.

READING DATA FROM THE AD7280

There are a number of read options available on the AD7280. The user may read back the results from all the conversions completed on an individual part in the chain, from all the conversions completed on all parts in the chain or from individual registers on selected parts in the chain.

In each case the user is required to first write to the Read register on the selected parts to configure that part to supply the correct data on the outputs. When reading back an individual register result, the address of that register should be written to the read register of the selected part. When reading back conversion results from any or all parts in the chain an address of 0h should be written to the read register of the selected parts. When the address written to the read register is 0h the conversion results selected for read back are controlled by setting bits D13 and D12 of the Control register. Please refer to Table 14. This allows the user to select 4 different read back options

- Read back 12 conversion results: 6 voltage and 6 temperature
- Read back 9 conversion results: 6 voltage and 3 temperature
- Read back 6 conversion results: 6 voltage results only
- Switch off read operation on this part

If the user wishes to read back the conversion results from a single AD7280 in the daisy chain bits D13 and D12 of the control register on that part should be set to select the correct conversion results. Bits D13 and D12 on all other AD7280s in the daisy chain should be set to switch off the read operation on those parts. It should be noted that it is more efficient in terms of 32-bit write cycles to first switch off the read operation on all AD7280s in the daisy chain. This can be achieved with a single write cycle, using bit D12 to address all parts in the chain. The user may then address the individual part and set bits D13 and D12 to select the required conversion results.

When reading back conversion data from any, or all, of the AD7280s in a daisy chain the conversion results returned from the AD7280 will be the last completed set of conversions on that part. It is recommended that the user also set bits D15 and D14 of the control register, to select the number of conversions to be completed on each part, and initiate the conversions through either the $\overline{\text{CNVST}}$ pin or the rising edge of $\overline{\text{CS}}$, as part of the read operation. This allows the user to implement a simple convert and read back routine with the most efficient number of 32-bit write and read operations. A general example of this routine, which would convert and read back from all parts in the AD7280 daisy chain would be:

- Write 0h to the Read register on all of the parts in the daisychain. Note: 0h is the default value of this register on power up and following a reset operation.
- Write to the Control register on all parts. Set bits D15 and D14 to select the required conversions. Set bits D13 and D12 to select the required conversion results for read back.
- Initiate the conversions through either the falling edge of $\overline{\text{CNVST}}$ or the rising edge of $\overline{\text{CS}}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Please refer to Converting Cell Voltages and Temperatures section.
- Apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

The following section outlines eleven examples of Conversion and/or Readback routines which would be commonly used in an application using a chain of AD7280s to monitor the voltage and/or temperature of the a stack of Lithium Ion batteries.

Example 1: Convert and Read all parts, all voltages and all temperatures

- Register address 0h should be written to the Read register on all parts. A Device Address of 0 is used when computing the CRC for commands to write to all parts. The 32 bit write command is 32'h38011C8. For a breakdown see Table 35, Example 1, Write 1.
- Bits D15-D12 of the CONTROL register should be set to 0 on all parts. The 32 bit write command is 32'h1A01318. For a breakdown see Table 35, Example 1, Write 2.
- Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

Example 2: Convert and Read all parts, all voltages and three temperatures per part

- Register address 0h should be written to the Read register on all parts. A Device Address of 0 is used when computing the CRC for commands to write to all parts. The 32 bit write command is 32'h38011C8. For a breakdown see Table 35, Example 2, Write 1.
- Bits D15 and D13 of the CONTROL register should be set to 0, bits D14 and D12 should be set to 1 on all parts. The 32 bit write command is 32'h1AA1060. For a breakdown see Table 35, Example 2, Write 2.

- Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

Example 3: Convert and Read all parts, all voltages and no temperatures

- Register address 0h should be written to the Read register on all parts. A Device Address of 0 is used when computing the CRC for commands to write to all parts. The 32 bit write command is 32'h38011C8. For a breakdown see Table 35, Example 3, Write 1.
- Bits D15 and D13 of the CONTROL register should be set to 1, bits D14 and D12 should be set to 0 on all parts. The 32 bit write command is 32'h1B415E8. For a breakdown see Table 35, Example 3, Write 2.
- Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

Example 4: Convert and Read one part, all voltages and all temperatures

- Register address 0h should be written to the Read register of the part that is to be read. This example uses a device address of 2. The 32 bit write command is 32'h438005F0. For a breakdown see Table 35, Example 4, Write 1.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts. The 32 bit write command is 32'h1A61518. For a breakdown see Table 35, Example 4, Write 2.
- Bits D15-D12 of the CONTROL register of the part to be read from should be set to 0. This example uses a device address of 2. The 32 bit write command is 32'h41A00720. For a breakdown see Table 35, Example 4, Write 3.
- Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

Example 5: Convert and Read one part, all voltages and temperatures 1, 3 & 5

- Register address 0h should be written to the Read register of the part that is to be read. This example uses a device address of 5. The 32 bit write command is 32'hA3800658. For a breakdown see Table 35, Example 5, Write 1.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts. The 32 bit write command is 32'h1A61518. For a breakdown see Table 35, Example 5, Write 2.
- Bit D15 and D13 of the CONTROL register of the part to be read from should be set to 0 and bits D14 and D12 should be set to 1. This example uses a device address of 5. The 32 bit write command is 32'hA1AA07F0. For a breakdown see Table 35, Example 5, Write 3.
- Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

Example 6: Convert and Read one part, all voltages, no temperatures

- Register address 0h should be written to the Read register of the part that is to be read. This example uses a device address of 7. The 32 bit write command is 32'hE3800270. For a breakdown see Table 35, Example 6, Write 1.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts. The 32 bit write command is 32'h1A61518. For a breakdown see Table 35, Example 6, Write 2.
- Bits D14 and D12 of the CONTROL register of the part to be read from should be set to 0 and bits D15 and D13 should be set to 1. This example uses a device address of 7. The 32 bit write command is 32'hE1B40650. For a breakdown see Table 35, Example 6, Write 3.
- Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.

- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

Example 7: Convert and Read a single voltage or temperature result

- The register address corresponding to the voltage or temperature result to be read should be written to the Read register of the part that is to be read, see Table 9 for register addresses. This example reads the Cell Voltage 6 result from device 3 in the stack. The 32 bit write command is 32'hC3828658. For a breakdown see Table 35, Example 7, Write 1.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts. The 32 bit write command is 32'h1A61518. For a breakdown see Table 35, Example 7, Write 2.
- Bits D13 and D12 of the CONTROL register of the part to be read from should be set such that a conversion will be completed on the required channel. Note: With the exception of a Self-Test conversion it is not possible to convert on a single channel, 6, 9 or 12 conversions must be completed. This example reads a voltage conversion from device 3 in the stack so bits D14 and D12 of the CONTROL register should be set to 0 and bits D15 and D13 should be set to 1 on device 3. The 32 bit write command is 32'h C1B400F8. For a breakdown see Table 35, Example 7, Write 3.
- Initiate conversions through the falling edge of $\overline{CNVST}$.
- Allow sufficient time for each conversion to be completed plus 5µs. Following the completion of the conversions, apply a $\overline{CS}$ low pulse that frames 32 SCLKs to read back the desired voltage or temperature result.

Example 8: Read a single configuration register all parts

- Bit D0 of the CONTROL register should be set to 1 on all parts. This enables the Daisychain Register Read operation on all parts. The 32 bit write command is 32'h1C2B6E0. For a breakdown see Table 35, Example 8, Write 1.
- The register address corresponding to the configuration register to be read should be written to the Read register on all parts, see Table 9 for register addresses. This example reads the Cell Balance register from all parts. The 32 bit write command is 32'h3829348. For a breakdown see Table 35, Example 8, Write 2.
- Apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each device in the stack to read back the desired register contents from all parts.

Example 9: Read a single register

- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts. The 32 bit write command is 32'h1A61518. For a breakdown see Table 35, Example 9, Write 1.
- Bits D13 and D12 of the CONTROL register of the part to be read from should be set to 0. This example reads from part 1 in the stack. The 32 bit write command is 32'h81A00220. For a breakdown see Table 35, Example 9, Write 2.
- The register address corresponding to the configuration register to be read should be written to the Read register of the part that is to be read, see Table 9 for register addresses. This example reads the Alert register from part 1 in the stack. The 32 bit write command is 32'h83898008. For a breakdown see Table 35, Example 9, Write 3.
- Apply a $\overline{CS}$ low pulse that frames 32 SCLKs to read back the desired register contents.

Example 10: Self-Test conversion, all parts

- Bits D15-D14 of the CONTROL register should be set to 1 and bits D13-D12 should be set to 0 on all parts to select the self-test conversion. The 32 bit write command is 32'h1B81090. For a breakdown see Table 35, Example 10, Write 1.
- Initiate conversions through the falling edge of $\overline{CNVST}$.
- Bit D0 of the CONTROL register should be set to 1 on all parts. This enables the Daisychain Register Read operation on all parts. The 32 bit write command is 32'h1C2B6E0. For a breakdown see Table 35, Example 10, Write 2.
- The register address corresponding to the self-test conversion should be written to the Read register of all parts, see Table 9 for register addresses. The 32 bit write command is 32'h38617C8. For a breakdown see Table 35, Example 10, Write 3.
- Allow sufficient time for each conversion to be

completed plus 5µs. Following the completion of the conversions, apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each device in the stack.

Example 11: Self-Test conversion, single part

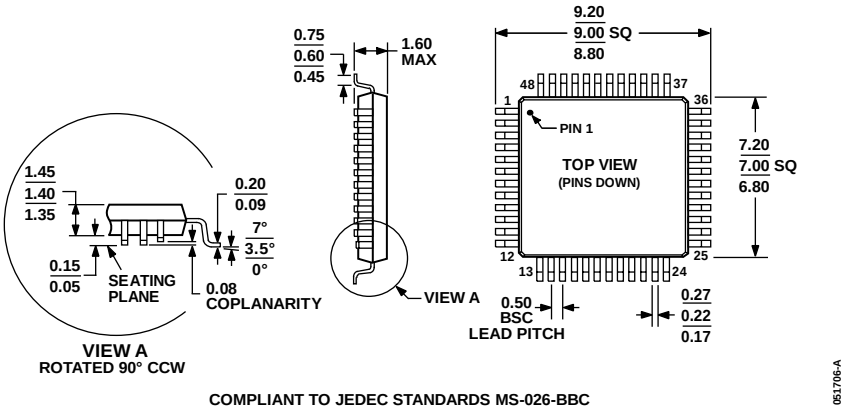
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts. Bit D8 in the CONTROL register of all parts should be set to 1 to put each part into a software power down. This prevents the ALERT function on the parts not undergoing a self-test conversion from being triggered. The 32 bit write command is 32'h1A63538. For a breakdown see Table 35, Example 11, Write 1.
- Bit D8 in the CONTROL register of the part for which a self-test conversion is requested should be set to 0. This brings this part out of software power down. Bits D15-D14 of the CONTROL register should be set to 1 on the part under test to select the self-test conversion. Bits D13-D12 of the CONTROL register should be set to 0 the part under test to enable reads. This example reads self-test conversion result from device 4 in the stack. The 32 bit write command is 32'h21B80628. For a breakdown see Table 35, Example 11, Write 1.
- Initiate conversions through the falling edge of $\overline{CNVST}$.
- The register address corresponding to the self-test conversion should be written to the Read register of the part under test (device 4 in this case); see Table 9 for register addresses. The 32 bit write command is 32'h23860170. For a breakdown see Table 35, Example 11, Write 3.
- Allow sufficient time the self-test conversion to be completed plus 5µs. Following the completion of the conversion, apply a $\overline{CS}$ low pulse that frames 32 SCLKs to read back the single self-test result.

Table 35. Reading Data from the AD7280 Examples

	Device Address	Register Address	Data	Write All	0	8-bit CRC	000	32-bit Write Command
Example 1 – Write 1	00000 = 5'h0	011100 = 6'h1C	00000000 = 8'h0	1	0	00111001 = 8'h39	000	32'h38011C8
Example 1 – Write 2	00000 = 5'h0	001101 = 6'hD	00000000 = 8'h0	1	0	01100011 = 8'h63	000	32'h1A01318
Example 2 – Write 1	00000 = 5'h0	011100 = 6'h1C	00000000 = 8'h0	1	0	00111001 = 8'h39	000	32'h38011C8
Example 2 – Write 2	00000 = 5'h0	001101 = 6'hD	01010000 = 8'h50	1	0	00001100 = 8'hC	000	32'h1AA1060
Example 3 – Write 1	00000 = 5'h0	011100 = 6'h1C	00000000 = 8'h0	1	0	00111001 = 8'h39	000	32'h38011C8
Example 3 – Write 2	00000 = 5'h0	001101 = 6'hD	10100000 = 8'hA0	1	0	10111101 = 8'hBD	000	32'h1B415E8
Example 4 – Write 1	01000 = 5'h8	011100 = 6'h1C	00000000 = 8'h0	0	0	10111110 = 8'hBE	000	32'h438005F0
Example 4 – Write 2	00000 = 5'h0	001101 = 6'hD	00110000 = 8'h30	1	0	10100011 = 8'hA3	000	32'h1A61518
Example 4 – Write 3	01000 = 5'h8	001101 = 6'hD	00000000 = 8'h0	0	0	11100100 = 8'hE4	000	32'h41A00720
Example 5 – Write 1	10100 = 5'h14	011100 = 6'h1C	00000000 = 8'h0	0	0	11001011 = 8'hCB	000	32'hA3800658
Example 5 – Write 2	00000 = 5'h0	001101 = 6'hD	00110000 = 8'h30	1	0	10100011 = 8'hA3	000	32'h1A61518
Example 5 – Write 3	10100 = 5'h14	001101 = 6'hD	01010000 = 8'h50	0	0	11111110 = 8'hFE	000	32'hA1AA07F0
Example 6 – Write 1	11100 = 5'h1C	011100 = 6'h1C	00000000 = 8'h0	0	0	01001110 = 8'h4E	000	32'hE3800270
Example 6 – Write 2	00000 = 5'h0	001101 = 6'hD	00110000 = 8'h30	1	0	10100011 = 8'hA3	000	32'h1A61518
Example 6 – Write 3	11100 = 5'h1C	001101 = 6'hD	10100000 = 8'hA0	0	0	11001010 = 8'hCA	000	32'hE1B40650
Example 7 – Write 1	11000 = 5'h18	011100 = 6'h1C	00010100 = 8'h14	0	0	11001011 = 8'hCB	000	32'hC3828658
Example 7 – Write 2	00000 = 5'h0	001101 = 6'hD	00110000 = 8'h30	1	0	10100011 = 8'hA3	000	32'h1A61518

Example 7 – Write 3	11000 = 5'h18	001101 = 6'hD	10100000 = 8'hA0	0	0	00011111 = 8'h1F	000	32'hC1B400F8
Example 8 – Write 1	00000 = 5'h0	001110 =6'hE	00010101 = 8'h15	1	0	11011100 = 8'hDC	000	32'h1C2B6E0
Example 8 – Write 2	00000 = 5'h0	011100 = 6'h1C	01010000 = 8'h50	1	0	01010110 = 8'h56	000	32'h38A12B0
Example 9 – Write 1	00000 = 5'h0	001101 = 6'hD	00110000 = 8'h30	1	0	10100011 = 8'hA3	000	32'h1A61518
Example 9 – Write 2	10000 = 5'h10	001101 = 6'hD	00000000 = 8'h0	0	0	01000100 = 8'h44	000	32'h81A00220
Example 9 – Write 3	10000 = 5'h10	011100 = 6'h1C	01001100 = 8'h4C	0	0	00000001 = 8'h01	000	32'h83898008
Example 10 – Write 1	00000 = 5'h0	001101 = 6'hD	11000000 = 8'hC0	1	0	00010010 = 8'h12	000	32'h1B81090
Example 10 – Write 2	00000 = 5'h0	001110 =6'hE	00010101 = 8'h15	1	0	11011100 = 8'hDC	000	32'h1C2B6E0
Example 10 – Write 3	00000 = 5'h0	011100 = 6'h1C	00110000 = 8'h30	1	0	11111001 = 8'hF9	000	32'h38617C8
Example 11 – Write 1	00000 = 5'h0	001101 = 6'hD	00110001 = 8'h31	1	0	10100111 = 8'hA7	000	32'h1A63538
Example 11 – Write 2	00100 = 5'h4	001101 = 6'hD	11000000 = 8'hC0	0	0	11000101 = 8'h C5	000	32'h21B80628
Example 11 – Write 3	00100 = 5'h4	011100 = 6'h1C	00110000 = 8'h30	0	0	00101110 = 8'h 2E	000	32'h23860170

OUTLINE DIMENSIONS

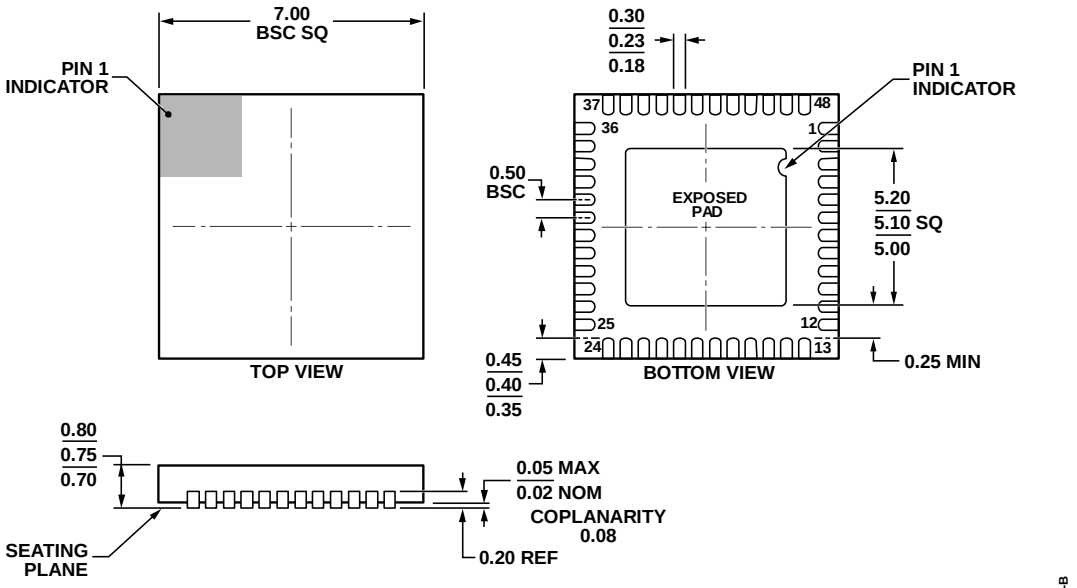


COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 22. 48-Lead Low Profile Quad Flat Package [LQFP]

(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 23. 48-Lead Frame Chip Scale Package [LFCSP]

(CP-48-4)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7280WBSTZ[1]	–40°C to +85°C	48-Lead LQFP	ST-48
AD7280WDSTZ[1]	–40°C to +105°C	48-Lead LQFP	ST-48
AD7280WBCPZ[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-4
AD7280WDCPZ[1]	–40°C to +105°C	48-Lead LFCSP	CP-48-4

[1] Z = Pb-free part.

PR07731-0-10/09(PrF)