AD587* PRODUCT PAGE QUICK LINKS

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Application Notes

- AN-713: The Effect of Long-Term Drift on Voltage References

Data Sheet

- AD587: High Precision 10 V Reference Data Sheet
- AD587: Military Data Sheet

TOOLS AND SIMULATIONS

- AD587 SPICE Macro-Model

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- AD587 Material Declaration
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REVISION HISTORY

9/07—Rev. G to Rev. H

Deleted AD587L Grade ... Universal
Change to Product Highlights ... 1
Changes to the Negative Reference Voltage from an AD587 Section ... 9
Changes to Figure 19 ... 10
Changes to Figure 21 and Figure 22 ... 10
Updated Outline Dimensions ... 11
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4/05—Rev. F to Rev. G

Updated Format ... Universal
Added Table 3 ... 5
Updated Outline Dimensions ... 11
Changes to Ordering Guide ... 13

7/04—Rev. E to Rev. F

Changes to Ordering Guide ... 3

7/03—Rev. D to Rev. E.

Deletion of S and T Grades ... Universal
Edits to Ordering Guide ... 2
Deletion of Die Specifications ... 3
Edits to Figure 3 ... 4
Updated Outline Dimensions ... 9

SPECIFICATIONS

T_A = 25°C, V_{IN} = 15 V, unless otherwise noted.

Table 1.

	AD587J			AD587K			AD587U			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
OUTPUT VOLTAGE	9.990		10.010	9.995		10.005	9.995		10.005	V
OUTPUT VOLTAGE DRIFT[1]										
0°C to 70°C			20			10			5	ppm/°C
−55°C to +125°C			20			10			5	ppm/°C
GAIN ADJUSTMENT	+3			+3			+3			%
	−1			−1			−1			%
LINE REGULATION[1]										
13.5 V ≤ $+V_{IN}$ ≤ 36 V										
T_{MIN} to T_{MAX}			±100			±100			±100	µV/V
LOAD REGULATION[1]										
Sourcing 0 mA < I_{OUT} < 10 mA										
T_{MIN} to T_{MAX}			±100			±100			±100	µV/mA
Sourcing −10 mA < I_{OUT} < 0 mA[2]										
T_{MIN} to T_{MAX}			±100			±100			±100	µV/mA
QUIESCENT CURRENT		2	4		2	4		2	4	mA
POWER DISSIPATION		30			30			30		mW
OUTPUT NOISE										
0.1 Hz to 10 Hz		4			4			4		µV p-p
Spectral Density, 100 Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY		±15			±15			±15		ppm/1000 hr
SHORT-CIRCUIT CURRENT-TO-GROUND		30	70		30	70		30	70	mA
SHORT-CIRCUIT CURRENT-TO-$+V_{IN}$		30	70		30	70		30	70	mA
TEMPERATURE RANGE										
Specified Performance (J, K)	0		70	0		70	0		70	°C
Operating Performance (J, K)[3]	−40		+85	−40		+85	−40		+85	°C
Specified Performance (U)	−55		+125	−55		+125	−55		+125	°C
Operating Performance (U)[3]	−55		+125	−55		+125	−55		+125	°C

[1] Specification is guaranteed for all packages and grades. CERDIP-packaged parts are 100% production tested.
[2] Load regulation (sinking) specification for SOIC (R-8) package is ±200 µV/mA.
[3] The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
$+V_{IN}$ to Ground	36 V
Power Dissipation (25°C)	500 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Package Thermal Resistance	
θ_{JC}	22°C/W
θ_{JA}	110°C/W
Output Protection	
Short to Ground	Indefinite[1]
Short to $+V_{IN}$	Momentary[1]

[1] Period for which output is safe.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

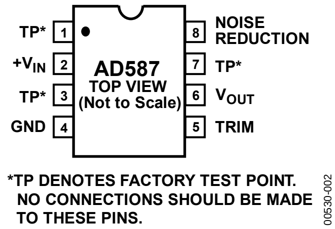


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 7	TP	No Connection. Leave floating.
2	$+V_{IN}$	Input Voltage.
4	GND	Ground.
5	TRIM	Fine Trimming of Output Voltage. See Figure 4.
6	V_{OUT}	Output Voltage.
8	NOISE REDUCTION	Noise Reduction of Output Voltage. Reduces noise via external capacitor to ground.

THEORY OF OPERATION

The AD587 consists of a proprietary buried Zener diode reference, an amplifier to buffer the output, and several high stability thin-film resistors, as shown in Figure 3. This design results in a high precision monolithic 10 V output reference with initial offset of 5 mV or less. The temperature-compensation circuitry provides the device with a temperature coefficient of less than 5 ppm/°C.

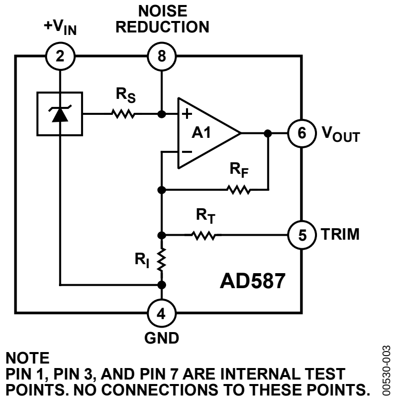


Figure 3. Functional Block Diagram

A capacitor can be added at the NOISE REDUCTION pin (Pin 8) to form a low-pass filter with R_S to reduce the noise contribution of the Zener to the circuit.

APPLYING THE AD587

The AD587 is simple to use in virtually all precision reference applications. When power is applied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 10 V output. No external components are required; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD587 requires less than 4 mA quiescent current from an operating supply of 15 V.

Fine trimming may be desired to set the output level to exactly 10.000 V (calibrated to a main system reference). System calibration may also require a reference voltage that is slightly different from 10.000 V, for example, 10.24 V for binary applications. In either case, the optional fine-trimming circuit shown in Figure 4 can offset the output by as much as 300 mV with minimal effect on other device characteristics.

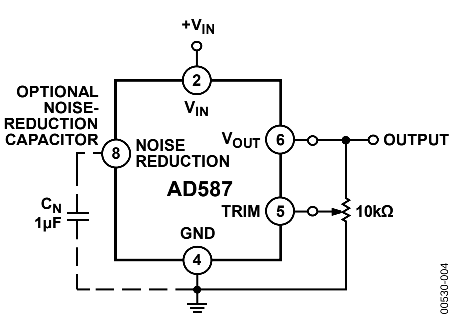


Figure 4. Optional Fine-Trimming Configuration

NOISE PERFORMANCE AND REDUCTION

Noise generated by the AD587 is typically less than 4 µV p-p over the 0.1 Hz to 10 Hz band. Noise in a 1 MHz bandwidth is approximately 200 µV p-p. The dominant source of this noise is the buried Zener, contributing approximately 100 nV/√Hz. By comparison, the contribution of the op amp is negligible. Figure 5 shows the 0.1 Hz to 10 Hz noise of a typical AD587. The noise measurement is made with a band-pass filter made of a 1-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 12.6 Hz to create a filter with a 9.922 Hz bandwidth.

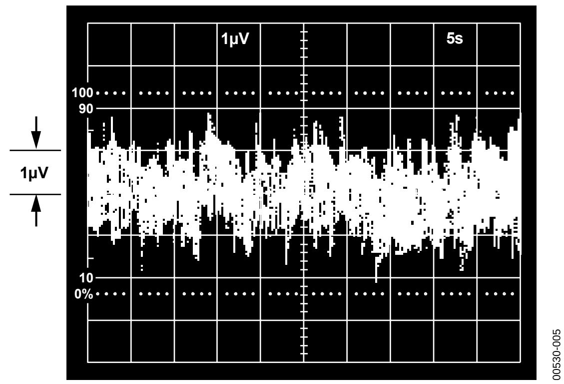


Figure 5. 0.1 Hz to 10 Hz Noise

If further noise reduction is desired, an external capacitor can be added between the NOISE REDUCTION pin and ground, as shown in Figure 4. This capacitor, combined with the 4 kΩ R_S and the Zener resistances, forms a low-pass filter on the output of the Zener cell. A 1 µF capacitor has a 3 dB point at 40 Hz and reduces the high frequency (up to 1 MHz) noise to about 160 µV p-p. Figure 6 shows the 1 MHz noise of a typical AD587, both with and without a 1 µF capacitor.

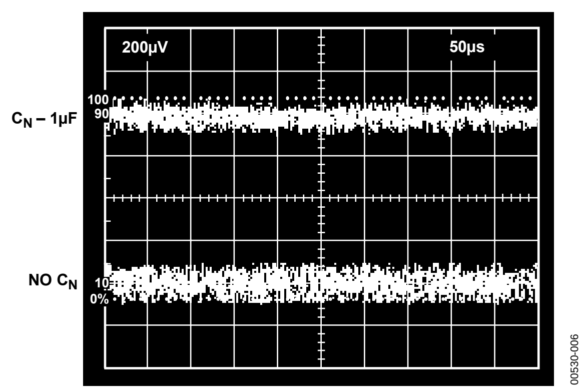


Figure 6. Effect of 1 µF Noise-Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 7, Figure 8, and Figure 9 show the turn-on characteristics of the AD587. These figures show the settling to be about 60 µs to 0.01%. Note the absence of any thermal tails when the horizontal scale is expanded to 1 ms/cm in Figure 8.

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor acts as an additional load to the current source of the internal Zener diode, resulting in a somewhat longer turn-on time. In the case of a 1 µF capacitor, the initial turn-on time is approximately 400 ms to 0.01%, as shown in Figure 9.

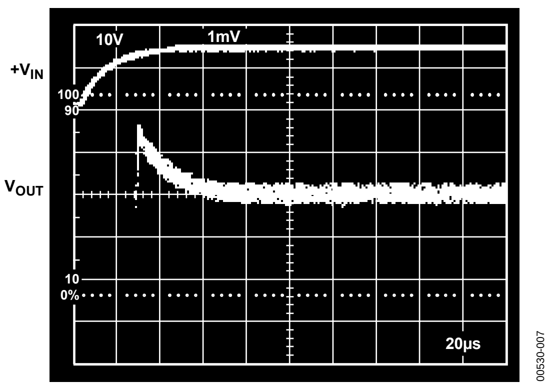


Figure 7. Electrical Turn-On

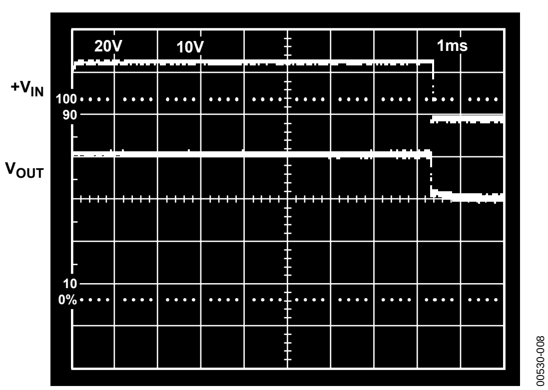


Figure 8. Extended Time Scale

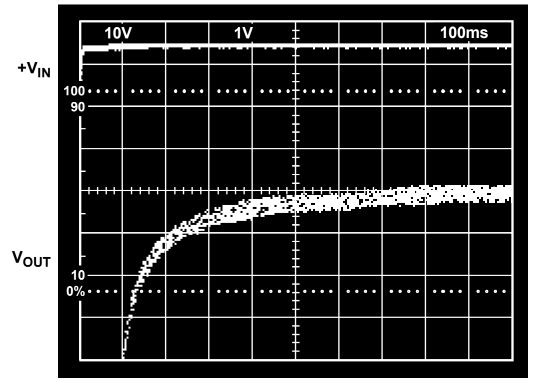


Figure 9. Turn-On with 1 µF C_N

DYNAMIC PERFORMANCE

The output buffer amplifier is designed to provide the AD587 with static and dynamic load regulation that is superior to less complete references.

Many ADCs and DACs present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 11 and Figure 12 display the characteristics of the AD587 output amplifier driving a 0 mA to 10 mA load.

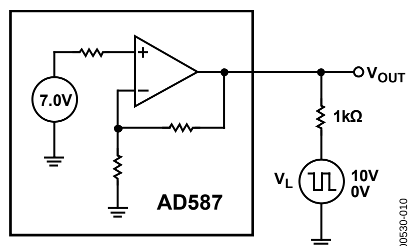


Figure 10. Transient Load Test Circuit

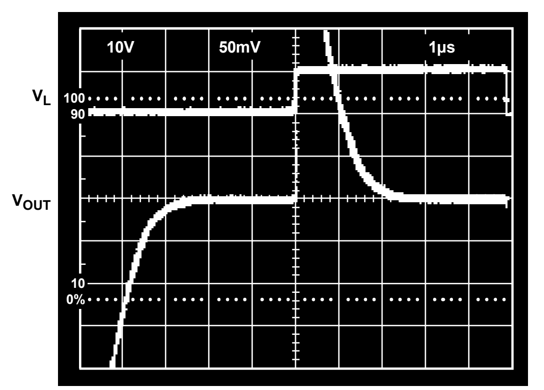


Figure 11. Large-Scale Transient Response

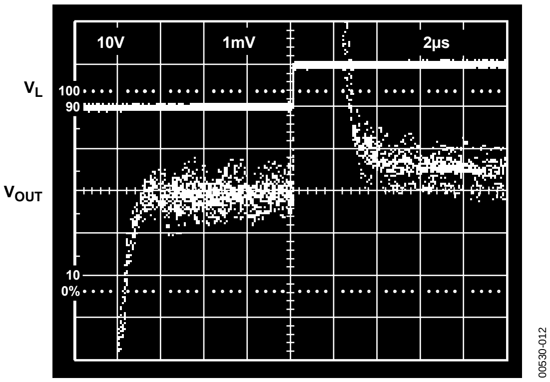


Figure 12. Fine-Scale Setting for Transient Load

In some applications, a varying load may be both resistive and capacitive in nature, or the load may be connected to the AD587 by a long capacitive cable.

Figure 14 displays the output amplifier characteristics driving a 1000 pF, 0 mA to 10 mA load.

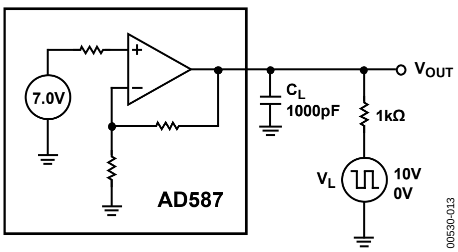


Figure 13. Capacitive Load Transient/Response Test Circuit

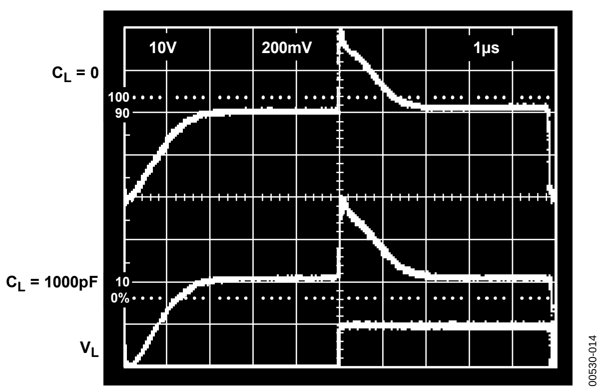


Figure 14. Output Response with Capacitive Load

LOAD REGULATION

The AD587 has excellent load regulation characteristics. Figure 15 shows that varying the load several milliamperes changes the output by only a few microvolts.

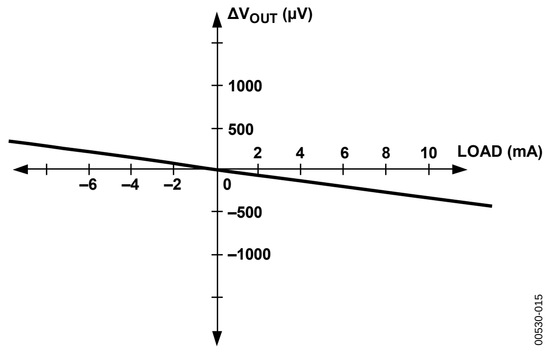


Figure 15. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The AD587 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Celsius, such as ppm/°C. However, because of nonlinearities in temperature characteristics that originated in standard Zener references (such as S-type characteristics), most manufacturers have begun to use a maximum limit error-band approach to specify devices. This technique involves the measurement of the output at three or more temperatures to specify an output voltage error band.

Each AD587J and AD587K grade unit is tested at 0°C, 25°C, and 70°C. Each AD587U grade unit is tested at −55°C, +25°C, and +125°C. This approach ensures that the variations of the output voltage that occur as the temperature changes within the specified range are contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale changes from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Figure 16. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE – mV 0 TO +70°C	–55°C TO +125°C
AD587J	14.00	
AD587K	7.00	
AD587U		9.00

00530-017

Figure 16. Maximum Output Change in Millivolts

NEGATIVE REFERENCE VOLTAGE FROM AN AD587

The AD587 can be used as shown in Figure 17 to provide a precision −10.000 V output. The $+V_{IN}$ pin is tied to at least a +3.5 V supply, the output pin is grounded, and the AD587 ground pin is connected through a resistor (R_S) to a −15 V supply. The −10 V output is taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor (R_S) so that the net current through the AD587 is between 2.5 mA and 10.0 mA (R_S should be kept below 1 kΩ). The temperature characteristics and long-term stability of the device is essentially the same as that of a unit used in the standard 10 V output configuration.

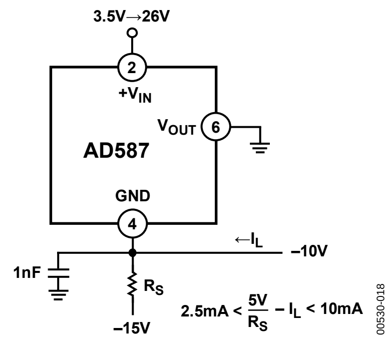


Figure 17. AD587 as a Negative 10 V Reference

APPLICATIONS INFORMATION

USING THE AD587 WITH CONVERTERS

The AD587 is an ideal reference for a variety of 8-bit, 12-bit, 14-bit, and 16-bit ADCs and DACs. Several examples follow.

10 V Reference with Multiplying CMOS DACs or ADCs

The AD587 is ideal for applications with 10-bit and 12-bit multiplying CMOS DACs. In the standard hookup, shown in Figure 18, the AD587 is paired with the AD7545 12-bit multiplying DAC and the AD711 high speed BiFET op amp. The amplifier DAC configuration produces a unipolar 0 V to −10 V output range. Bipolar output applications and other operating details can be found in the individual product data sheets.

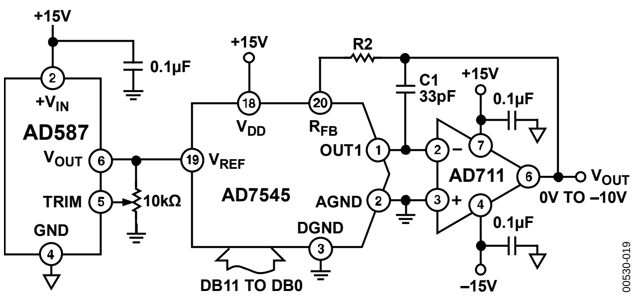


Figure 18. Low Power 12-Bit CMOS DAC Application

The AD587 can also be used as a precision reference for multiple DACs. Figure 19 shows the AD587, the AD7628 dual DAC, and the AD712 dual op amp hooked up for single-supply operation to produce 0 V to −10 V outputs. Because both DACs are on the same die and share a common reference and output op amps, the DAC outputs will exhibit similar gain temperature coefficients (TCs).

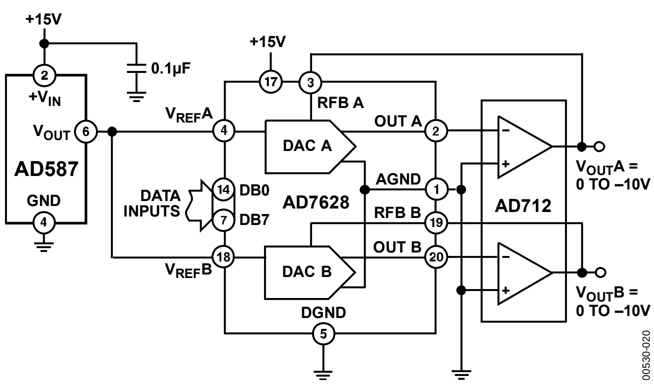


Figure 19. AD587 as a 10 V Reference for a CMOS Dual DAC

Precision Current Source

The design of the AD587 allows it to be easily configured as a current source. By choosing the control resistor (R_C) via the equation shown in Figure 20, the user can vary the load current from the quiescent current (2 mA typically) to approximately 10 mA.

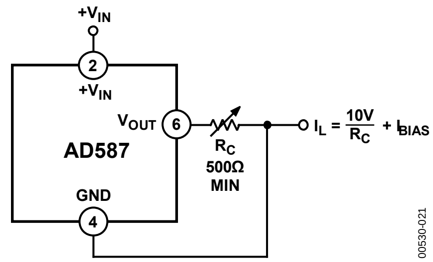


Figure 20. Precision Current Source

Precision High Current Supply

For higher currents, the AD587 can easily be connected to a power PNP or power Darlington PNP device. The circuits in Figure 21 and Figure 22 can deliver up to 4 A to the load. The 0.1 µF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results can be obtained by removing the capacitor.

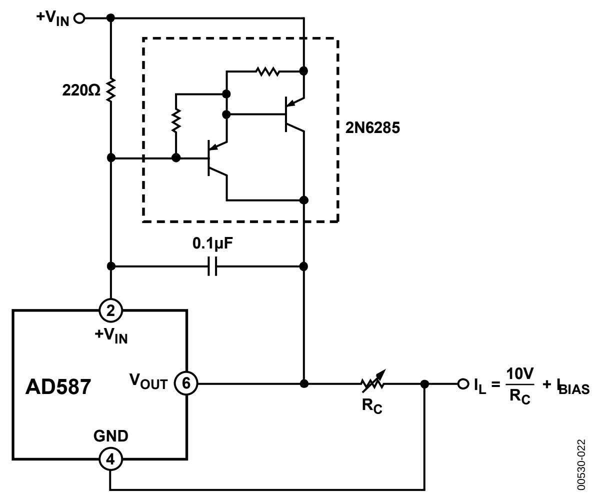


Figure 21. Precision High Current Source

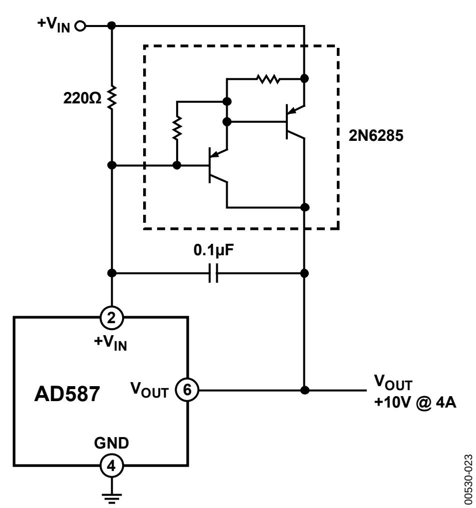
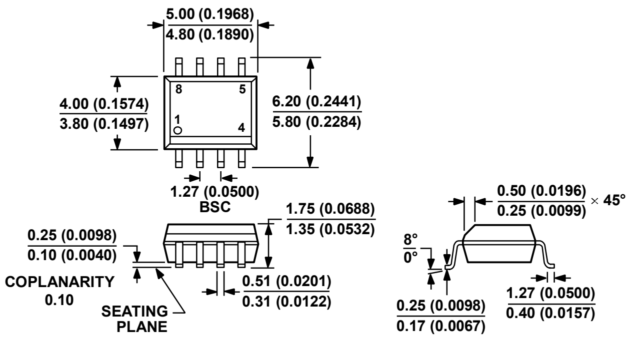


Figure 22. Precision High Current Voltage Source

OUTLINE DIMENSIONS

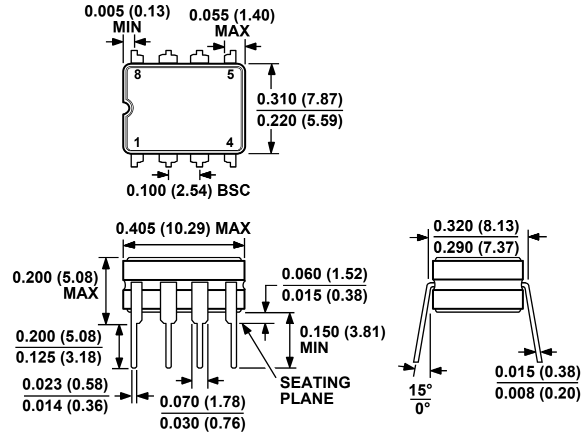


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

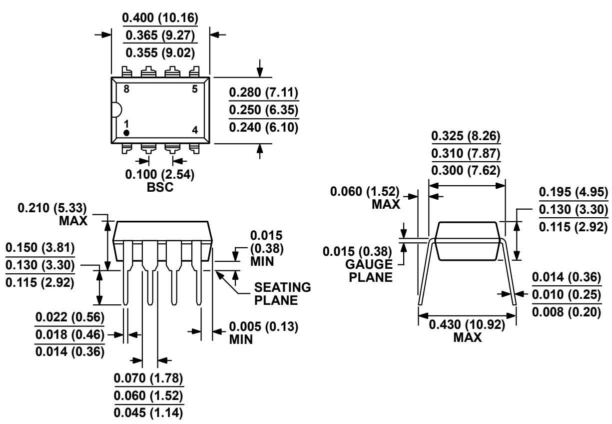
012407-A

Figure 23. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 24. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Initial Error	Temperature Coefficient	Temperature Range	Package Description	Package Option
AD587JQ	10 mV	20 ppm/°C	0°C to 70°C	8-Lead CERDIP	Q-8
AD587JR	10 mV	20 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587JR-REEL	10 mV	20 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587JR-REEL7	10 mV	20 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587JRZ[1]	10 mV	20 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587JRZ-REEL[1]	10 mV	20 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587JRZ-REEL7[1]	10 mV	20 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587JN	10 mV	20 ppm/°C	0°C to 70°C	8-Lead PDIP	N-8
AD587JNZ[1]	10 mV	20 ppm/°C	0°C to 70°C	8-Lead PDIP	N-8
AD587KR	5 mV	10 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587KR-REEL	5 mV	10 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587KR-REEL7	5 mV	10 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587KRZ[1]	5 mV	10 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587KRZ-REEL[1]	5 mV	10 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587KRZ-REEL7[1]	5 mV	10 ppm/°C	0°C to 70°C	8-Lead SOIC_N	R-8
AD587KN	5 mV	10 ppm/°C	0°C to 70°C	8-Lead PDIP	N-8
AD587KNZ[1]	5 mV	10 ppm/°C	0°C to 70°C	8-Lead PDIP	N-8
AD587UQ	5 mV	5 ppm/°C	−55°C to +125°C	8-Lead CERDIP	Q-8

[1] Z = RoHS Compliant Part.

C00530-0-9/07(H)