SELECTION GUIDE

Part Number	Ambient Temperature	Package	Packing
A5932GLPTR-T	-40 to 105C	24L eTSSOP	4000 pieces per 13-in. reel
A5932GESSR-T	-40 to 105C	24L eQFN	6000 pieces per 13-in. reel

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}				50	V
Logic Input Voltage Range (SPD, BRAKE, DIR)	V_{IN}		-.3		6	V
Logic Output – FG, RD, nFAULT	Vo	FG (I<5mA)			6	V
LSS	V_{LSS}	DC	-500		500	mV
		Tw <500ns	-1		4	V
Output Voltage	V_{OUT}	SA,SB,SC	-2		V_{BB}+2	V
CTAP	V_{CTAP}	DC	-.6		Vbb+.6	V
		Tw <500ns	-2		V_{BB}+2	
GHx	V_{GH}		SX-.3		V_{CP}+.3	V
GLx	V_{GL}		LGS-.3		8.5	V
VCP			V_{BB}-.3		V_{BB}+8	V
CP1			-.3		V_{BB}+.3	V
CP2			V_{BB}-.3		V_{CP}+.3	V
ISET			-.3		5.5	V
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-55		150	°C
Operating Temperature Range	Ta		-40		105	°C
Package Thermal Resistance						
LP	R_{θ}	2 sided PCB 1 in^2 Copper		36		°C/W
ES				45		°C/W

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TERMINAL LIST

LP	QFN	Pin Name	Pin Description
1	16	CP2	Charge Pump
2	17	CP1	Charge Pump
3	18	BRAKE	Logic Input
4	19	VREF	Logic Supply Output
5	20	SPD	Speed Input
6	21	DIR	Logic Output
7	22	RD	Speed Output
8	23	FG	Speed Output
9	24	nFAULT	Logic Output
10	1	ISET	Analog Input
11	2	GND	Ground
12	3	GLA	Gate Drive Output
13	4	GLB	Gate Drive Output
14	5	GLC	Gate Drive Output
15	6	LSS	Low Side Source
16	7	SA	Motor Output
17	8	GHA	Gate Drive Output
18	9	SB	Motor Output
19	10	GHB	Gate Drive Output
20	11	SC	Motor Output
21	12	GHC	Gate Drive Output
22	13	CTAP	Motor Common
23	14	VCP	Charge Pump
24	15	VBB	Power Supply

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ELECTRICAL CHARACTERISTICS (unless noted otherwise)

G version: valid for TA = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Load Supply Voltage Range	VBB	Driving			V_{BBOV}	V
		Operating			50	V
VBB Supply Current	I_{BB}	I_{VREF}=0mA		11	15	mA
		Standby Mode		5	20	µA
VREF	V_{REF}	I_{OUT}=20mA	2.75	2.86	2.95	V
VREF Current Limit	V_{REFOCL}	V_{REF}=0V	30	50	80	mA
Charge Pump	V_{CP}	VBB=8V, Relative To V_{BB}	6.5	7	7.5	V
		VBB=5.5V	tbd	5		V
Gate Drive						
High Side Gate Drive Output	V_{GH}	VBB=8V	6.5	7		V
Low Side Gate Drive Output	V_{GL}	VBB=8V	6.5	7		V
Gate Drive Source Current	I_{SO}	Relative to target, R_{ISET}=15K to 150K	-25		25	%
Gate Drive Sink Current	I_{SI}	Relative to target, R_{ISET}=15K to 150K	-25		25	%
Gate Drive Source Current	I_{SO}	R_{ISET}=GND		32		mA
Gate Drive Sink Current	I_{SI}	R_{ISET}=15K		60		mA
Motor Drive						
PWM Duty On Threshold	DC_{ON}	Relative to Target	.5		.5	%
PWM Duty OFF Threshold	DC_{OFF}	Relative to Target	.5		.5	%
PWM Input Frequency Range	F_{PWM}		.1		100	kHz
SPD Standby Threshold (Analog)	SPDTH		.5	.75	1	V
SPD On threshold	SPD_{ON}	DCON = 10.2%	220	250	280	mV
SPD Max	SPD_{MAX}			2.5		V
SPD ADC Resolution				4.89		mV
SPD ADC Accuracy		SPD = .2V to 2.5V		+/-6		LSB
Speed Setpoint	F_{SPD}	PWM Mode	-4		4	%
Dead Time	t_{DT}	Code=10		480		ns
Motor PWM Frequency	f_{PWM}		23.67	24.4	25.15	kHz

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization
2. Gate Drive Output characteristics are valid from 5.5V to VBBOV

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ELECTRICAL CHARACTERISTICS (unless noted otherwise)

G version: valid for TA = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Protection						
VBB UVLO	VBB_{UVLO}	V_{BB} rising		4.75	4.95	V
VBB UVLO HYS	VBB_{HYS}		200	300	450	mV
VBB Overvoltage Threshold	VBB_{OV}	Relative to target	-4		4	%
VBB Overvoltage Hystersis	VBB_{OVHYS}			2		V
OverCurrent Threshold	V_{OCL}		240	250	260	mV
VREF UVLO	$VREF_{UVLO}$	falling		2.6		V
VCP UVLO	VCP_{UVLO}	falling		3.9		V
Lock Timing	T_{LOCK}	Relative to Target	-4		4	%
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing	150	170	190	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = T_{JTSD} - ΔT_J		20		°C
Logic/Input Output/I2C						
Input Current (SPD,FG)	I_{IN}	Vin=0 to 5.[illegible]V	-5	<1	5	uA
Input Current (BRK, DIR)	I_{IN}	Vin=[illegible]		50		uA
Logic Input Low Level	V_{IL}		0		.8	V
Logic Input High Level	V_{IH}		2		5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Sat Voltage	V_{SAT}	I=5mA			.3	V
FG,RD, nFAULT Output Leakage	I_{FG}	V=5V			1	uA
SCL Clock Frequency	fCLK		3	–	400	kHz
I2C timing						
Bus Free Time Between Stop/Start	tBUF		1.3	–	–	µs
Hold Time Start Condition	tHD:STA		0.6	–	–	µs
Setup Time for Start Condition	tSU:STA		0.6	–	–	µs
SCL Low Time	tLOW		1.3	–	–	µs
SCL High Time	tHIGH		0.6	–	–	µs
Data Setup Time	tSU:DAT		100	–	–	ns
Data Hold Time	tHD:DAT		0	–	900	ns
Setup Time for Stop Condition	tSU:STO		0.6	–	–	µs

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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Functional Description

The A5932 targets high speed server fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan is controlled by variable duty cycle PWM input.

The PWM input duty is measured and converted to a 9bit number. This 9 bit "demand" is applied to a pwm generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

Protection features include lock detection with restart, motor output short circuit, supply undervoltage monitor and thermal shutdown.

Standby mode can be achieved by holding SPD pin low for longer than the programmed Lock off-time. In specific speed curve options, the motor will never turn off with 0% duty cycle applied. In this type of configuration, standby mode is not available.

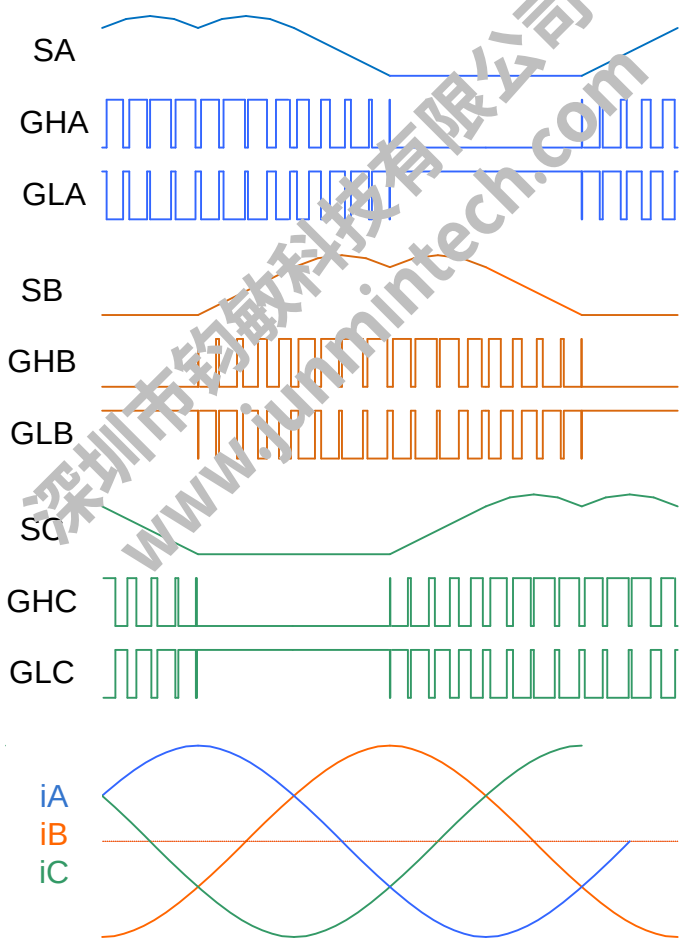

Figure 1: Sinusoidal PWM (DIR=HI)

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Functional Description

VREF. Voltage reference (2.8V) to power internal digital logic and analog circuitry. V_{REF} can be used to power external circuitry with up to 20mA bias current if desired. Stabilize with .1uF or greater ceramic capacitor.

FG. Open drain output provides speed information to the system. The open drain output can be pulled up to V_{REF} or external 3.3 or 5V supply.

RD.
Open drain output, Logic high indicates a rotor fault condition as defined by EEPROM variables. RD function can be disabled via EEPROM. When function is disabled RD pin low to high transition indicates end of open loop starting sequence.

BRAKE. Active High signal turns on all low sides for braking function. Brake Function will prevent IC from entering standby mode. Brake function overrides Speed control input. Care should be taken to avoid stress on the MOSFET when braking while motor is running. With braking the current will be limited by V_{BEMF}/R_{MOTOR}.

DIR. Logic Input to control motor direction**.** For logic high, motor phases are ordered A→B→C. For logic low A→C→B. If Direction input is changed while motor running, motor will coast for a duration defined by T_Coast. After this delay, motor will then attempt to restart in desired direction.

ISET. A resistor (R_{ISET}) to GND sets the magnitude of gate current. The sink and source current ratios are fixed at approximately 2:1. Resistor value RISET should be in the range 15K to 150K.

The formula for gate drive current is as follows:

I_{GATE_SRC}(mA) = 1.9 + 900/R_{ISET} (Kohms)
I_{GATE_SNK}(mA) = 3.5 + 1700/R_{ISET} (Kohms)

If pin ISET is connected to GND, the circuit will default to a level equivalent to 30K. If ISET is open, the motor outputs will be disabled.

CTAP. This analog input is an optional connection for motor common (Wye motors). If not used, as in case of Delta wound motor, then pin must be left open circuit. Speed

SPD. Speed Demand input pin. Choice of analog voltage control or PWM duty control is determined by EEPROM selection.

Duty cycle control. The PWM frequency must be in the range 100Hz to100kHz. Duty cycle resolution is 9Bit.

Analog control. Voltage applied will increase speed demand. An internal 9 bit A/D converter will translate the input to a speed demand.

Standby Mode. A low power mode is activated if SPD pin is held low. Standby Mode will turn off all circuitry including charge pump and VREF. Upon power up, the A5932 will immediately wake up. If SPD remains low for the programmed lock time, standby mode will be activated. Standby mode can be disabled via EEPROM bit.

Lock Detect. A logic circuit monitors the motor position to determine if motor is running as expected. If a fault is detected, the motor drive will be disabled for T_{LOCK} before an auto-restart is attempted.

Current Limit. Maximum load current can be set by choice of external sense resistor connected between LSS terminal and GND.

I_{LIM} = 250mV/R_{SENSE}

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nFAULT. The following signals will bring output nFAULT low:

1) VBB Undervoltage
2) Thermal Shutdown
3) Charge Pump UVLO
4) VBB Overvoltage
5) Output Vds Fault (OCP)
6) Loss of synchronization

Fault	**Fault Action**	**Latched**	**Readback Reg[Bit]**
Vbb Undervoltage	Disable Outputs	N	147[8]
TSD	Disable Outputs	N	147[6]
Charge Pump	Disable Outputs	N	147[7]
Vbb Overvoltage	Disable Outputs or disabled outputs and set Lock detect	N	147[9]
VDS Fault	Choose by EEPROM bit OCPOPT	If OCPOP=1	147[5:0]
Loss of Sync	Set Lock detect timeout	N	148[6:0]

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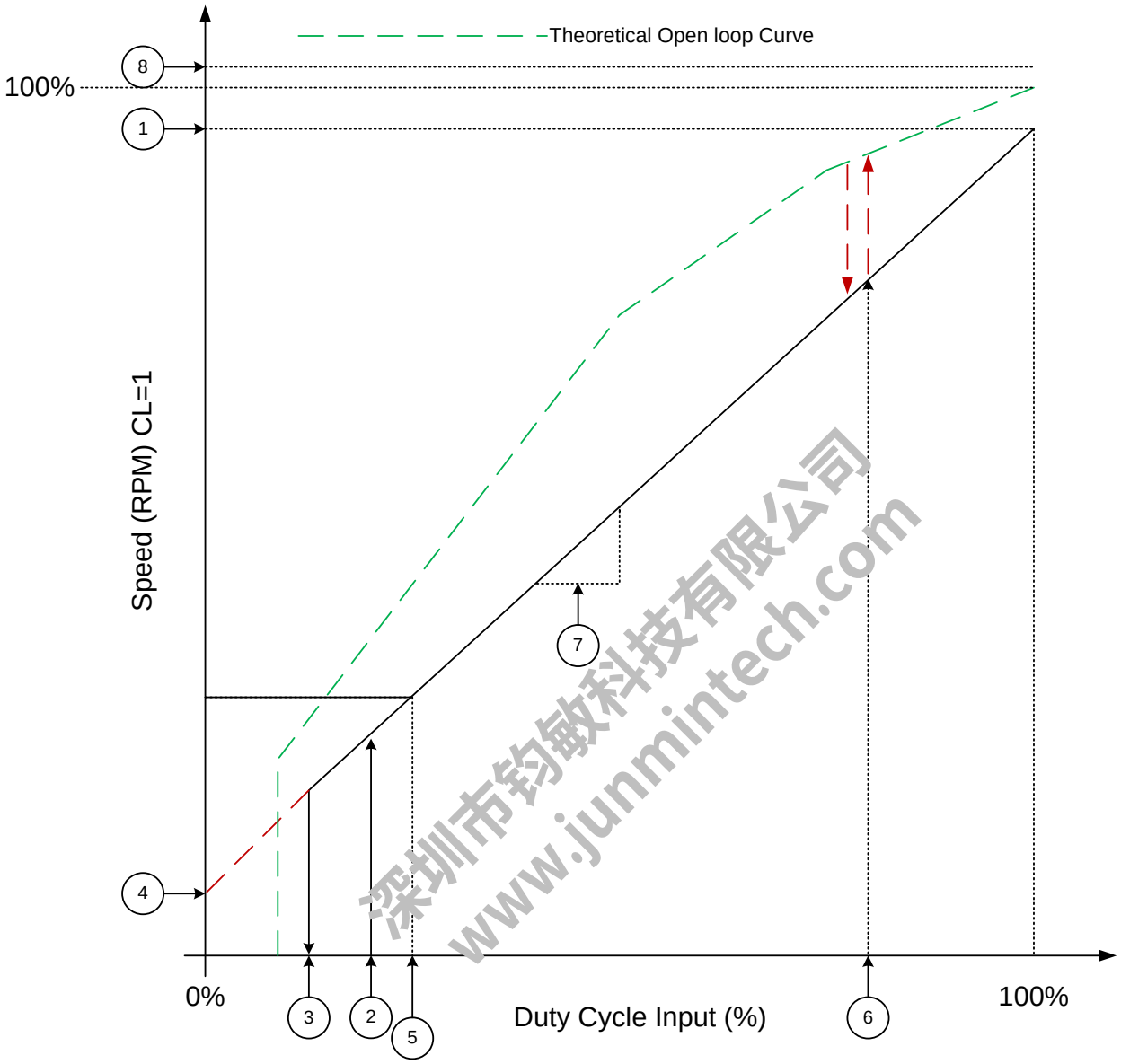
Speed Control Options.



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1. Maximum Speed (calculated from Slope of line AND Offset)
2. Duty On (DCON/511)
3. Duty Off (DCOFF/511
4. MINSPD
5. Min Duty Clamp
6. Max Duty Threshold and Hystersis
7. Slope (based on SPDSLP variable)
8. OPNLPMAX

Figure 1) Speed Curve Options

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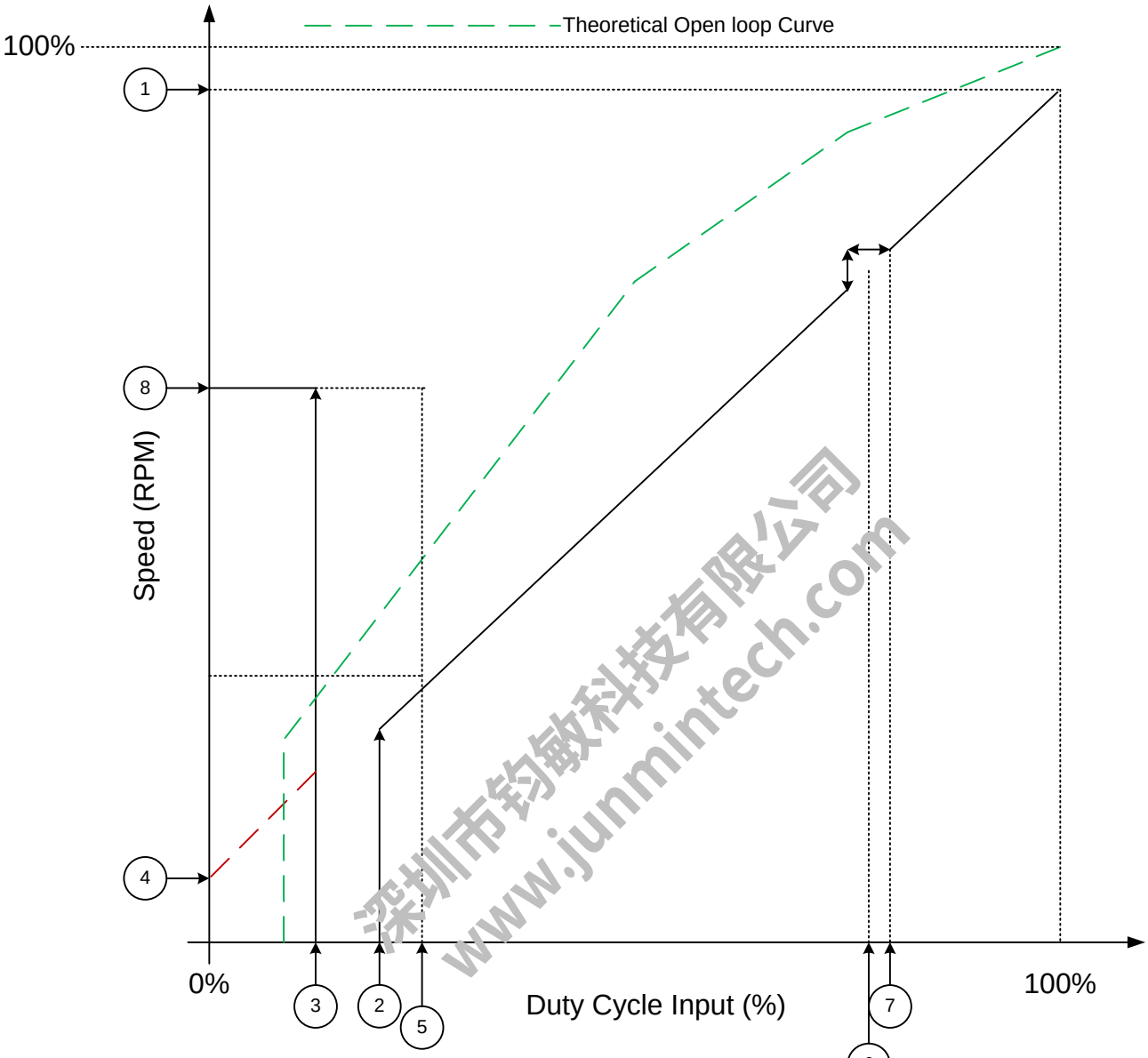

1 Maximum Speed (calculated from Slope of line AND Offset)

2 DConoff1 (hys=.8%)

3 DConoff2 (hys=.8%)

4 MINSPD

5 MAXOFFDTY

6 RESDTY

7 RESWID

8 REVOPT

Figure 2) Speed Curve Options - 2

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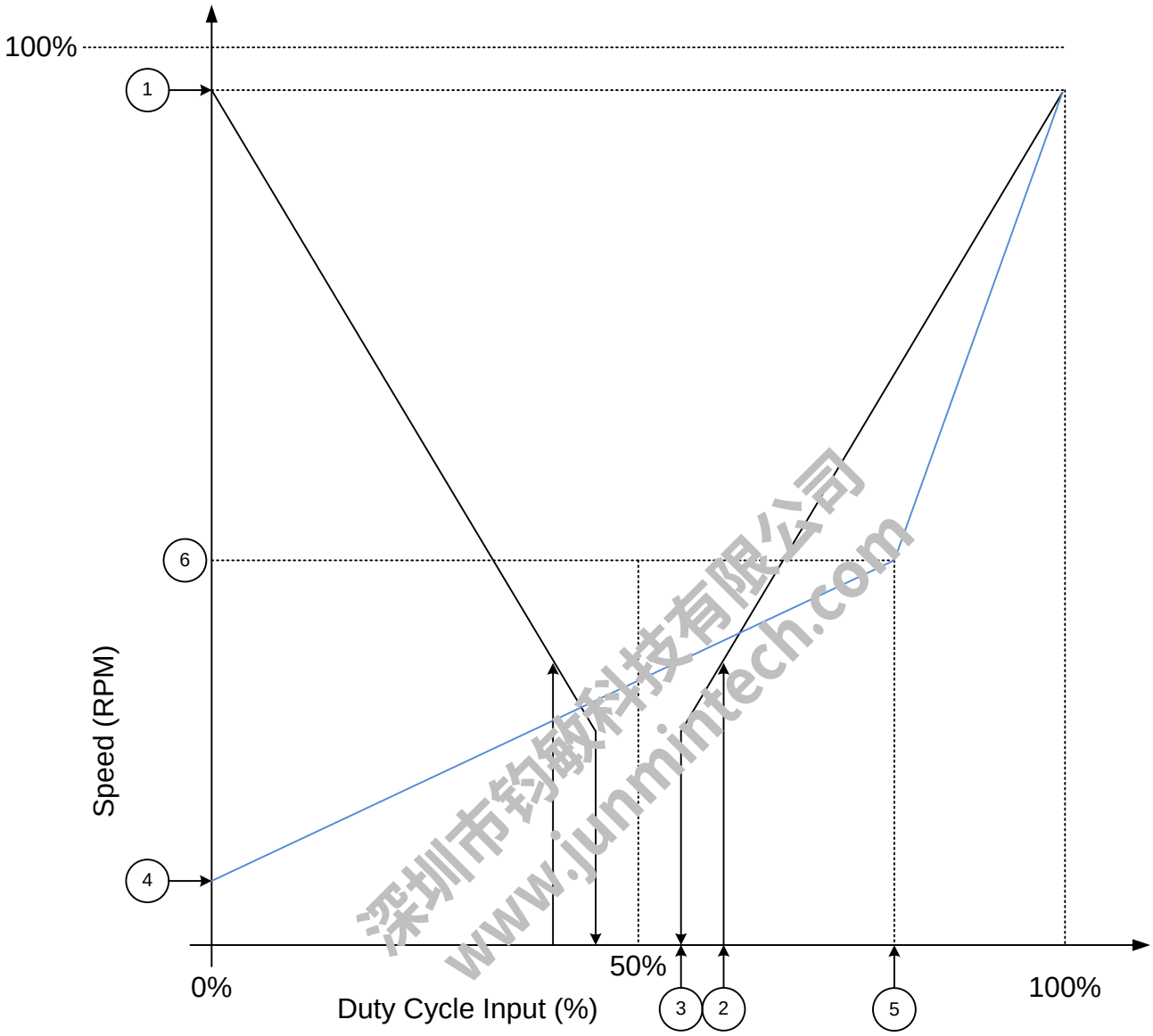

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1 Maximum Speed (calculated from Slope of line AND Offset)

2 DCON

3 DCOFF

4 MINSPD

5 SLPSWDTY

6 SLPSWRPM

Figure 3) Speed Curve Options -3

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Speed Curve Parameters (continued)
Refer to Figure 1-3 for below items.

Minimum Speed Set point.
The minimum speed is defined by the value stored in EEPROM variable MINSPD. The resolution is 1RPM.

MINSPD (RPM) = 0..4095

Maximum Speed Set point.
The A5932 calculates the maximum speed based on line equation y=mx + B. The maximum speed is defined as the speed with input duty = 100%.

The desired maximum speed is used to set the EEPROM variable SPDSLP.

SPDSLP = 64*(Maximum Speed (Rpm) – MINSPD)/511

Example: Max Speed = 25000, Min Speed = 3000.

SPDSLP = 64*22000/511 = 2755

Where SPDSLP = 0..16383

Motor Speed (RPM) = Slope*DutyIN + MINSPD.

Where Slope = SPDSLP*511/64 and DutyIN expressed in %.

Duty In Enable Threshold.
EEPROM variable DCON defines the input duty signal that enables the drive. DCON is a 8 bit number with resolution of .2%, which results in a max setting of 49.9%.

Duty On (%) = 100*DCON/511

If DCON is set to “0”, motor will turn on with 0% duty cycle input.

Duty In Disable Threshold.
EEPROM variable DCOFF defines the input duty signal that disables the drive. DCOFF is an 8 bit number with resolution of .2%, which results in a max setting of 49.9%.

Duty Off(%) = DCOFF/511
DCOFF should always be set to a lower number than DCON.

ON/Off Control Option.
If bit ONOFFCNTRL bit is set to “1” then the motor will runs off if duty is between the values set by DCON & DCOFF. A fixed value of .8% hysteresis is applied. In this option, if the duty is below DCOFF, then the motor will be enabled with a PWM level set by variable MAXDTYOFF. (see figure 2)

Additionally, if duty is below DCOFF, the motor direction can be made to be reverse if REVOPT is set to “1”.

Duty Cycle Invert.
To create mirror image of speed curve, set Duty cycle invert bit to “1”.

Minimum Duty Clamp.
Minimum speed can be clamped to a value to allow motor to run at defined low level speed. This is achieved by ignoring the duty cycle input if below the programmed MINDTY level.

Min Duty Clamp (%) = 100*MINDTY/511

Therefore the minimum speed will be defined by:

MinSpeedClamp(RPM) = Slope*MinDutyClamp+MINSPD

Setting MINDTY to 0 disables the function.

MINDTY=0..255

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Maximum Duty Clamp.
EEPROM variable DTYMAX defines a duty level at which the motor will change operation from closed loop curve. The change of operation would depend on MAXDTYOPT setting. If MAXDTYOP = 0, open loop operation will result, if MAXDTYOPT = 1 then operation will remain closed loop however the speed will be clamped at the value calculated by DTYMAX level.

4 bits are used for this setting at resolution of 1.6% to cover the range 76.5% to 100%.

Maximum Duty (%) = 100*(511-MAXDTY*8)/511

MAXDTY = 0..15; If MAXDTY=0 then function is disabled.

Hysteresis is needed to prevent motor from going back and forth between open and closed loop mode.

MAXDTYHYS = 0...15

Hys(%) = (MAXDTYHYS+1)*.4

50% Duty Option.
If bit DIR50 is set to 1, the motor direction can be controlled by duty cycle level. (see figure 3)
For this setting, the motor enable and disable functions will be set by:

DCONnew = 50% +/- DCON
DCOFFnew = 50% +/-DCOFF

Since the duty cycle reference changes from 100% scale to 50% scale. The slope of the curve is now 2X compared to normal (DIR50=0) setting. When duty changes to switch direction, the motor will coast for time programmed via TCOAST variable before attempting to startup in opposite direction. Care should be taken to minimize stress on the MOSFETS when switching direction.

Dual Slope Option. (see figure 3)
Two different slopes can be selected by setting variable SLPSWDTY greater than 0.

Slope2 = (MAXSPEED-SLPSWRPM)/(100%-SLPSWDTY)

Slope1 = (SLPSWRPM – MINSPEED)/SLPSWDTY

Resonance Option. (see figure 3)
To avoid any issues with mechanical resonance at a particular speed band, variable RESWID & RESDTY are provided to allow skipping over a defined RPM and.

RESDTY: defines duty cycle that is center of band
RESWID: defines width of band relative to center duty value

Open Loop Maximum Limit
When the speed curve is set to open loop mode it is possible to limit the speed to prevent fan speed overshoot. Rpm is monitored and the demand will be clamped at level that results in max limit.

OPNLPMAX variable has no effect in closed loop mode.

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EEPROM MAP

Note: refer to application note and user interface for additional detail.

I2C REG	EE ADDR	Bits	Name	Description	Default Setting	Default Value (decimal)
64	0	15:0	Dev1	Allegro Reserved	n/a	n/a
65	1	15:0	Dev1	Allegro Reserved	n/a	n/a
66	2	15:0	Dev1	Allegro Reserved	n/a	n/a
67	3	15:0	Dev1	Allegro Reserved	n/a	n/a
68	4	15:0	Dev1	Allegro Reserved	n/a	n/a
69	5	15:0	Dev1	Allegro Reserved	n/a	n/a
70	6	15:0	Dev1	Allegro Reserved	n/a	n/a
71	7	15:0	Dev1	Allegro Reserved	n/a	n/a
72	8	3:0	MAXDTYCLP	Range= 100% to 76.5%, LSB=1.6%	0	0
		7:4	MAXDTYHYS	Range= 0 to 5.9%, LSB=.4%	0	0
		14:8	MINDTYCLP	Range= Range=0 to 49.9% LSB=.78%	0	0
73	9	8:0	STRTDMD	LSB=VBBRNG/511	.8V	17
		15:9	DMDPOST	Range=0 to 100%, LSB=.8%	79.5%	202
74	10	7:0	ALIGNT	Range=0 to 20.4S LSB=100ms	.5S	63
		15:8	ASLOPE	Range= 160ms to 40S	.16S	255
75	11	7:0	STRTF	Range=0 to 15.94Hz LSB=.0625mHz	.19Hz	3
		15:8	ACCEL	Range= 0 to 99.6 Hz/S LSB=.78	41.8Hz	107
76	12	7:0	ACCELT	Range=0 to 10.2S LSB=40ms	480ms	12
		15:8	MAXOFFDTY	Range=100% to 76.5% LSB=.4%	100%	0
77	13	3:0	DMDRMPAL	Range=3.8 to 63.8ms/count, LSB=3.8	23.8ms/count	5
		7:4	DMDRMPAH	Range=3.8 to 63.8ms/count, LSB=3.8	15.8 ms/count	3
		11:8	DMDRMPDL	Range=3.8 to 63.8ms/count, LSB=3.8	27.8 ms/count	6
		15:12	DMDRMPDH	Range=3.8 to 63.8ms/count, LSB=3.8	27.8 ms/count	6
78	14	8:0	RESDTY	Range = 0 to 100%, LSB=.2%	Disabled	0
			RESWID	Range = 0 to 50%, LSB=.4%	n/a	0
79	15	7:0	MAXSPD	Maximum Electrical Frequency	509hz	24
		15:8	TLOCK	0 to 25.5S	5S	50
80	16	7:0	RDLOW	Range=0 to 4095, LSB=16RPM	0	0
		15:8	RDHIGH	Range=0 to 4095, LSB=16RPM	0	0
81	17	7:0	RDBLK	Range=0 to 25.5S, LSB=100ms	0	0
		11:8	RDDLY	Range=0 to 15S, LSB=1S	0	0
		12	Unused			
		13	DITHDT	0=1.28ms 1=5.12ms/step	0	0
		14	DITHSTP	0=16steps 1=32 steps	0	0
		15	DITHENB	1=Enable	disabled	0
82	18	11:0	PHASLP	Calculated Slope for Linear Phase Advance	12.7deg	98
		15:12	SOWLIN	Window Width With Linear Phase Advance	28.2deg	15
83	19	0	PCDLY	Post Coast delay 0=100ms 1=500ms	500ms	1
		1	STBYDIS	Standby Mode 0=Enable 1=Disable	1	1
		3:2	PWMF	Motor PWM Selection	24/48kHz	2
		5:4	BEMFFILT	Bemf comp filter	4us	0
		6	TCENB	Temperature Compensation 0: Off 1:On	0	0
		8:7	WINDM	Windmill Option	0	0
		12:9	SPDCLP	Minimum clamp is speed control mode	4.6%	2
		14:13	PHARNG	0: >32krpm 1:16k-32k 2: 8k-16k 3:<8k	8k-16k	2
		15	OCLOPT	0=Cycle by cycle 1: Reduce demand	1	1

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EEPROM MAP (Continued)

I2C REG	EE ADDR	Bits	Name	Description	Default Setting	Default Value (decimal)
84	20	0	CL	Speed Control Mode 0=OpenLoop 1=Closed	Enabled	1
		1	PHA	Running Mode 0=Auto 1=Linear Phase Advance	0	0
		2	RDOPT	Rd Function Mode select	0	0
		3	SPDSEL	Speed Control Select 0=PWM Duty, 1=Analog	0	0
		6:4	PP	Pole Pair = PP+1	2pp	1
		7	NOCOAST	1=NOCOAST, 0=Coast	Nocoast	1
		8	ALIGNMODE	0=Align 1=One Cycle	Align	0
		9	QCKSTRT	0=Disable 1= Enable	disable	0
		10	OVPOPT	0=Disable 1:lock detect	T_{LOCK}	1
		11	FGSTRT	0=FG disabled during Startup, 1=FG Enabled	0	0
		13:12	BEMFHYS	Bemf Hys Level for Startup	40mV	1
		14	SOWAUTO	Initial Value of Window	21°	1
		15	OCPOPT	0=Reset after T_{LOCK} 1= After PWM on/off	T_{LOCK}	0
85	21	7:0	KP	Closed Loop	16	16
		15:8	KI	Closed Loop	2	2
86	22	7:0	SLPSWDTY	Duty at which slope changes	Disabled	0
		14:8	TRAPSWDTY	Duty to switch to trap	Disabled	0
		15	TRAPENB	1=Enable	Disabled	0
87	23	14:0	SLPSWRPM	Range 0 to 16384, LSB=1rpm	Disabled	0
88	24	13:0	SPDSLP2	Calculated Slope	0	0
		15:14	Unused			
89	25	0	DUTYINV	0=Normal 1=Invert	0	0
		1	MAXDTYOPT	0=Run in Open Loop, 1= Run at MAXDTYCLP	0	0
		2	ONOFFCNTL	0=Normal hysteretic on/off , 1= Motor Off between DC_On & DC_Off	0	0
		3	DIR50	1=enable direction change based on 50% duty	0	0
		4	REVOPT	1= reverse when duty < dc_off & ONOFFCNTL=1	0	0
		5	BRKOFF	0=Coast 1=Brake when PWM off state after t_{COAST}	0	0
		6	n/a	Set to 0	0	0
		8:7	PIOS	0=1x 1=2x 2=4x 4=8x	0	0
90	26	7:0	TCOAST	Coast time for brake or dir change	3S	30
		15:8	OPNLPMAX	Max speed limit for open loop mode	30208	118
91	27	11:0	MINSPD	Minimum Speed (y intercept)	1000	1000
		13:12	OVPSEL	18/28/38/48V	28	1
		14	VBBRNG	0=24V 1=48V	24	0
92	28	13:0	SPDSLP1	Calculated Slope of Speed Curve	1378	1378
93	29	7:0	DCON	Range=0 to 49.9% LSB=.2%	10%	97
		15:8	DCOFF	Range=0 to 49.9% LSB=.2%	7.4%	79
94	30	3:0	DT	Deadtime	480nS	10
		4	VDSTH	OCP VDS Threshold 0=1V 1=2V	1V	0
		5	OCPDIS	OCP Disable 0=Enabled 1=Disabled	Enabled	0
		7:6	n/a	Allegro Reserved	n/a	0
		15:8	n/a	Allegro Reserved	n/a	89
95	31	15:0	n/a	Allegro Reserved	n/a	n/a

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Serial Port Control Option

Normally the IC is controlled by duty cycle input and uses the EEPROM data that is stored to create the speed curve profile (as show in Figure xx). However, it is possible to use direct serial port control to avoid programming EEPROM. When using direct control, the input duty cycle command is replaced by writing to a 9 bit number to register 165.

Example:
REGADDR[data]: (in decimal)
165[511] → Duty=100%
165[102] → Duty=102/511=20%

Upon power up, IC defaults to duty cycle input mode. To use serial port mode, the internal registers should be programmed before turning the part on. The sequence to use serial port mode is:

1) Drive FG & SPD pins low**
2) Power up IC
3) Program registers for parameter setting that correspond to each of the EEPROM memory locations.
    a. REGADDR = 64 + EEPROM ADDR.
    b. Program register addresses 65 to 84 corresponding to EEPROM addresses 1 to 20
    c. It may be helpful to use the GUI text file to help define the register data for each of the EEPROM addresses.
4) Write to register 165 to start motor

**Note: If SPD is not driven low before power up, motor will try to start immediately as the default high value will demand 100% on signal.

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Serial Port.
The A5931 uses standard fast mode I2C serial port format to program the EEPROM or to control the IC speed serially. The SPD pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running the FG may pull then data line low while trying to initialize into serial port mode. Once an I2C command is sent the SPD input is ignored, and the motor will turn off as if a PWM duty command of 0% was sent.

The 5931 7 bit slave address is 0x55).

I²C Timing Diagrams.

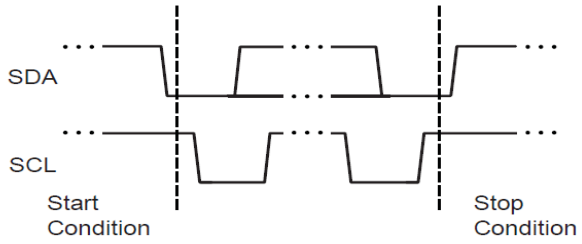

Figure 5. Start and Stop conditions

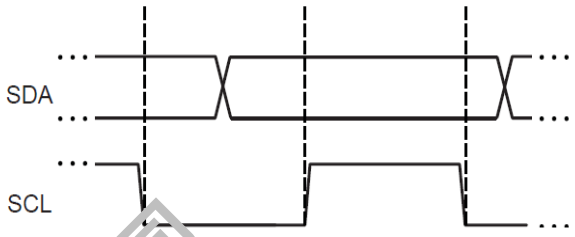

Figure 6: Clock and data bit synchronization

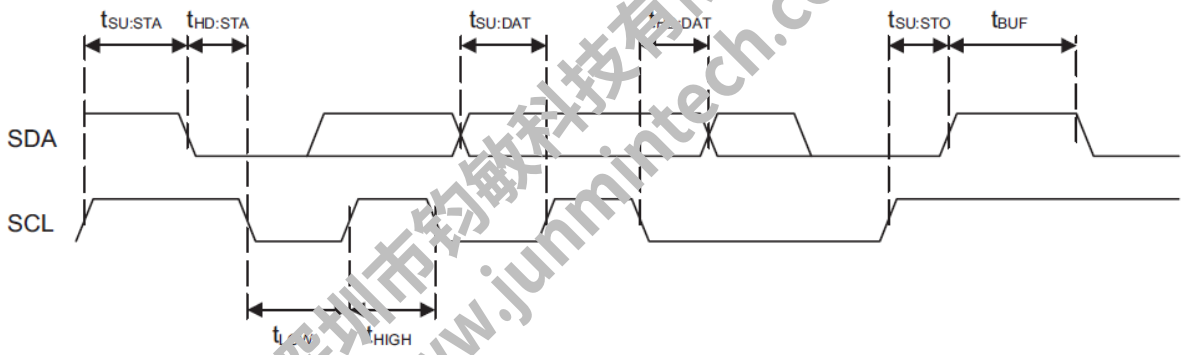

Figure 7: I2C™-Compatible Timing Requirements

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Write command:

1) Start Condition
2) 7 bit I2C Slave Address (Device ID) 1010101, R/W Bit = 0
3) Internal Register Address
4) 2 data bytes, MSB first
5) Stop Condition

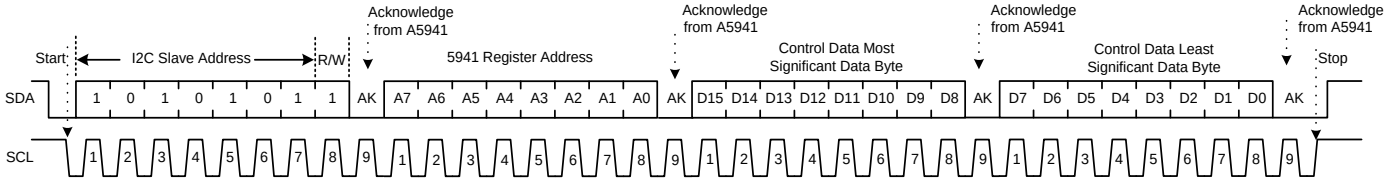

Figure 8: Write Command

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Read command: Two Step Process

1) Start Condition
2) 7 bit I2C Slave Address (Device ID) 1010101, R/W Bit = 0
3) Internal Register Address to be read
4) Stop Condition
5) Start Condition
6) 7 bit I2C Slave Address (Device ID) 1010101, R/W Bit = 1
7) Read 2 data bytes
8) Stop Condition

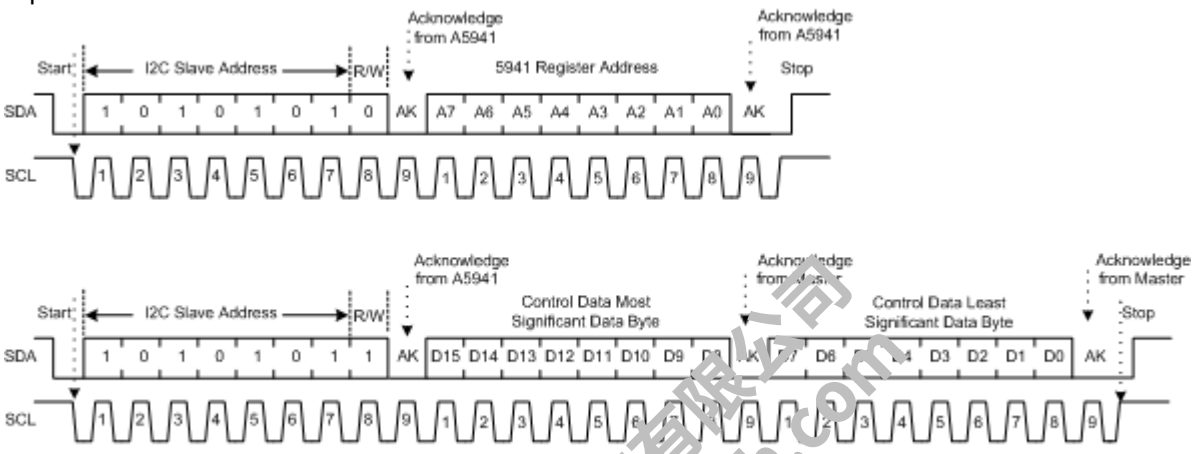

Figure 9: Read Command

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Programming EEPROM. The A5931 contains 24words of 16 bit length. The EEPROM is controlled with the following i2c registers. Refer to application note for EEPROM definition.

EEPROM Control – Register **161**: Used to control programming of EEPROM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEProm Voltage required for Writing or Erasing
1	ER	Sets Mode to Erase
2	WR	Sets Mode to Write
3	RD	Sets Mode to Read
15:4	n/a	Do not use, always set to Zero during programming process

EEPROM Address– Register **162**: Used to set the EEPROM address to be altered

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
0	eeADDRESS	Used to specify EEPROM address to be changed. There are 20 addresses. Do not change address 0 or 19 as these are factory controlled
15:5	n/a	Do not use always set to Zero during programming process

EEPROM DataIn – Register **163**: Used to set the EEPROM new data to be programmed

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed.

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EEPROM DataOUT – Register 164: Used for read operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAout															

Bit	Name	Description
15:0	eeDATAout	Used to readback EEPROM data from address defined in register 162

There are 3 basic commands, Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 10ms per word.
Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (hex=0x0105)

1) Erase the word

   I2c Write REGADDR[Data] ; comment

   a. 162[5] ; set EEPROM address to erase
   b. 163[0] ; set 0000 as Data In
   c. 161[3] ; set control to Erase and Voltage High
   d. Wait 15ms ; requires 15ms High Voltage Pulse to Write
   e. 161[0] ; clear Voltage

2) Write the new data

   a. 162[5] ; set EEPROM address to write
   b. 163[261] ; set Data In = 261
   c. 161[5] ; set control to Write and Set Voltage High
   d. Wait 15ms ; requires 15ms High Voltage Pulse to Write
   e. 161[5] ; clear Voltage

Example #2 Read address 5 to confirm correct data properly programmed.

1) Read the word

   a. 5[i2c read] ; read register 5; this will be contents of EEPROM

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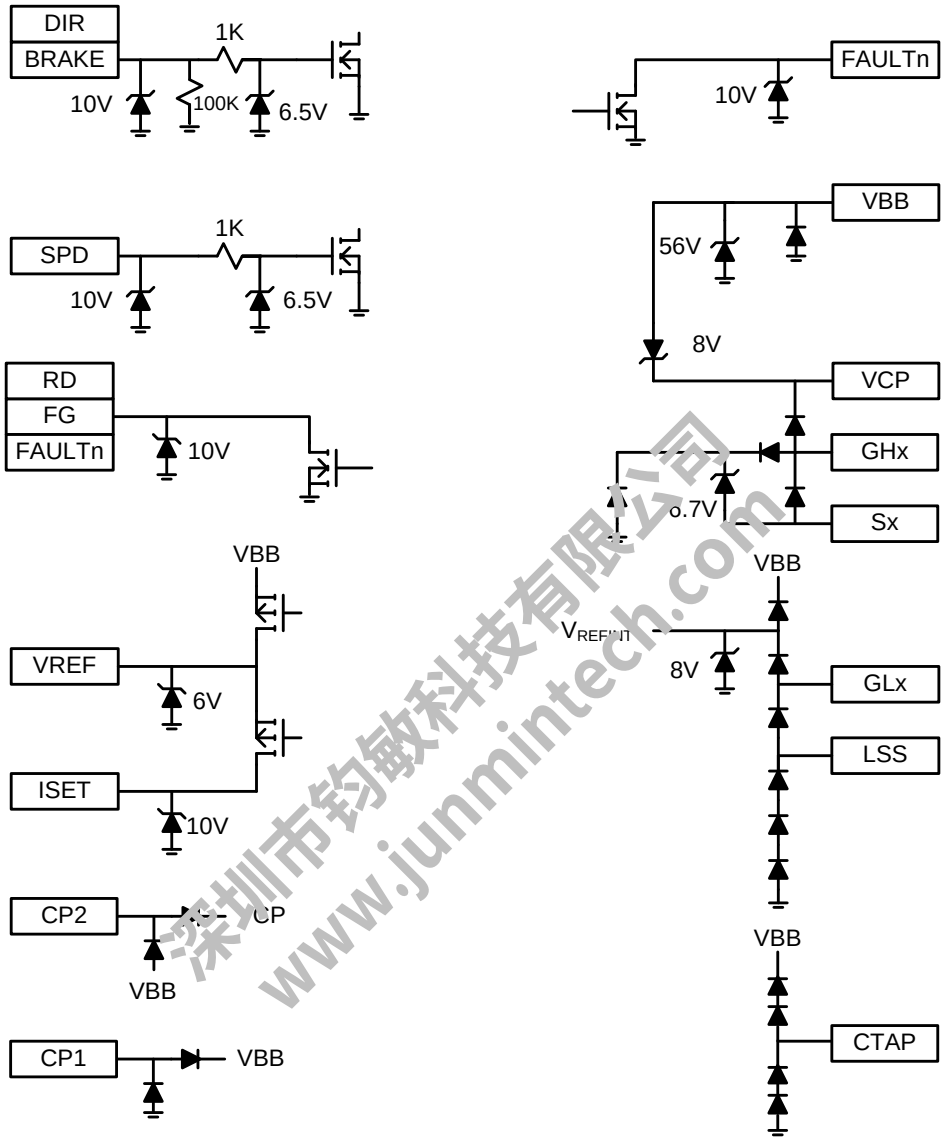
Pin Diagrams



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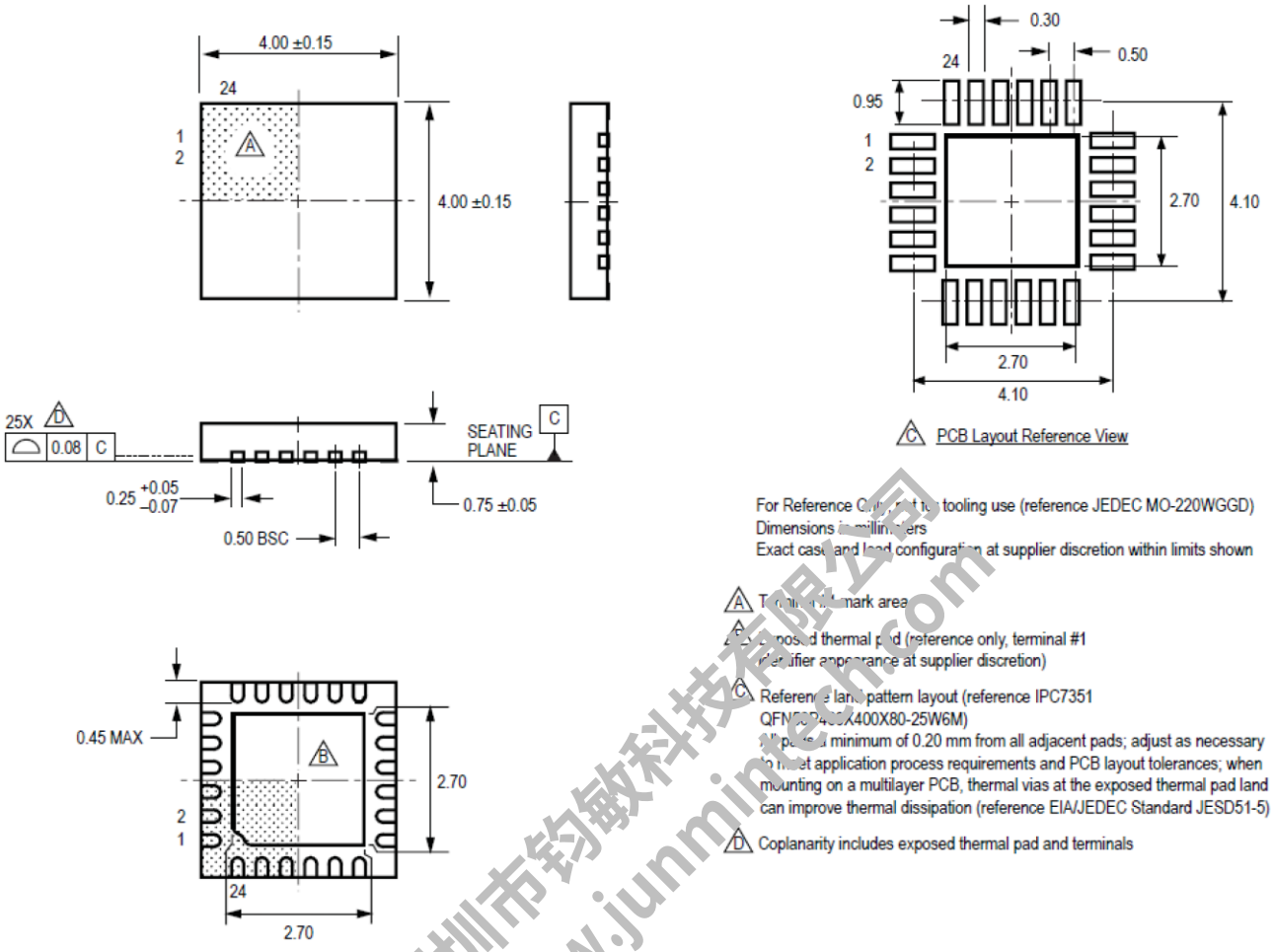
Package ES, 24 pin eQFN



For Reference Only – not for tooling use (reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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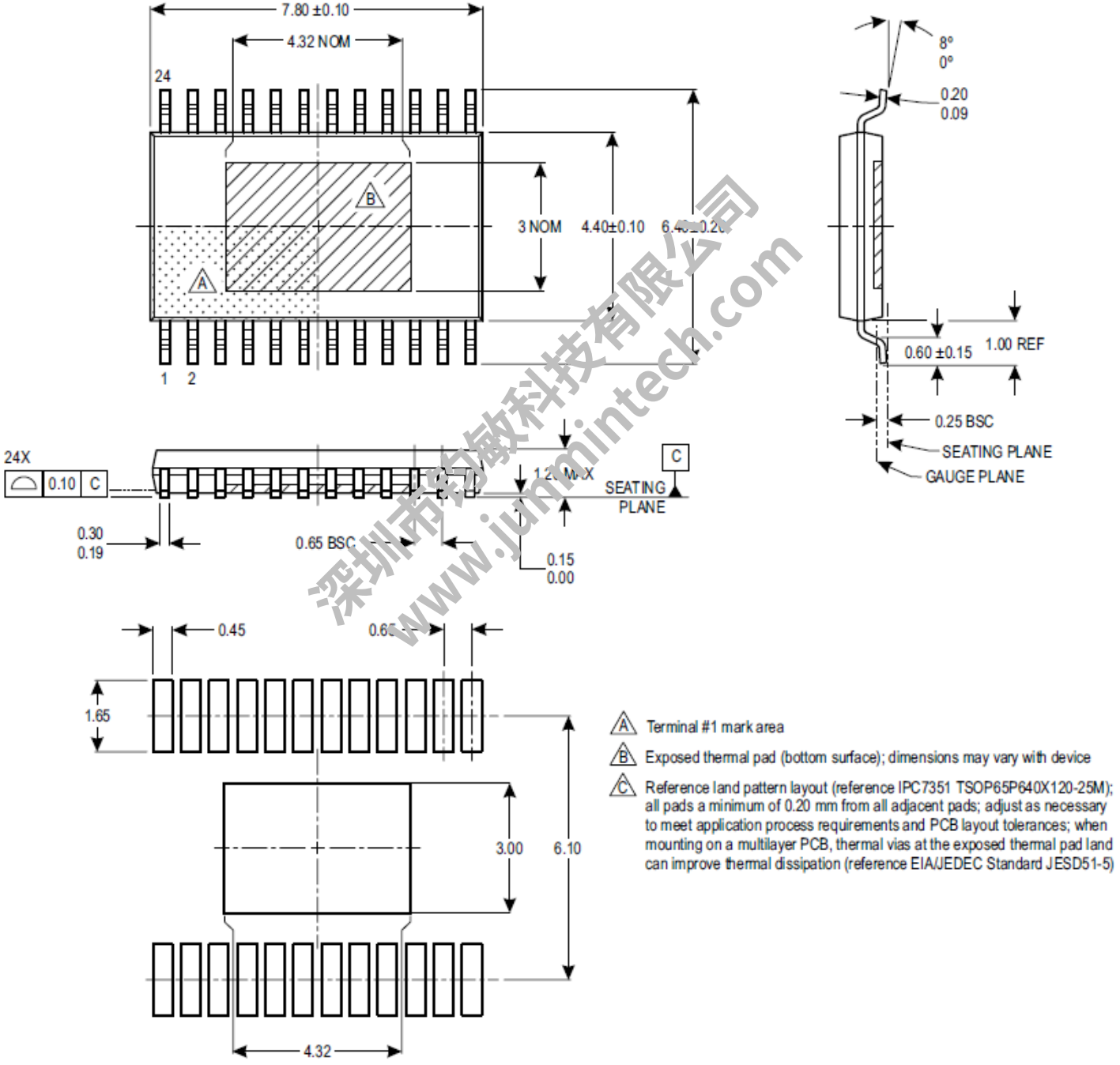
Package LP, 24 pin TSSOP

For Reference Only – Not for Tooling Use
(Reference MO-153 ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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