

October 2001 Revised May 2005

# 74ALVC16244

# Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

# **General Description**

The ALVC16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/ receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74ALVC16244 is designed for low voltage (1.65V to 3.6V)  $\rm V_{CC}$  applications with I/O capability up to 3.6V.

The 74ALVC16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### **Features**

- $\blacksquare$  1.65V–3.6V  $\rm V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- t<sub>PD</sub>

3.0 ns max for 3.0V to 3.6V  $\rm V_{CC}$  3.5 ns max for 2.3V to 2.7V  $\rm V_{CC}$  6.0 ns max for 1.65V to 1.95V  $\rm V_{CC}$ 

- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED98
- ESD performance:

Human body model > 2000V Machine model > 200V

Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver

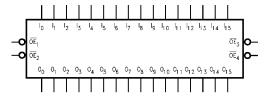
#### **Ordering Code:**

Order Number	Package Number	Package Description
74ALVC16244GX (Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]
74ALVC16244MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: BGA package available in Tape and Reel only.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol

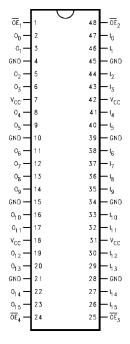


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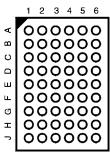
DS500677

# **Connection Diagrams**

#### Pin Assignment for TSSOP



#### Pin Assignment for FBGA



(Top Thru View)

# **Pin Descriptions**

Pin Names	Description
<del>OE</del> n	Output Enable Input (Active LOW)
I <sub>0</sub> –I <sub>15</sub>	Inputs
O <sub>0</sub> -O <sub>15</sub>	Outputs
NC	No Connect

# **FBGA Pin Assignments**

	1	2	3	4	5	6
Α	O <sub>0</sub>	NC	OE <sub>1</sub>	OE <sub>2</sub>	NC	$I_0$
В	O <sub>2</sub>	O <sub>1</sub>	NC	NC	I <sub>1</sub>	l <sub>2</sub>
С	O <sub>4</sub>	O <sub>3</sub>	V <sub>CC</sub>	V <sub>CC</sub>	l <sub>3</sub>	I <sub>4</sub>
D	O <sub>6</sub>	O <sub>5</sub>	GND	GND	I <sub>5</sub>	I <sub>6</sub>
E	O <sub>8</sub>	O <sub>7</sub>	GND	GND	I <sub>7</sub>	I <sub>8</sub>
F	O <sub>10</sub>	O <sub>9</sub>	GND	GND	I <sub>9</sub>	I <sub>10</sub>
G	O <sub>12</sub>	O <sub>11</sub>	V <sub>CC</sub>	V <sub>CC</sub>	I <sub>11</sub>	I <sub>12</sub>
Н	O <sub>14</sub>	O <sub>13</sub>	NC	NC	I <sub>13</sub>	I <sub>14</sub>
J	O <sub>15</sub>	NC	OE <sub>4</sub>	OE <sub>3</sub>	NC	I <sub>15</sub>

# **Truth Tables**

Inp	outs	Outputs		
OE <sub>1</sub>	I <sub>0</sub> –I <sub>3</sub>	O <sub>0</sub> -O <sub>3</sub>		
L	L	L		
L	Н	Н		
Н	X	Z		

Inp	outs	Outputs		
ŌE <sub>3</sub>	I <sub>8</sub> -I <sub>11</sub>	O <sub>8</sub> -O <sub>11</sub>		
L	L	L		
L	Н	Н		
Н	Χ	Z		

Inp	outs	Outputs
OE <sub>2</sub>	I <sub>4</sub> -I <sub>7</sub>	O <sub>4</sub> -O <sub>7</sub>
L	L	L
L	Н	Н
н	Χ	Z

Inj	outs	Outputs
ŌE₄	l <sub>12</sub> -l <sub>15</sub>	O <sub>12</sub> -O <sub>15</sub>
L	L	L
L	Н	н
н	X	Z

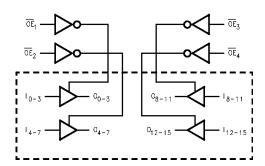
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

# **Functional Description**

The 74ALVC16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable  $(\overline{OE}_n)$  input. When  $\overline{OE}_n$  is LOW, the outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

# **Logic Diagram**



# **Absolute Maximum Ratings**(Note 4)

 $\label{eq:supply Voltage VCC} \begin{array}{ll} \text{Supply Voltage (V}_{CC}) & -0.5 \text{V to } +4.6 \text{V} \\ \text{DC Input Voltage (V}_{I}) & -0.5 \text{V to } 4.6 \text{V} \\ \end{array}$ 

Output Voltage (V $_{\rm O}$ ) (Note 5)  $-0.5 \mbox{V}$  to V $_{\rm CC}$  +0.5 \mathbf{V}

DC Input Diode Current (I<sub>IK</sub>)

 $V_{I} < 0V \hspace{1cm} -50 \hspace{1cm} mA \hspace{1cm}$ 

DC Output Diode Current (I<sub>OK</sub>)

 $V_O < 0V$  –50 mA

DC Output Source/Sink Current

 $(I_{OH}/I_{OL})$  ±50 mA

DC  $V_{CC}$  or GND Current per

Supply Pin (I $_{CC}$  or GND)  $\pm 100$  mA

Storage Temperature Range (T<sub>STG</sub>) -65°C to +150°C

# Recommended Operating Conditions (Note 6)

Power Supply

Operating 1.65V to 3.6V Input Voltage ( $V_1$ ) 0V to  $V_{CC}$ 

Output Voltage (V<sub>O</sub>) 0V to V<sub>CC</sub> Free Air Operating Temperature ( $T_A$ )  $-40^{\circ}C$  to  $+85^{\circ}C$ 

Minimum Input Edge Rate (Δt/ΔV)

 $V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$  10 ns/\

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5:  $I_{\rm O}$  Absolute Maximum Rating must be observed, limited to 4.6V.

Note 6: Floating or unused control inputs must be held HIGH or LOW.

# **DC Electrical Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub>	Min	Max	Units
Зуппоп	Farameter	Conditions	(V)	IVIIII	IVIAA	Onits
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V <sub>CC</sub>		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V <sub>IL</sub>	LOW Level Input Voltage		1.65 - 1.95		0.35 x V <sub>CC</sub>	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	1.65 - 3.6	V <sub>CC</sub> - 0.2		
		I <sub>OH</sub> = -4 mA	1.65	1.2		
		I <sub>OH</sub> = -6 mA	2.3	2.0		
		I <sub>OH</sub> = -12 mA	2.3	1.7		V
			2.7	2.2		
			3.0	2.4		
		I <sub>OH</sub> = -24 mA	3.0	2		
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	1.65 - 3.6		0.2	
		I <sub>OL</sub> = 4 mA	1.65		0.45	
		I <sub>OL</sub> = 6 mA	2.3		0.4	V
		I <sub>OL</sub> = 12 mA	2.3		0.7	V
			2.7		0.4	
		I <sub>OL</sub> = 24 mA	3.0		0.55	
I	Input Leakage Current	$0 \le V_I \le 3.6V$	3.6		±5.0	μА
l <sub>OZ</sub>	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	3.6		±10	μА
Icc	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μА
Δl <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μΑ

# **AC Electrical Characteristics**

		$T_A = -40^{\circ}$ C to $+85^{\circ}$ C, $R_L = 500\Omega$								
Symbol	Parameter	C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				Units
- Cymbol		$V_{CC}=3.3V\pm0.3V$		V <sub>CC</sub> = 2.7V		$V_{CC}=2.5V\pm0.2V$		$V_{CC} = 1.8V \pm 0.15V$		Onito
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.3	3	1.5	3.5	1.0	3.0	1.5	6.0	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.3	4.0	1.5	4.6	1.0	4.1	1.5	8.2	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.3	4.0	1.5	4.3	1.0	3.8	1.5	6.8	ns

# Capacitance

Symbol	Parameter		Conditions	<b>T</b> <sub>A</sub> = -	Units	
Symbol Farameter		Conditions	V <sub>CC</sub>	Typical		
C <sub>IN</sub>	Input Capacitance		V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	6	pF
C <sub>OUT</sub>	Output Capacitance		V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	7	pF
C <sub>PD</sub>	Power Dissipation Capacitance O	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 0 pF	3.3	20	pF
				2.5	20	Pi

# **AC Loading and Waveforms**

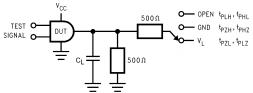


Table 1: Values for Figure 1

TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
$t_{PZL}$ , $t_{PLZ}$	$V_{L}$
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

FIGURE 1. AC Test Circuit

Table 2: Variable Matrix (Input Characteristics: f = 1MHz;  $t_r$  =  $t_f$  = 2ns;  $Z_0$  = 50 $\Omega$ )

Symbol	V <sub>CC</sub>							
Cymbol	$3.3V \pm 0.3V$	2.7V	2.5V ± 0.2V	1.8V ± 0.15V				
V <sub>mi</sub>	1.5V	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2				
V <sub>mo</sub>	1.5V	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2				
V <sub>X</sub>	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.15V	V <sub>OL</sub> + 0.15V				
$V_{Y}$	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.15V	V <sub>OH</sub> – 0.15V				
V <sub>L</sub>	6V	6V	V <sub>CC</sub> *2	V <sub>CC</sub> *2				

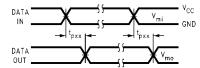


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

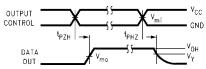


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

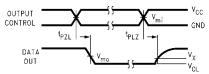
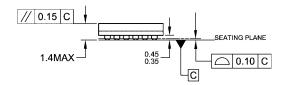


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

## Physical Dimensions inches (millimeters) unless otherwise noted ○ 0.10 B В 5.5 0.8 Α -(0.8) 0.10 A —(0.75) <sub>1</sub> ABCDEFGHJ 00000 PIN ONE 8 0.8 1/23<sup>|</sup>456 Top



View

#### NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- **B. ALL DIMENSIONS IN MILLIMETERS**
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
  .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
  D. DRAWING CONFORMS TO ASME Y14.5M-1994

54X 0.5<sup>+0.05</sup>

0.15(M) C A B 0.08(M) C

**Bottom** 

View

#### BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide Package Number BGA54A

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-89 9.20 B.10 50. O.2 C B A ALL LEAD TIPS PIN #1 IDENT LAND PATTERN RECOMMENDATION O.1 C ALL LEAD TIPS SEE DETAIL A 0.90+0.15 0.09-0.20 0.10±0.05 0.17-0.27 0.50 ♦ 0.13\( \old{\text{0}} \) A B\( \old{\text{S}} \) C\( \old{\text{S}} \) 12.00' TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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