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1 Block diagram and pin descriptions

Figure 1. Block diagram

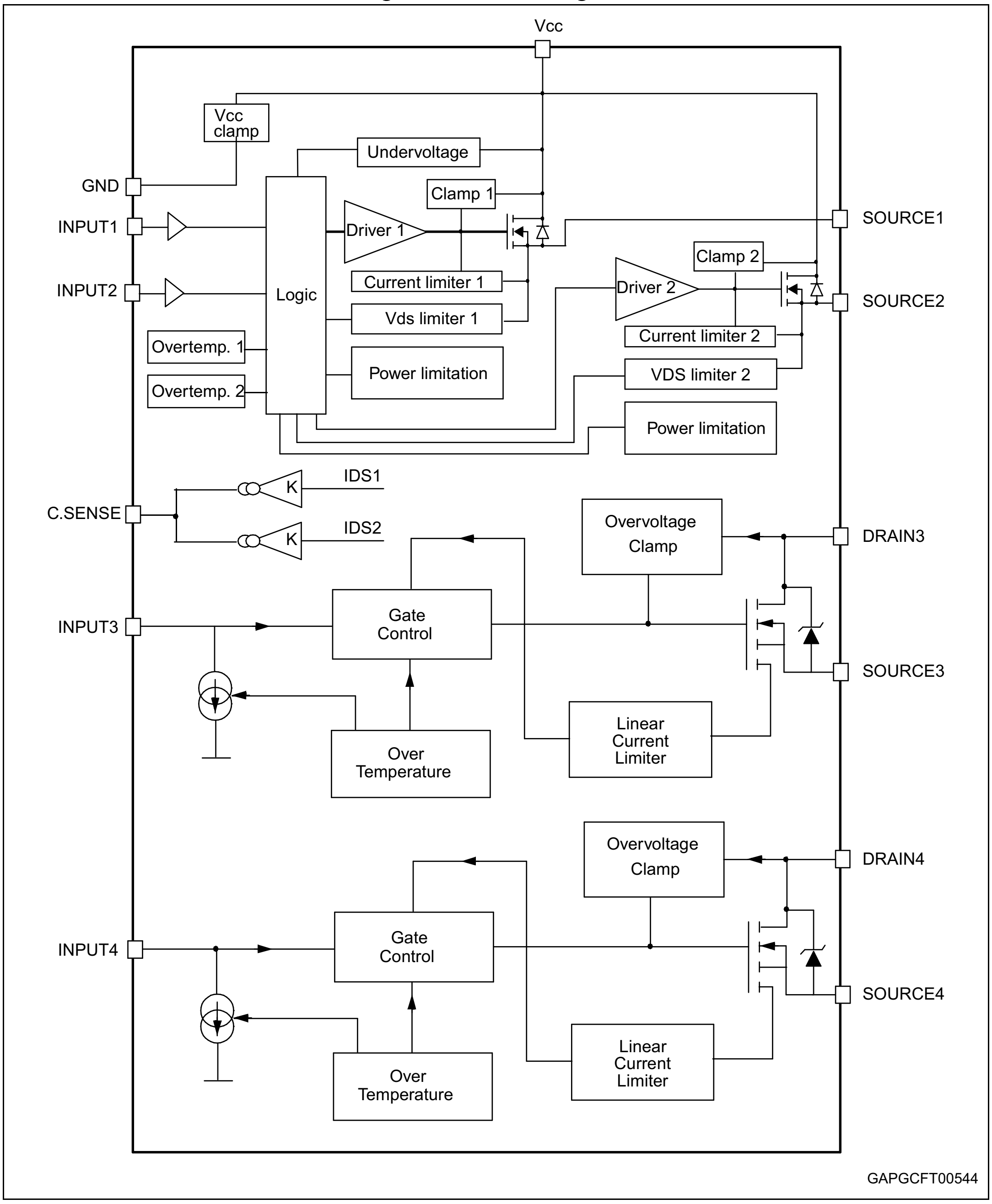


Table 1. Pin descriptions

No	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switch)
2	INPUT 3	Input of switch 3 (low-side switch)
4, 11	N.C.	Not connected
5, 10, 19, 24	V_{CC}	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
7	INPUT 1	Input of switch 1 (high-side switches)
8	INPUT 2	Input of switch 2 (high-side switch)
9	CURRENT SENSE	Analog current sense pin, it delivers a current proportional to the load current
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switch)
20, 21	SOURCE 2	Source of switch 2 (high-side switch)
22, 23	SOURCE 1	Source of switch 1 (high-side switch)
26, 27	SOURCE 3	Source of switch 3 (low-side switch)

Figure 2. Configuration diagram (top view)

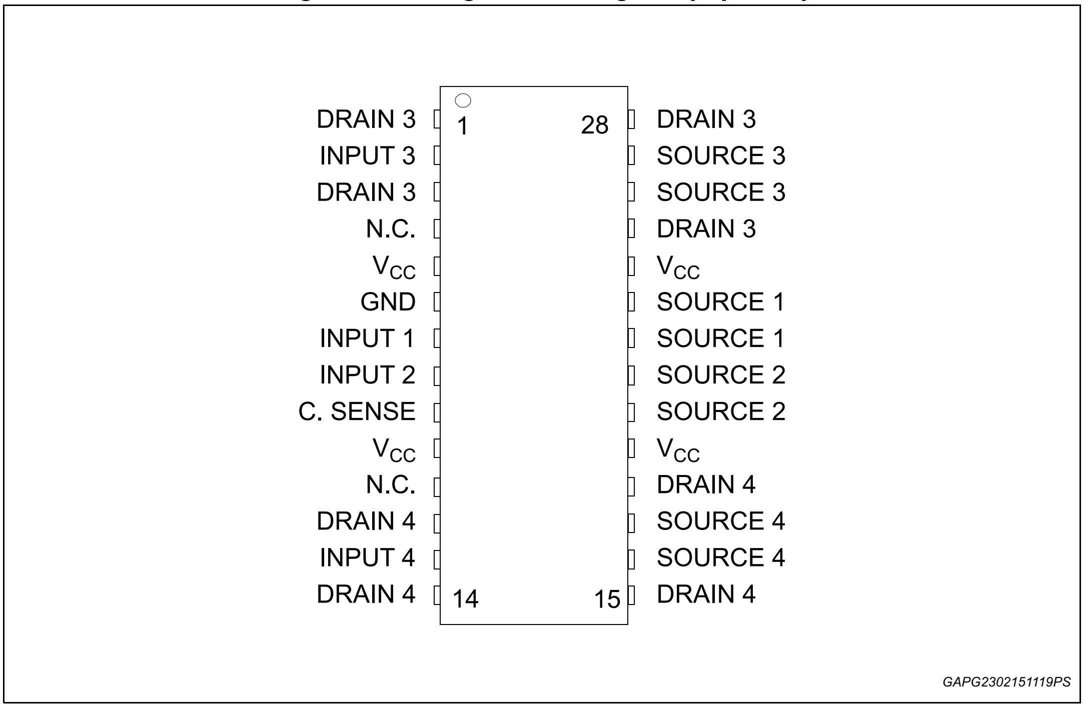


Table 2. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-lead (high-side switch)	10	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-lead (low-side switch)	7	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 39*	°C/W

2 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* and *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in *Section 2.1: Absolute maximum ratings* for extended periods may affect device reliability.

2.1 Absolute maximum ratings

Table 3. Dual high-side switch

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-12	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 3.7 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; $I_{OUT} = I_{limL}$(Typ.))	32	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) – INPUT – CURRENT SENSE – OUTPUT – V_{CC}	 4000 2000 5000 5000	 V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Table 4. Low-side switch

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-source voltage (V_{INn} = 0 V)	Internally clamped	V
V_{INn}	Input voltage	Internally clamped	V
I_{INn}	Input current	+/-20	mA
$R_{IN\ MINn}$	Minimum input series impedance	220	Ω
I_{Dn}	Drain current	Internally limited	A
I_{Rn}	Reverse DC output current	-12	A
V_{ESD1}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF)	4000	V
V_{ESD2}	Electrostatic discharge on output pins only (R = 330 Ω, C = 150 pF)	16500	V
P_{tot}	Total dissipation at T_c = 25 °C	4	W
T_j	Operating junction temperature	Internally limited	°C
T_c	Case operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

3 Electrical characteristics

3.1 Electrical characteristics for dual high-side switch

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C < T_j < 150 °C, unless otherwise specified (for each channel).

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 3 A; T_j = 25 °C		160		mΩ
		I_{OUT} = 3 A; T_j = 150 °C			320	mΩ
		I_{OUT} = 3 A; V_{CC} = 5 V; T_j = 25 °C			210	mΩ
V_{clamp}	Clamp Voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		2(1)	5(1)	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		3	6	mA
$I_{L(off)}$	Off-state output current(2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0		3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	µA
V_F	Output - V_{CC} diode voltage(2)	-I_{OUT} = 3 A; T_j = 150 °C			0.7	V

1. PowerMOS leakage included
2. For each channel

Table 6. Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 4.3 Ω (see *Figure 3*)	—	15	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 4.3 Ω (see *Figure 3*)	—	10	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 4.3 Ω	—	See *Figure 15*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 4.3 Ω	—	See *Figure 17*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 4.3 Ω (see *Figure 3*)	—	0.16	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 4.3 Ω (see *Figure 3*)	—	0.08	—	mJ

Table 7. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V

Table 8. Protection and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	V_{CC} = 13 V	6	8.5	12	A
		5 V < V_{CC} < 36 V			12	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		3.5		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 1 A; V_{IN} = 0; L = 20 mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.03 A; T_j = -40 °C to 150 °C (see *Figure 4*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 9. Current sense ($8V<V_{CC}<16V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.08 A; V_{SENSE} = 0.5 V; T_j = -40°C to 50°C	850	1450	2120	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.35 A; V_{SENSE} = 0.5V; T_j = -40°C to 150°C	840	1360	2000	
		T_j = 25°C to 150°C	980	1360	1740	
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3A; V_{SENSE} = 4V; T_j = -40°C to 150°C	1200	1270	1350	
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 4A; V_{SENSE} = 4V; T_j = -40°C to 150°C	1200	1270	1350	
I_{SENSE0}	Analog sense current	I_{OUT} = 0A; V_{SENSE} = 0V; V_{IN} = 0V; T_j = -40°C to 150°C	0		1	µA
		I_{OUT} = 0A; V_{SENSE} = 0V; V_{IN} = 5V; T_j = -40°C to 150°C	0		2	µA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 5A; R_{SENSE} = 3.9 KΩ	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC} = 13V; R_{SENSE} = 3.9 KΩ		9		V
I_{SENSEH}	Analog sense output current in overtemperature condition	V_{CC} = 13V		8		mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE}<4 V; 0.35 A<I_{out}<5 A; I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 5*)		70	300	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE}<4 V; 0.35 A<I_{out}<5 A; I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 5*)		100	250	µs

Figure 3. Switching time waveforms

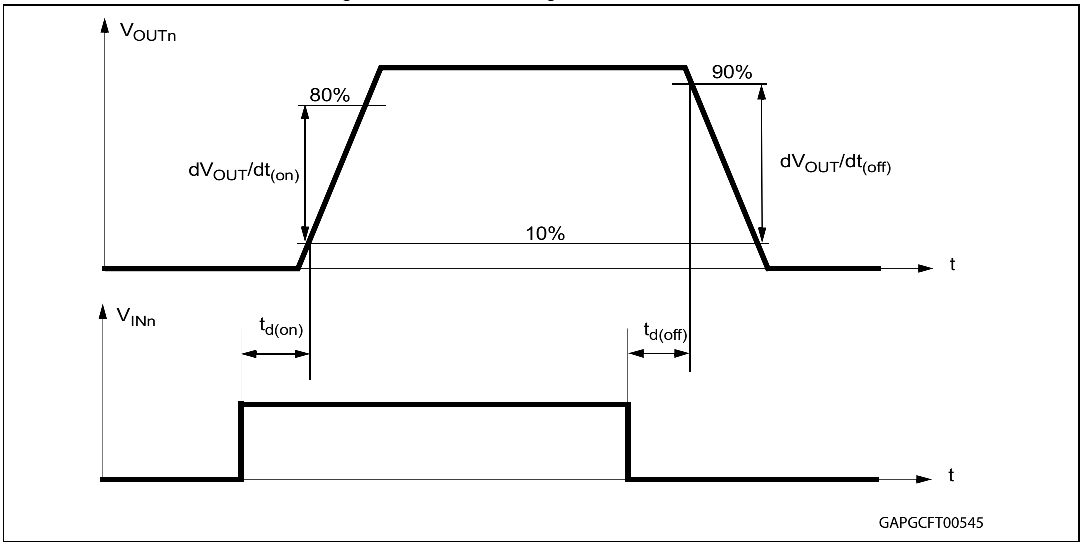


Figure 4. Output voltage drop limitation

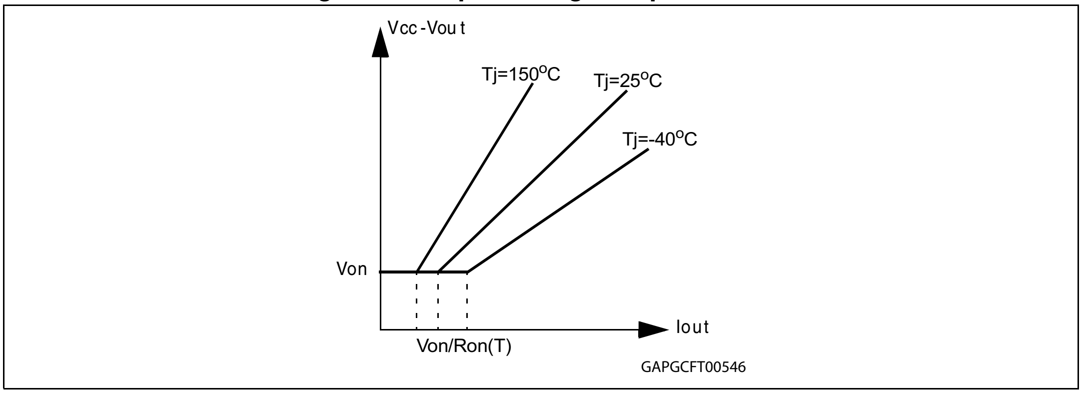
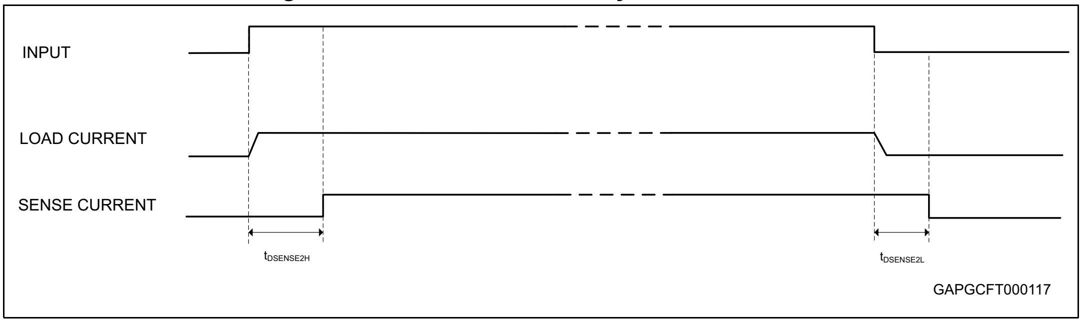


Table 10. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short circuit to GND	L H	L L	0 0
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Figure 5. Current sense delay characteristics



4 Electrical characteristics curves for dual high-side switch

Figure 6. Off-state output current

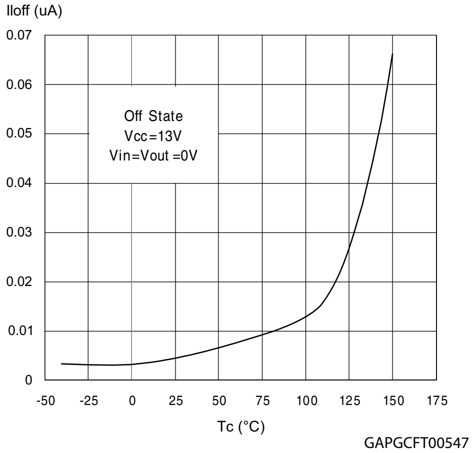


Figure 7. High level input current

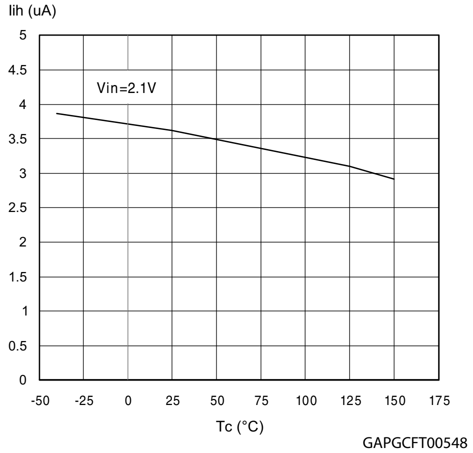


Figure 8. Input clamp voltage

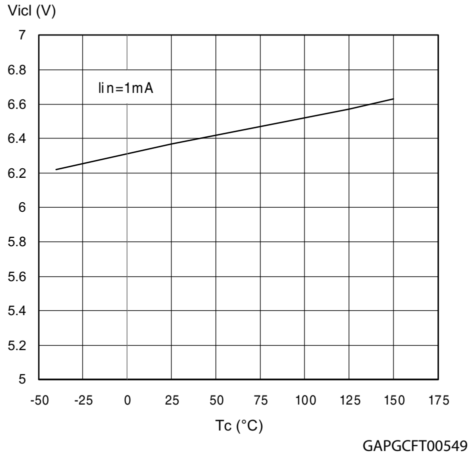


Figure 9. Input low level

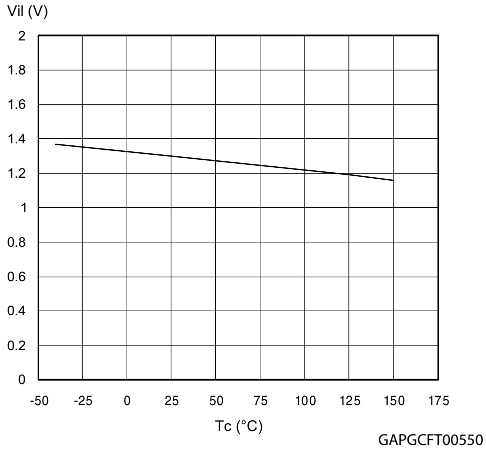


Figure 10. Input high level

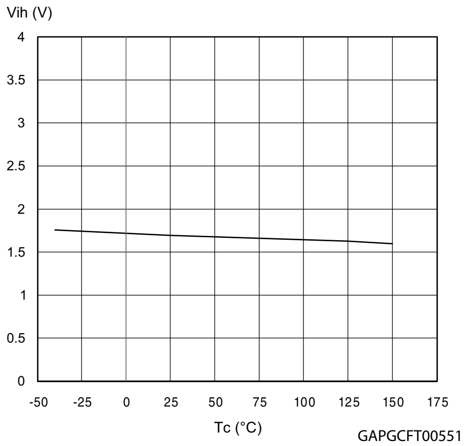


Figure 11. Input hysteresis voltage

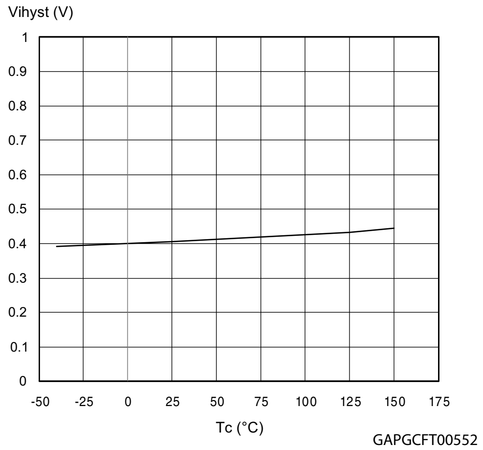


Figure 12. On-state resistance vs T_{case}

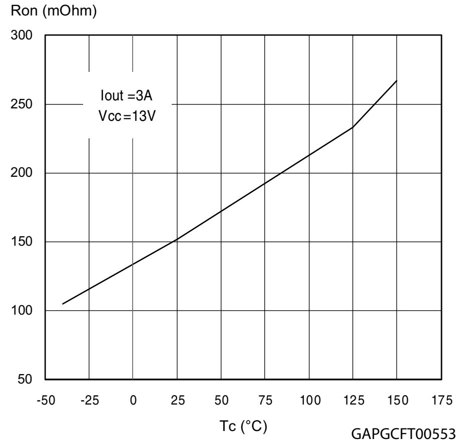


Figure 13. On-state resistance vs V_{CC}

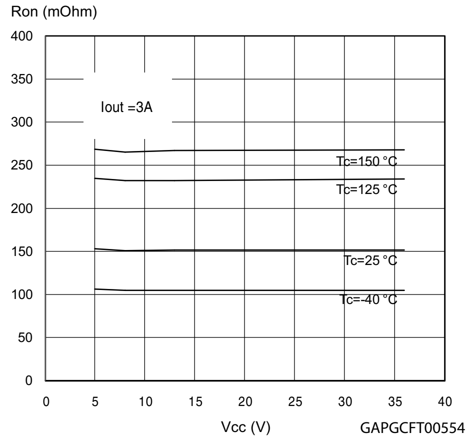


Figure 14. Undervoltage shutdown

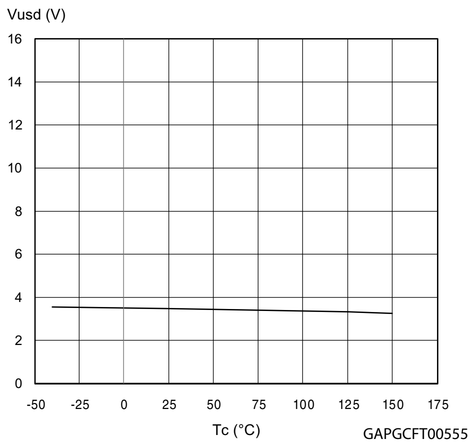


Figure 15. Turn-on voltage slope

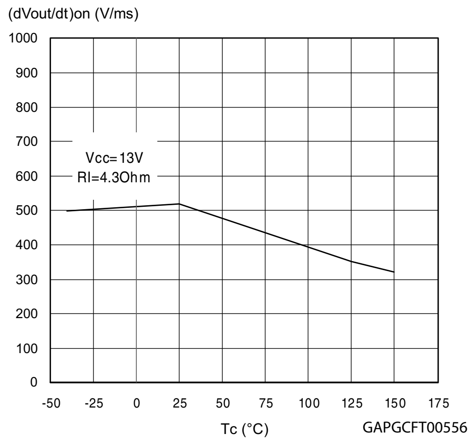


Figure 16. I_{LIMH} vs T_{case}

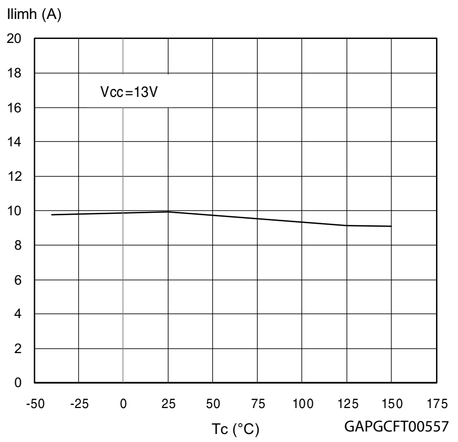
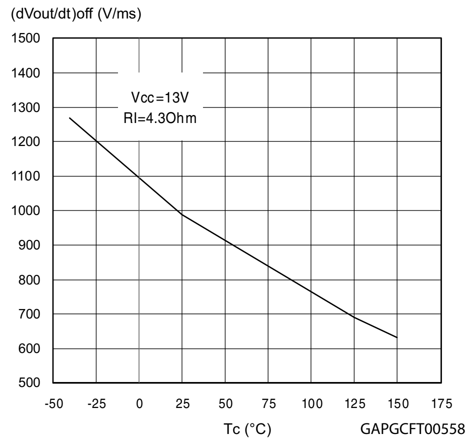


Figure 17. Turn-off voltage slope



4.1 Electrical characteristics for low-side switches

Values specified in this section are for -40 °C < T_j < 150 °C, unless otherwise specified

Table 11. Off

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 1.5 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS} = V_{IN}; I_D = 1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS} = 0 V; V_{IN} = 5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} = 0V)	V_{DS} = 13 V; V_{IN} = 0 V; T_j = 25 °C			30	µA
		V_{DS} = 25 V; V_{IN} = 0 V			75	µA

Table 12. On

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static drain-source on resistance	V_{IN} = 5 V; I_D = 3 A; T_j = 25 °C	—	—	120	mΩ
		V_{IN} = 5 V; I_D = 3 A	—	—	240	mΩ

Table 13. Dynamic (T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g_{fs}	Forward transconductance	V_{DD} = 13 V; I_D = 1.5 A	—	2.5	—	S
C_{OSS}	Output capacitance	V_{DS} = 13 V; f = 1 MHz; V_{IN} = 0 V	—	150	—	pF

Table 14. Switching (T_j = 25 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 3 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MINn}$ = 220 Ω	—	200	400	ns
t_r	Rise time		—	1.2	2.5	µs
$t_{d(off)}$	Turn-off delay time		—	600	1350	ns
t_f	Fall time		—	400	1000	ns
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 3 A V_{gen} = 5 V; R_{gen} = 2.2 KΩ	—	0.80	2.5	µs
t_r	Rise time		—	3.7	7.5	µs
$t_{d(off)}$	Turn-off delay time		—	2.6	7.5	µs
t_f	Fall time		—	2.3	7.0	µs

Table 14. Switching (T_j = 25 °C, unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$(dI/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V; I_D = 3 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MINn}$ = 220 Ω	—	3.0		A/µs
Q_i	Total input charge	V_{DD} = 12 V; I_D = 3 A; V_{IN} = 5 V; I_{gen} = 2.13 mA	—	9.0		nC

Table 15. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = 1.5 A; V_{IN} = 0 V	—	0.8	—	V
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A; dI/dt = 12 A/ms; V_{DD} = 30 V; L = 200 µH	—	400	—	ns
Q_{rr}	Reverse recovery charge		—	200	—	nC
I_{RRM}	Reverse recovery current		—	1.0	—	A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 16. Protection and diagnostics (-40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{lim}	Drain current limit	V_{IN} = 5 V; V_{DS} = 13 V	6	8.5	12	A
t_{dlim}	Step response current limit	V_{IN} = 5 V; V_{DS} = 13 V		10		µs
T_{jsh}	Overtemperature shutdown		150	175	200	°C
T_{jrs}	Overtemperature reset		135			°C
I_{gf}	Fault sink current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	Starting T_j = 25 °C; V_{DD} = 24 V; V_{IN} = 5 V; R_{gen} = $R_{IN\ MINn}$ = 220 Ω; L = 24 mH	100			mJ

4.2 Electrical characteristics curves for low-side switches

Figure 18. Static drain source on resistance

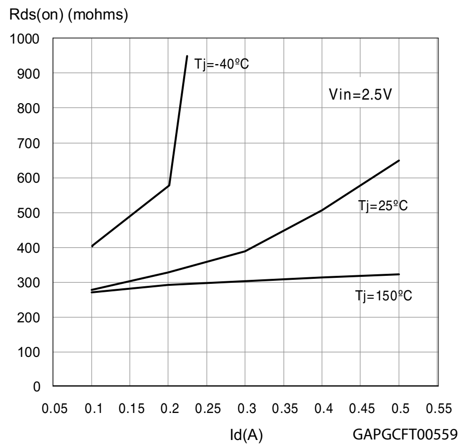


Figure 19. Derating curve

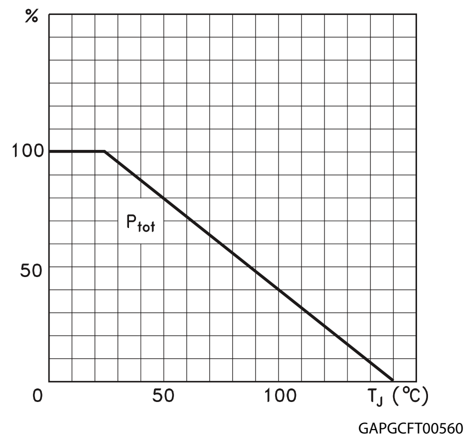


Figure 20. Transconductance

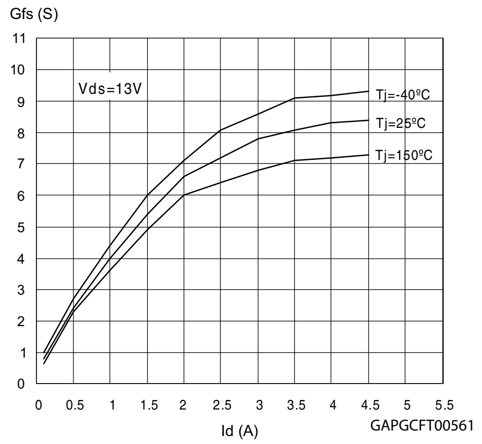


Figure 21. Transfer characteristics

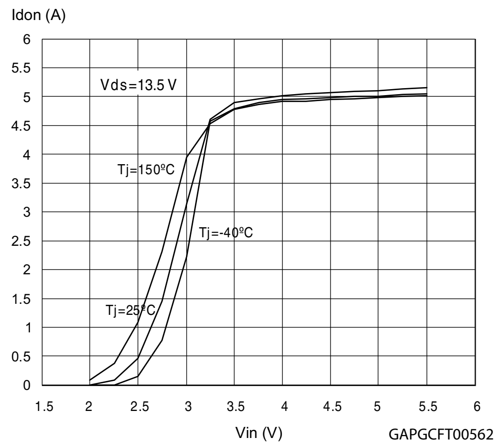


Figure 22. Input voltage vs input charge

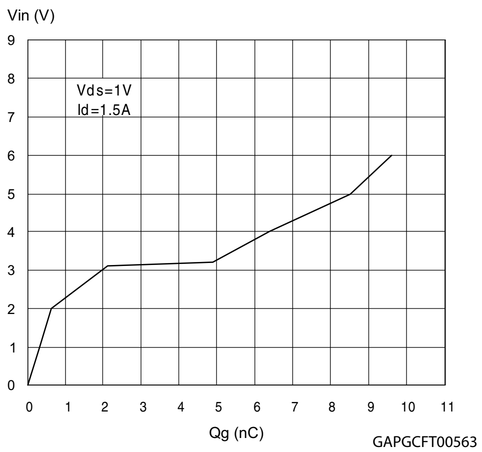


Figure 23. Capacitance variations

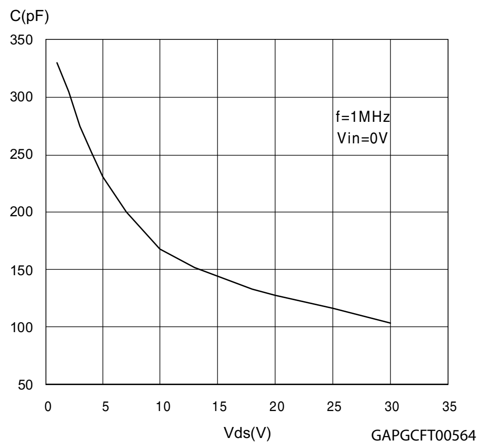


Figure 24. Output characteristics

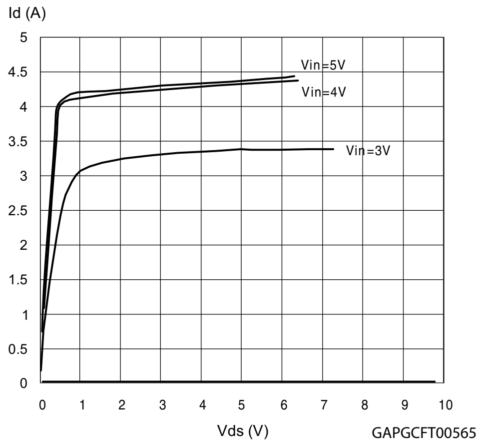


Figure 25. Step response current limit

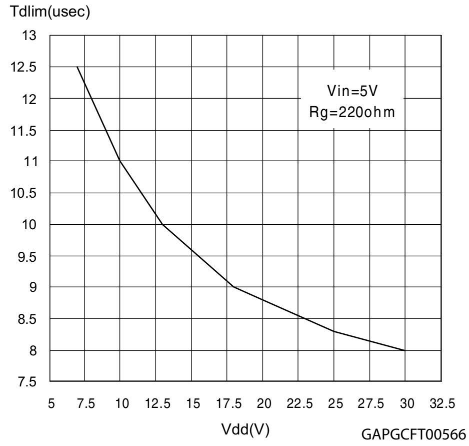


Figure 26. Source-drain diode forward characteristics

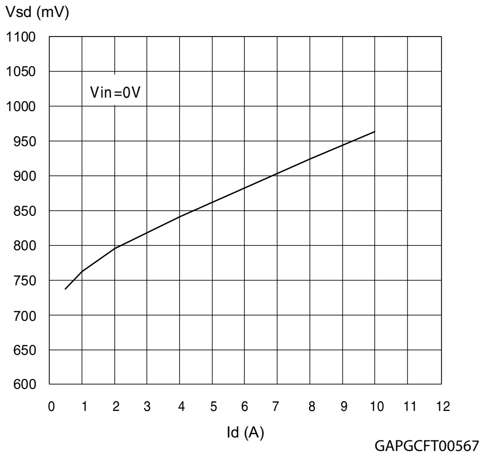


Figure 27. Static drain-source on resistance vs I_D

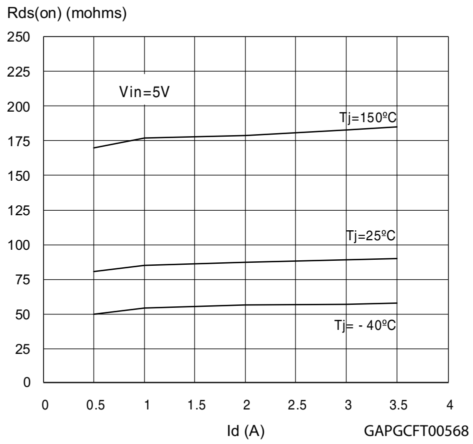


Figure 28. Static drain-source on resistance vs input voltage (part 1)

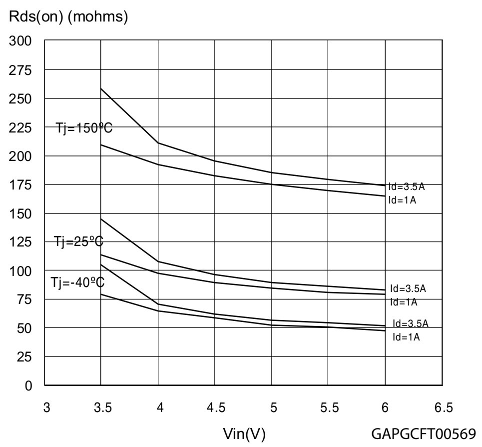


Figure 29. Static drain-source on resistance vs input voltage (part 2)

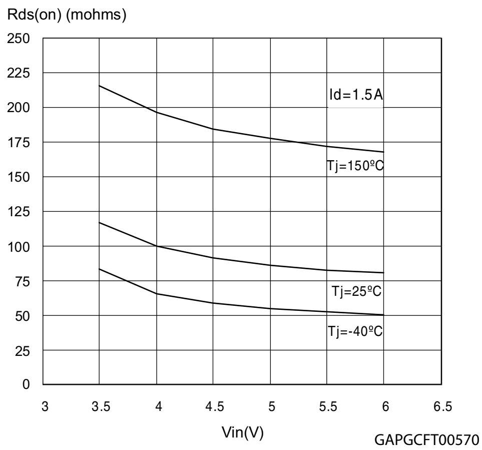


Figure 30. Normalized input threshold voltage vs temperature

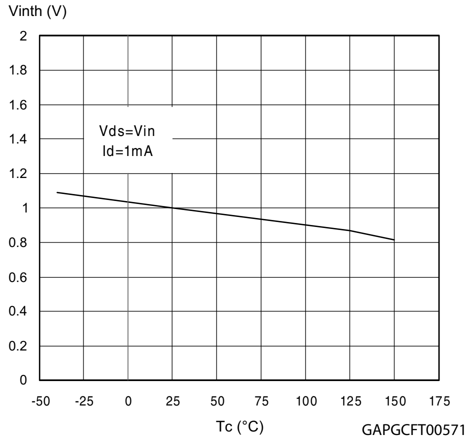


Figure 31. Normalized on resistance vs temperature

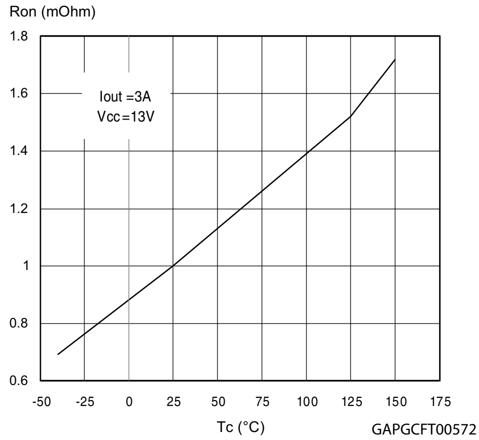
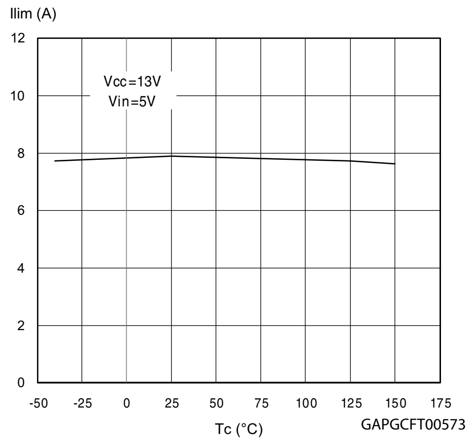
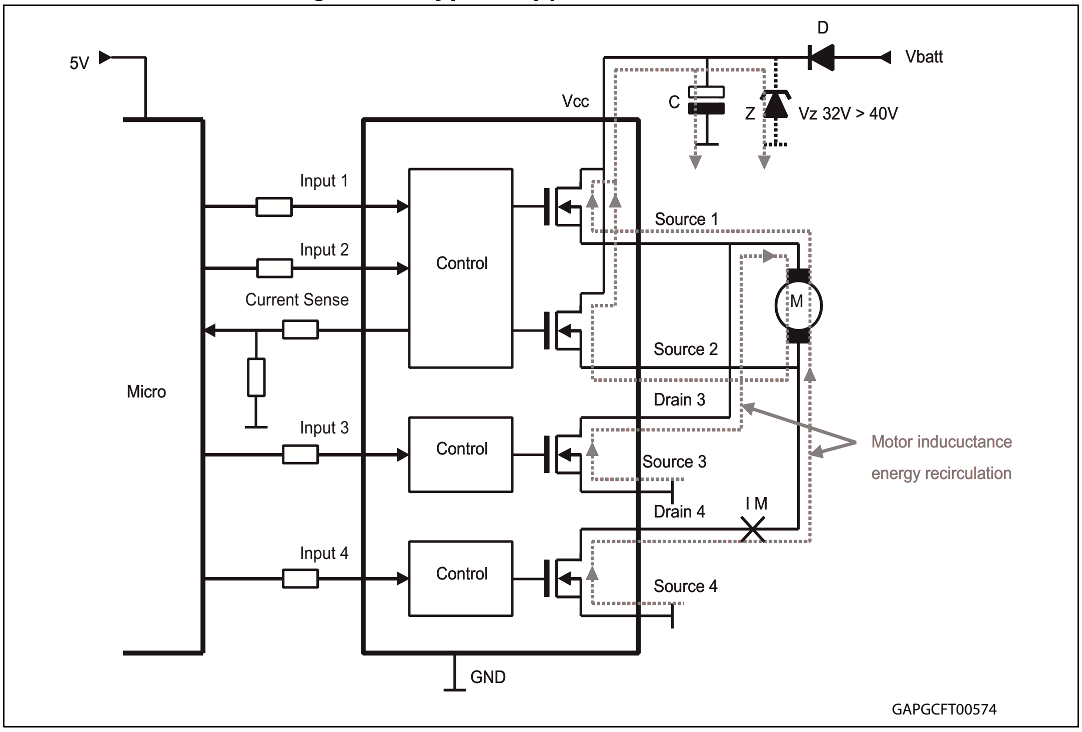


Figure 32. Current limit vs junction temperature



5 Application information

Figure 33. Typical application schematic



Note: *Mostly motor bridge drivers use a reverse battery protection diode (D) inside supply rail. This diode prevents a reverse current flow back to Vbatt in case the bridge gets disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (Vcc), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50 µF per 1 A load current in recommended. In alternative, also a Zener protection (Z) is suitable. Even if a reverse polarity diode is not present, it is recommended to use a capacitor or zener at Vcc because a similar problem appears in case supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while motor is operating.*

Figure 34. Recommended motor operation

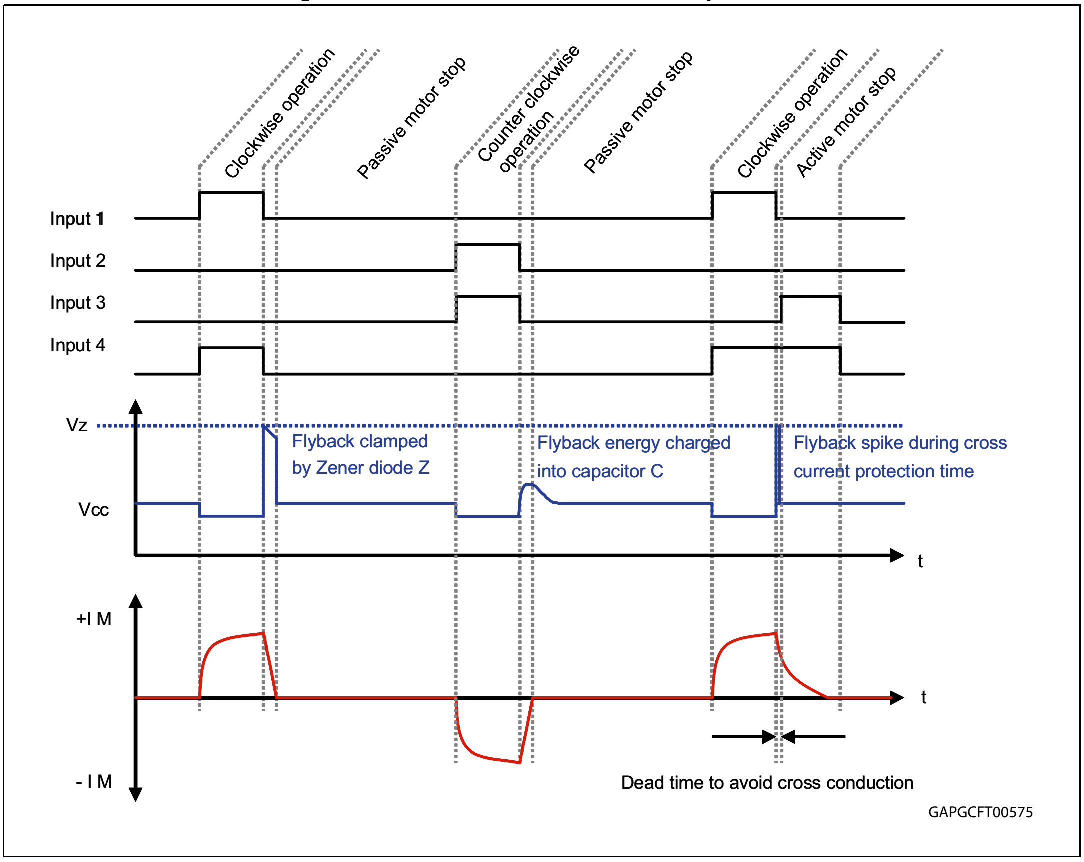
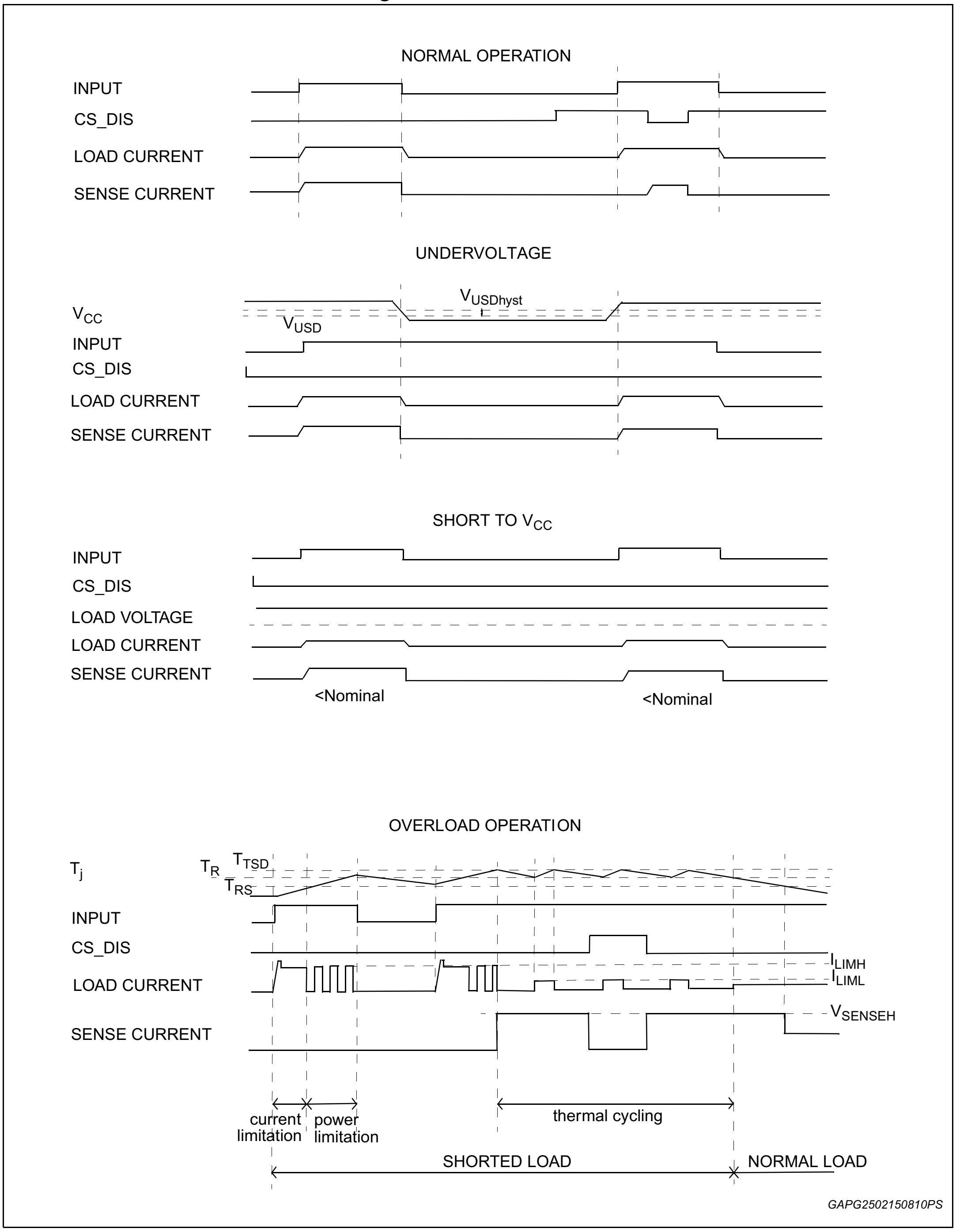
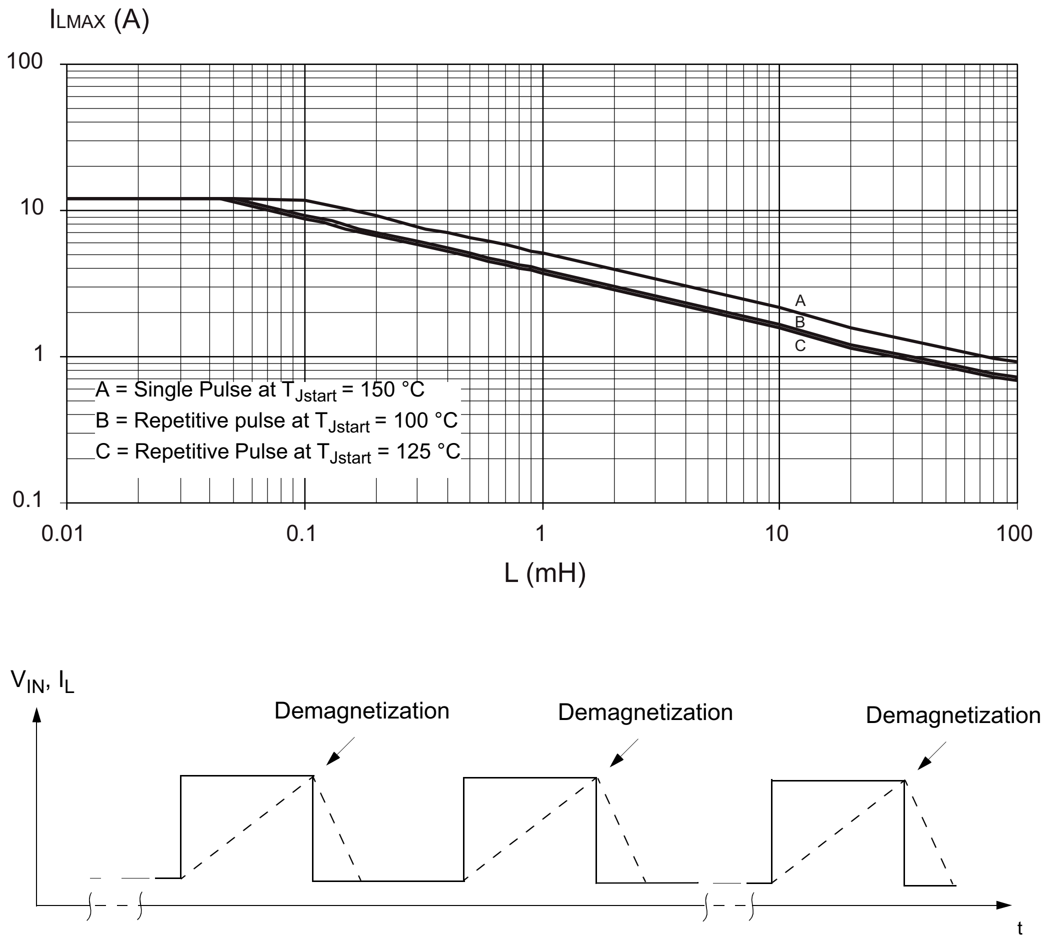


Figure 35. Waveforms



5.1 Maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 36. Maximum turn off current versus load inductance



Note:
Values are generated with R_L = 0 Ω
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

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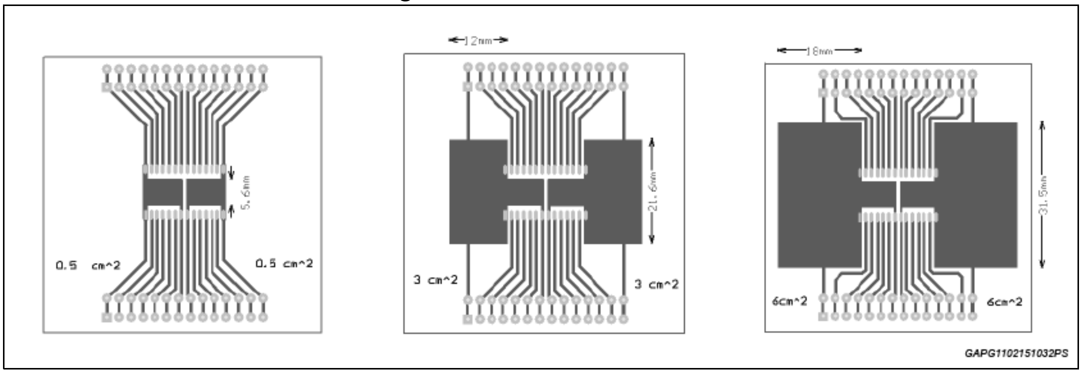
6 Package and thermal data

6.1 SO-28 thermal data

Figure 37. SO-28 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: from minimum pad layout to 16 cm^2).

Figure 38. Chipset configuration

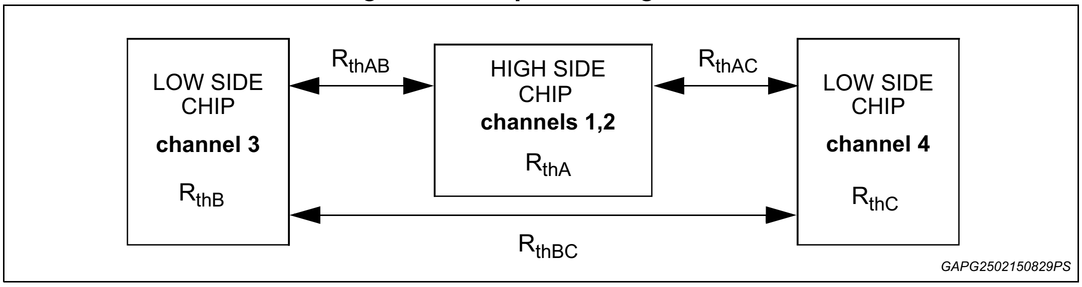
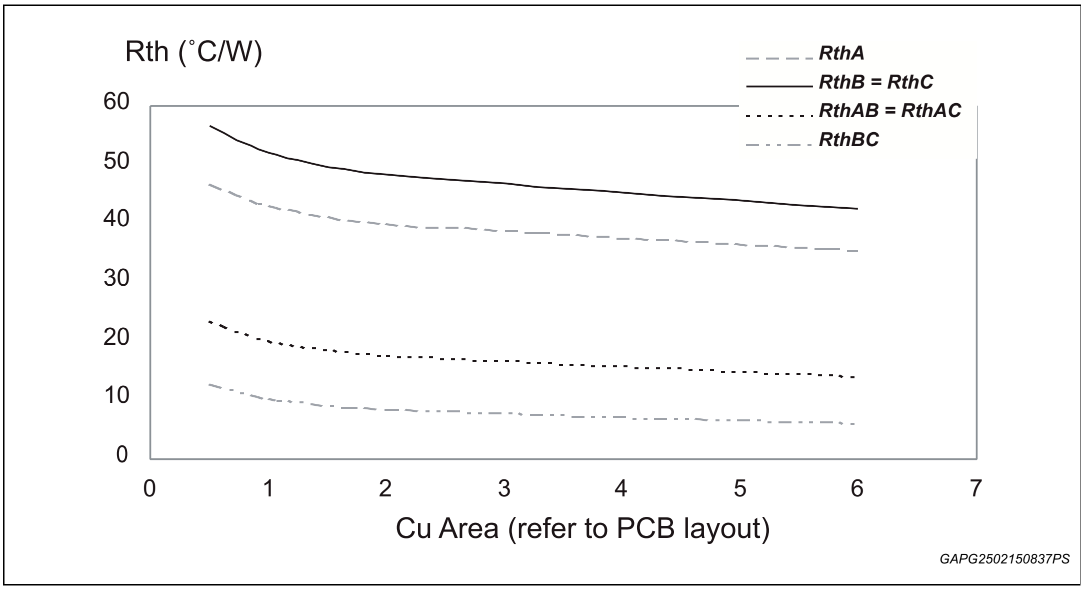


Figure 39. Auto and mutual Rthj-amb vs PCB copper area in open box free air condition



Note: See Figure 38. For more detailed information see Table 17 and Table 18.

Table 17. Thermal calculations in clockwise and anti-clockwise operation in steady-state mode

HS_1	HS_2	LS_3	LS_4	T_{jHS12}	T_{jLS3}	T_{jLS4}
ON	OFF	OFF	ON	$P_{dHS1} \times R_{thHS} + P_{dLS4} \times R_{thHSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHS2} \times R_{thHS} + P_{dLS3} \times R_{thHSLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLSLS} + T_{amb}$

Table 18. Thermal resistances definitions

Parameter	Definition
$R_{thHS} = R_{thHS1} = R_{thHS2}$	High-side chip thermal resistance junction to ambient (HS_1 or HS_2 in ON-state)
$R_{thLS} = R_{thLS3} = R_{thLS4}$	Low-side chip thermal resistance junction to ambient
$R_{thHSLS} = R_{thHS1LS4} = R_{thHS2LS3}$	Mutual thermal resistance junction to ambient between high-side and low-side chips
$R_{thLSLS} = R_{thLS3LS4}$	Mutual thermal resistance junction to ambient between low-side chips

Note: Values dependent on PCB heatsink area.

Table 19. Single pulse thermal impedance definitions

Parameter	Definition
Z_{thHS}	High-side chip thermal impedance junction to ambient
$Z_{thLS} = Z_{thLS3} = Z_{thLS4}$	Low-side chip thermal impedance junction to ambient
$Z_{thHSLS} = Z_{thHS12LS3} = Z_{thHS12LS4}$	Mutual thermal impedance junction to ambient between high-side and low-side chips
$Z_{thLSLS} = Z_{thLS3LS4}$	Mutual thermal impedance junction to ambient between low-side chips

Note: Values dependent on PCB heatsink area.

Table 20. Thermal calculations in transient mode

Parameter	Definition
T_{jHS12}	$Z_{thHS} \times P_{dHS12} + Z_{thHSLS} \times (P_{dLS3} + P_{dLS4}) + T_{amb}$
T_{jLS3}	$Z_{thHSLS} \times P_{dHS12} + Z_{thLS} \times P_{dLS3} + Z_{thLSLS} \times P_{dLS4} + T_{amb}$
T_{jLS4}	$Z_{thHSLS} \times P_{dHS12} + Z_{thLSLS} \times P_{dLS3} + Z_{thLS} \times P_{dLS4} + T_{amb}$

Note: Calculation is valid in any dynamic operating condition. Pd values set by user.

Figure 40. SO-28 HSD thermal impedance junction ambient single pulse

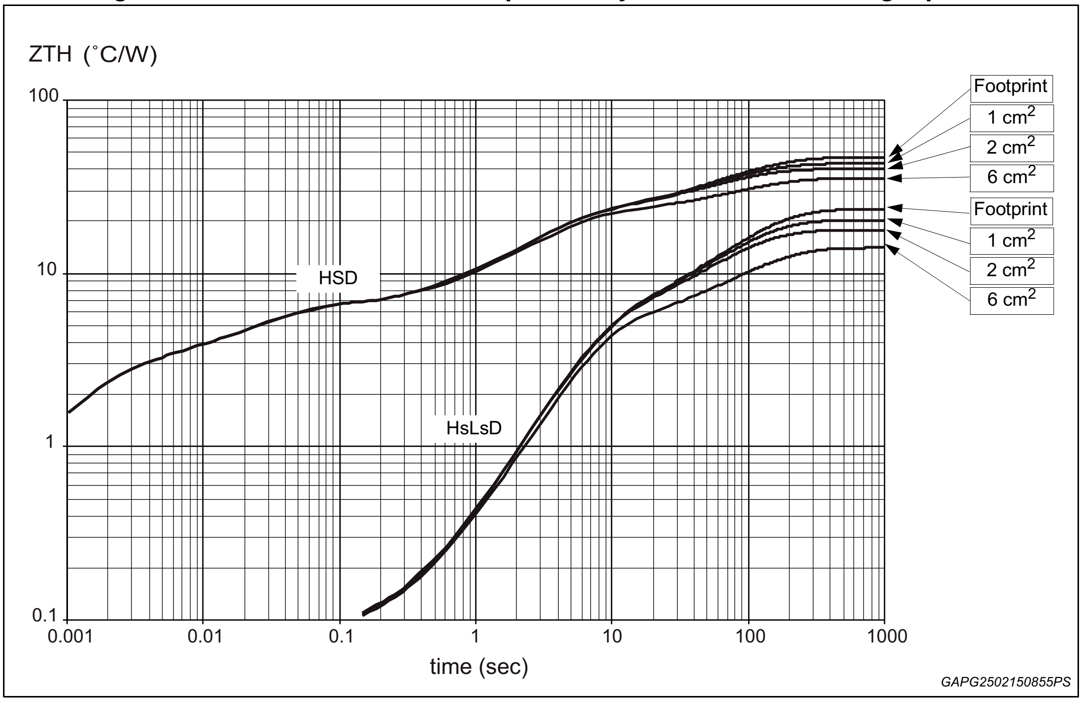
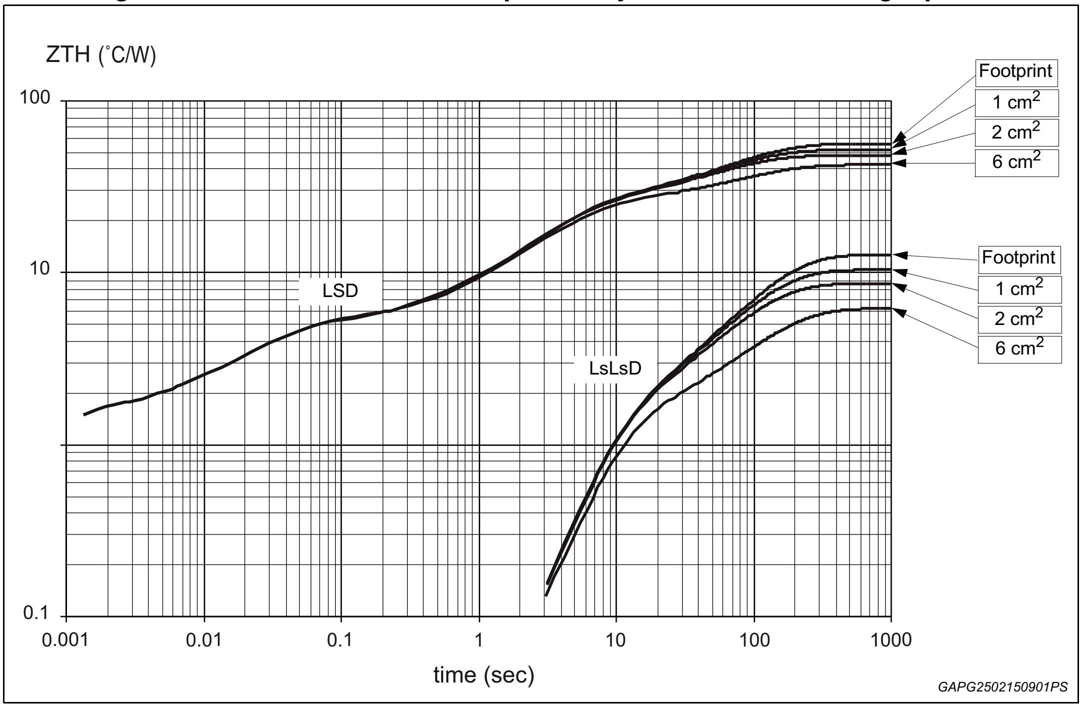


Figure 41. SO-28 LSD thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 42. Thermal fitting model of an H-bridge in SO-28

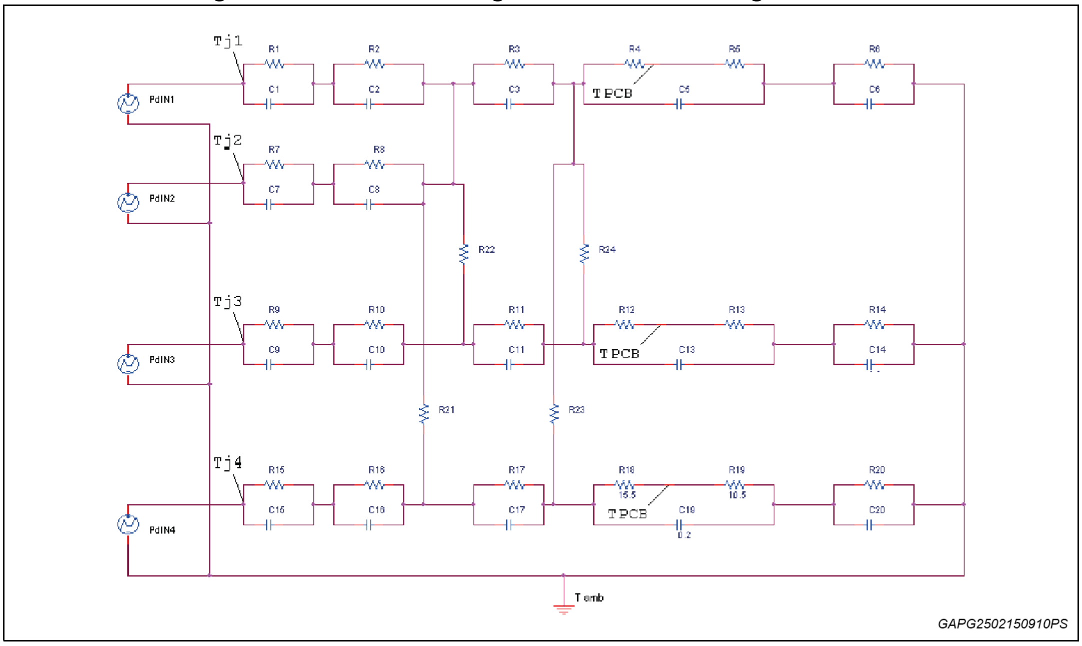


Table 21. Thermal parameters

Area/island (cm^2)	Footprint	1	2	6
R1 = R7 (°C/W)	1			
R2 = R8 (°C/W)	1.8			
R3 = R11 = R17 (°C/W)	3.5			
R4 (°C/W)	13.5			
R5 = R13 = R19 (°C/W)	10.5			
R6 = R14 = R20 (°C/W)	62.28	52.28	44.28	32.28
R9 = R15 (°C/W)	0.24			
R10 = R16 (°C/W)	1.2			
R12 (°C/W)	15.2			
R18 (°C/W)	15.5			
R21 = R22 = R23 (°C/W)	150			
R24 (°C/W)	150	52.28	44.28	32.28
C1 = C7 (W·s/°C)	0.0008			
C2 = C8 (W·s/°C)	0.001			
C3 = C11 = C17 (W·s/°C)	0.008			
C5 = C13 = C19 (W·s/°C)	0.2			
C6 = C14 = C20 (W·s/°C)	1.6	1.61	1.7	3.25
C9 = C15 (W·s/°C)	0.00015			
C10 = C16 (W·s/°C)	0.0005			

Note: A blank space means that the value is the same as the previous one.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 SO-28 package information

Figure 43. SO-28 package outline

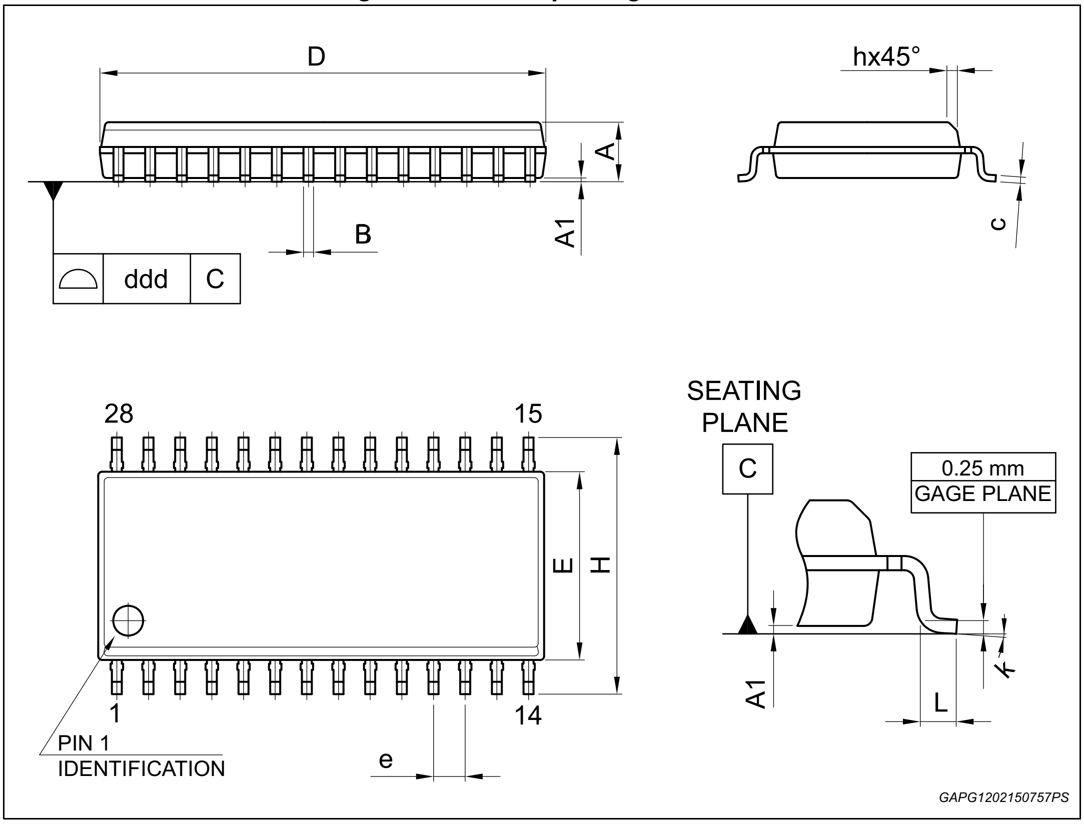


Table 22. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D(1)	17.70		18.10

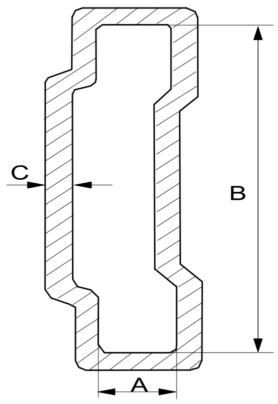
Table 22. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

7.2 SO-28 packing information

Figure 44. SO-28 tube shipment (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

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Figure 45. Reel for SO-28

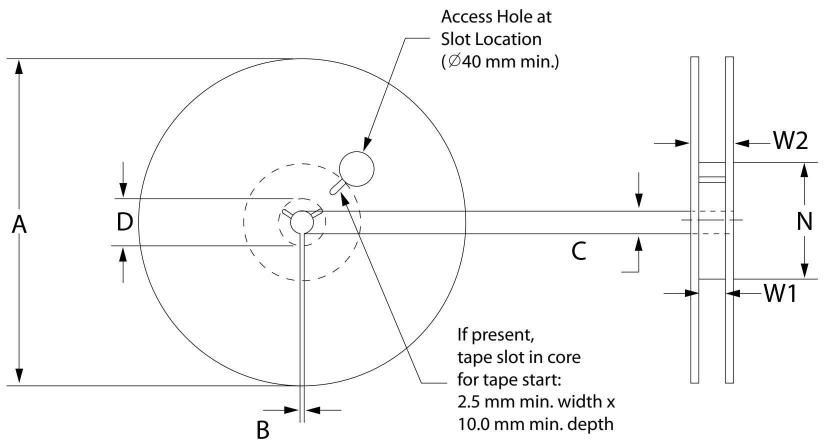

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Table 23. Reel dimensions

Description	Value[(1)]
Base quantity	1000
Bulk quantity	1000
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2/ -0)	24.4
W2 (max)	30.4

1. All dimensions are in mm.

Figure 46. SO-28 carrier tape

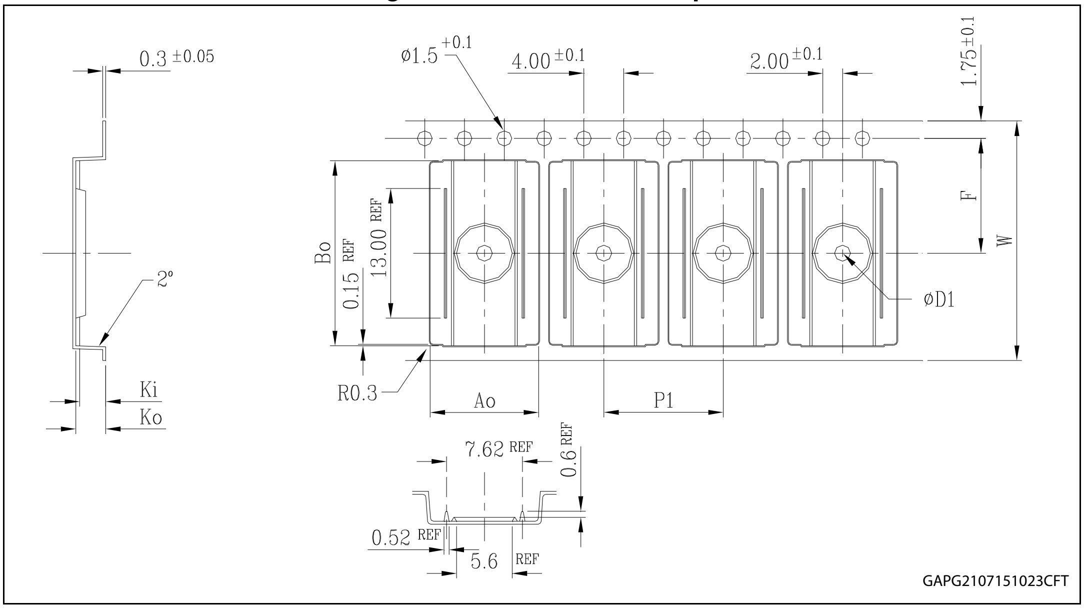
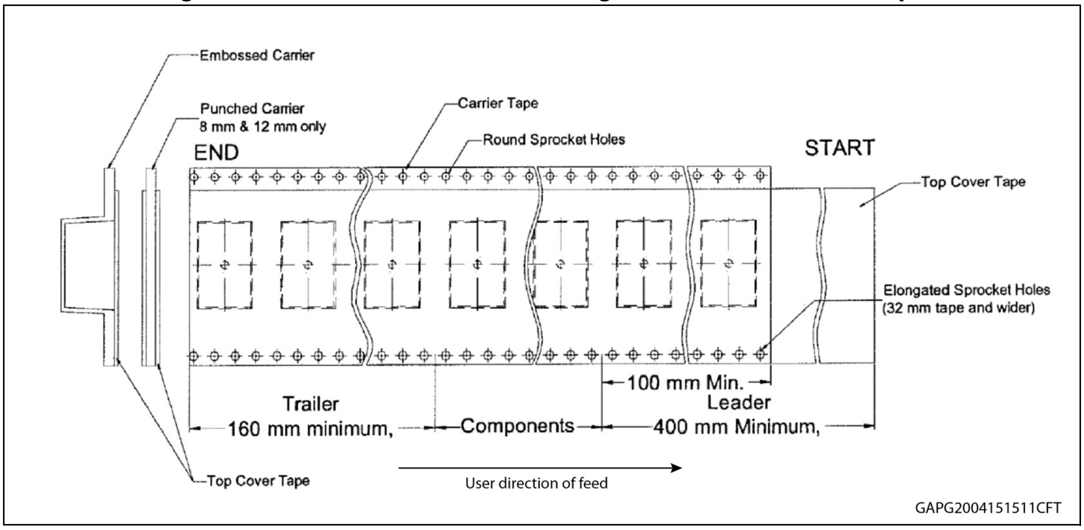


Table 24. SO-28 carrier tape dimensions

Description	Value(1)
A_0	10.90 ± 0.1
B_0	18.55 ± 0.1
K_0	3.0 ± 0.1
K_1	2.6 ± 0.1
F	11.5 ± 0.1
P_1	12.0 ± 0.1
D1	1.5 ± 0.1
W	24.0 ± 0.3

1. All dimensions are in mm.

Figure 47. SO-28 schematic drawing of leader and trailer tape



8 Order codes

Table 25. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VN5770AKP-E	VN5770AKPTR-E

9 Revision history

Table 26. Document revision history

Date	Revision	Changes
11-Nov-2010	1	Initial release.
04-Jan-2012	2	*Table 9: Current sense (8V<VCC<16V)* - K_0 values modified
20-Feb-2012	3	Update *Figure 2: Configuration diagram (top view)* and *Figure 33: Typical application schematic*
02-Oct-2012	4	*Table 9: Current sense (8V<VCC<16V)*: – K_0: updated values
23-Sep-2013	5	Updated Disclaimer Fixed order code value on the cover page and *Table 25: Device summary*
25-Feb-2015	6	Updated: – *Section 7.1: SO-28 package information*; – Tape dimensions in *Figure 8: Order codes on page 35*.
21-Jul-2015	7	Updated *Section 7.2: SO-28 packing information*