Contents

1 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	7	V
V_{id}	Differential input voltage[2]	±1	V
V_i	Input voltage	V_{CC-} -0.3 to V_{CC+} +0.3	V
T_{oper}	Operating free-air temperature range	-40 to + 125	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient [3] SOT23-5 miniSO-8 SO-8 SO-14 TSSOP8 TSSOP14	 250 190 125 103 120 100	°C/W
R_{thjc}	Thermal resistance junction to case SOT23-5 miniSO-8 SO-8 SO-14 TSSOP8 TSSOP14	 81 39 40 31 37 32	°C/W
ESD	HBM: human body model[4]	2	kV
	MM: machine model[5]	200	V
	CDM: charged device model[6]	1.5	kV
	Lead temperature (soldering, 10sec)	250	°C
	Output short-circuit duration	See note[7]	

1. All voltage values, except differential voltages, are with respect to network terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. If V_{id} > ±1 V, the maximum input current must not exceed ±1 mA. When V_{id} > ±1 V, add an input series resistor to limit the input current.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
4. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
5. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
6. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.
7. Short-circuits from the output to V_{CC} can cause excessive heating. The maximum output current is approximately 48 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 6	V
V_{icm}	Common-mode input voltage range T_{op} = 25°C, 1.8 ≤ V_{CC} ≤ 6 V T_{min} < T_{op} < T_{max}, 1.8 ≤ V_{CC} ≤ 5.5 V	 V_{CC-} - 0.2 to V_{CC+} + 0.2 V_{CC-} to V_{CC+}	V
T_{oper}	Operating free-air temperature range	-40 to + 125	°C

2 Electrical characteristics

Table 4. Electrical characteristics measured at V_{CC+} = +1.8 V, V_{CC-} = 0 V, with C_L and R_L connected to $V_{CC}/2$, T_{amb} = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	TS1851/2/4 $T_{min} \leq T_{amb} \leq T_{max}$ TS1851A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$		0.1	3 6 1 1.5	mV
ΔV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ (2) $T_{min} \leq T_{amb} \leq T_{max}$		1	9 25	nA
I_{ib}	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ (2) $T_{min} \leq T_{amb} \leq T_{max}$		10	50 80	nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	$0 \leq V_{icm} \leq V_{CC}$ $T_{min} \leq T_{amb} \leq T_{max}$	55 52	85		dB
A_{vd}	Large signal voltage gain	V_{out} = 0.5 to 1.3 V R_L = 10 kΩ R_L = 2 kΩ	 80 70	 100 100		dB
V_{OH}	High level output voltage	V_{id} = 100 mV R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 2 kΩ	 1.7 1.65 1.7 1.65	 1.77 1.7		V
V_{OL}	Low level output voltage	V_{id} = -100 mV R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 2 kΩ		 40 62	 70 90 100 120	mV
I_o	Output source current	V_{id} = 100 mV, $V_O = V_{CC-}$ at T_{amb}	15	29		mA
		at $T_{min} \leq T_{amb} \leq T_{max}$	5	5		
	Output sink current	V_{id} = -100 mV, $V_O = V_{CC+}$, at T_{amb}	15	46		mA
		at $T_{min} \leq T_{amb} \leq T_{max}$	5			
I_{CC}	Supply current (per amplifier)	$V_{out} = V_{CC}/2$ A_{VCL} = 1, no load $T_{min} \leq T_{amb} \leq T_{max}$		120	170 200	µA
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz	300	530		kHz
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, A_V = 1	0.1	0.18		V/µs
ϕm	Phase margin	C_L = 100 pF		60		Degrees
e_n	Input voltage noise	f = 1 kHz		40		nV/√Hz
THD	Total harmonic distortion			0.01		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 5. Electrical characteristics measured at V_{CC+} = +3 V, V_{CC-} = 0 V, with C_L and R_L connected to $V_{CC}/2$, T_{amb} = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1851/2/4 $T_{min} \leq T_{amb} \leq T_{max}$ TS1851A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$		0.1	3 6 1 1.5	mV
ΔV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ (2) $T_{min} \leq T_{amb} \leq T_{max}$		1	9 25	nA
I_{ib}	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ (2) $T_{min} \leq T_{amb} \leq T_{max}$		10	55 85	nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	$0 \leq V_{icm} \leq V_{CC}$ $T_{min} \leq T_{amb} \leq T_{max}$	60 57	90		dB
A_{vd}	Large signal voltage gain	V_{out} = 0.5 to 2.5 V R_L = 10 kΩ R_L = 2 kΩ	83 74	102 102		dB
V_{OH}	High level output voltage	V_{id} = 100 mV R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 2 kΩ	2.9 2.85 2.9 2.85	2.96 2.94		V
V_{OL}	Low level output voltage	V_{id} = -100 mV R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 2 kΩ		10 46	90 100 120 130	mV
I_o	Output source current	V_{id} = 100 mV, $V_O = V_{CC-}$, at T_{amb}	15	47		mA
		At $T_{min} \leq T_{amb} \leq T_{max}$	5			
	Output sink current	V_{id} = -100 mV, $V_O = V_{CC+}$, at T_{amb}	15	47		mA
		At $T_{min} \leq T_{amb} \leq T_{max}$	5			
I_{CC}	Supply current (per amplifier)	$V_{out} = V_{CC}/2$ A_{VCL} = 1, no load $T_{min} \leq T_{amb} \leq T_{max}$		150	200 230	µA
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz	370	600		kHz
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, A_V = 1	0.12	0.2		V/µs
ϕm	Phase margin	C_L = 100 pF		60		Degrees
e_n	Input voltage noise	f = 1 kHz		40		nV/√Hz
THD	Total harmonic distortion	V_{out} = 2 V_{pk-pk}, A_V = -1, f = 1 kHz		0.005		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 6. Electrical characteristics measured at V_{CC+} = +5 V, V_{CC-} = 0 V, with C_L and R_L connected to $V_{CC}/2$, T_{amb} = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1851/2/4 $T_{min} \leq T_{amb} \leq T_{max}$ TS1851A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$		0.1	3 6 1 1.5	mV
ΔV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ (2) $T_{min} \leq T_{amb} \leq T_{max}$		1	9 25	nA
I_{ib}	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ (2) $T_{min} \leq T_{amb} \leq T_{max}$		16	63 93	nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	$0 \leq V_{icm} \leq V_{CC}$ $T_{min} \leq T_{amb} \leq T_{max}$	65 62	95		dB
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{CC} = 1.8 to 5 V	70	90		dB
A_{vd}	Large signal voltage gain	V_{out} = 0.5 to 4 V R_L = 10 kΩ R_L = 2 kΩ	85 77	104 104		dB
V_{OH}	High level output voltage	V_{id} = 100 mV R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 2 kΩ	4.85 4.8 4.85 4.8	4.95 4.91		V
V_{OL}	Low level output voltage	V_{id} = -100 mV R_L = 10 kΩ R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10 kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 2 kΩ		40 80	180 200 180 200	mV
I_o	Output source current	V_{id} = 100 mV, $V_O = V_{CC-}$, at T_{amb}	15	48		mA
		at $T_{min} \leq T_{amb} \leq T_{max}$	5			
	Output sink current	V_{id} = -100 mV, $V_O = V_{CC+}$, at T_{amb}	15	48		mA
		at $T_{min} \leq T_{amb} \leq T_{max}$	5			
I_{CC}	Supply current (per amplifier)	$V_{out} = V_{CC}/2$ A_{VCL} = 1, no load $T_{min} \leq T_{amb} \leq T_{max}$		162	220 250	µA
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz	380	656		kHz
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, A_V = 1	0.13	0.25		V/µs
φm	Phase margin	C_L = 100 pF		60		Degrees
e_n	Input voltage noise	f = 1 kHz		40		nV/√Hz
THD	Total harmonic distortion	V_{out} = 2 V_{pk-pk}, A_V = -1, f = 1 kHz		0.01		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 1. Input offset voltage distribution

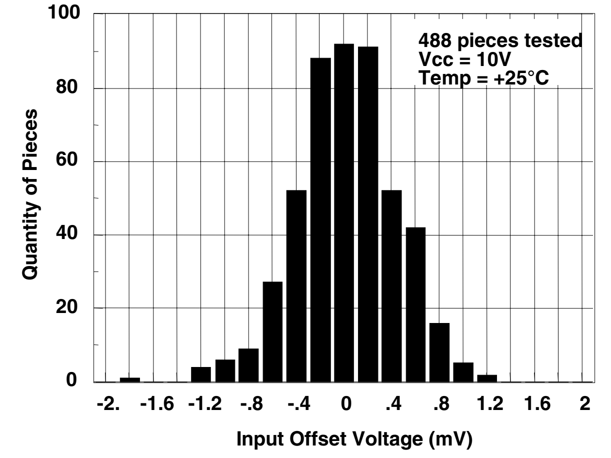


Figure 2. Input offset voltage vs. temperature

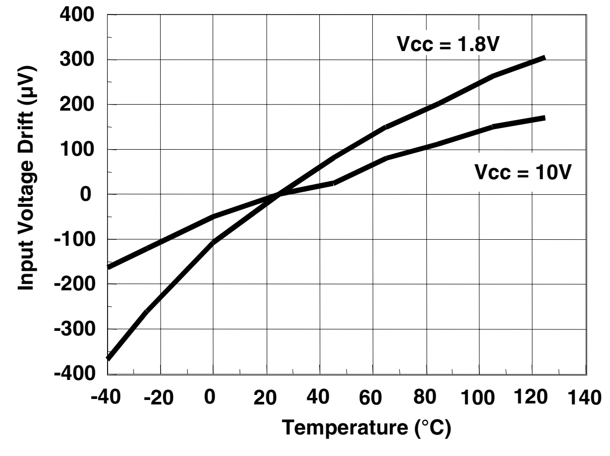


Figure 3. Input bias current vs. temperature at Vcc = 1.8 V

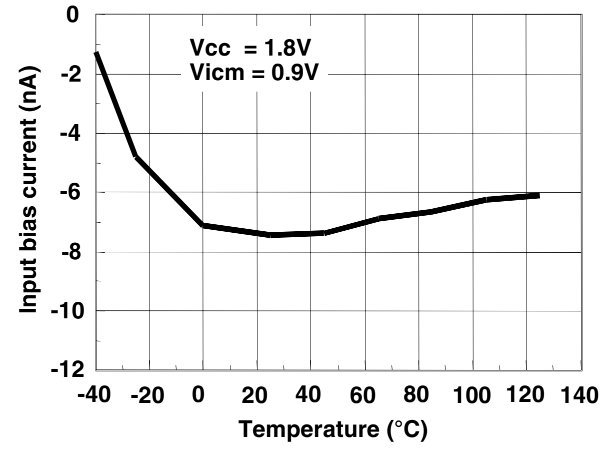


Figure 4. Input bias current vs. temperature at Vcc = 3 V

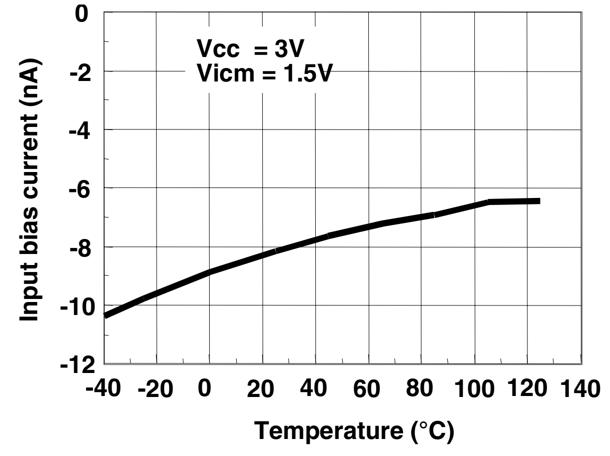


Figure 5. Input bias current vs. temperature at Vcc = 5 V

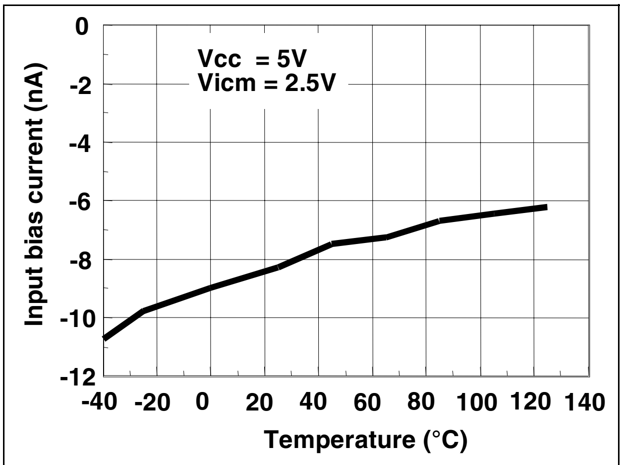


Figure 6. Supply current/amplifier vs. supply voltage

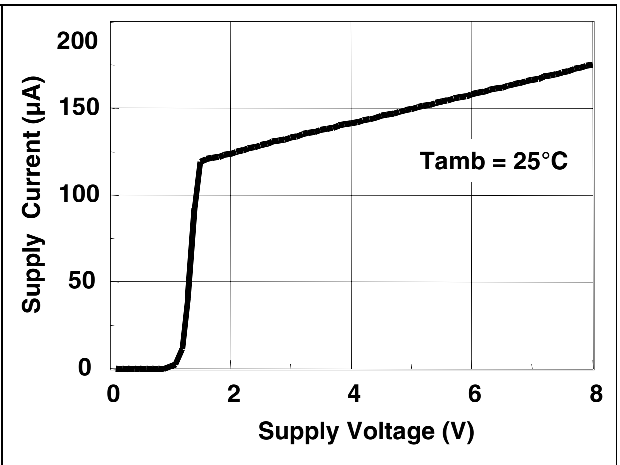


Figure 7. Supply current/amplifier vs. temperature

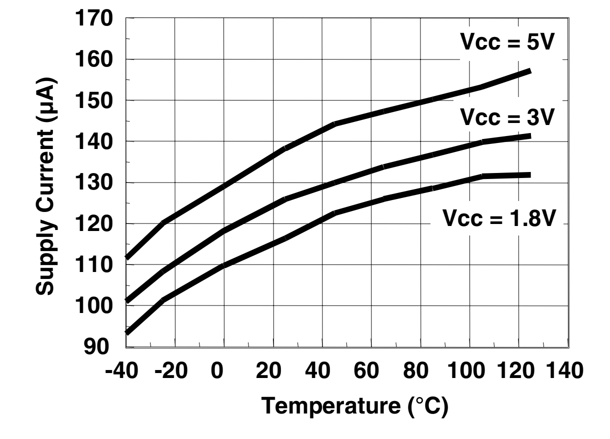


Figure 8. Common mode rejection vs. temperature at Vcc = 1.8 V

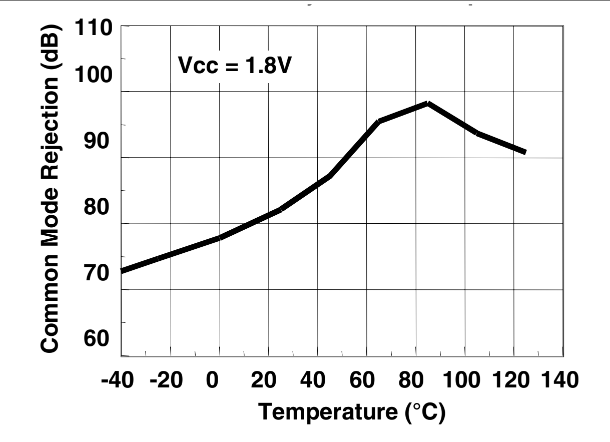


Figure 9. Common mode rejection vs. temperature at Vcc = 3 V

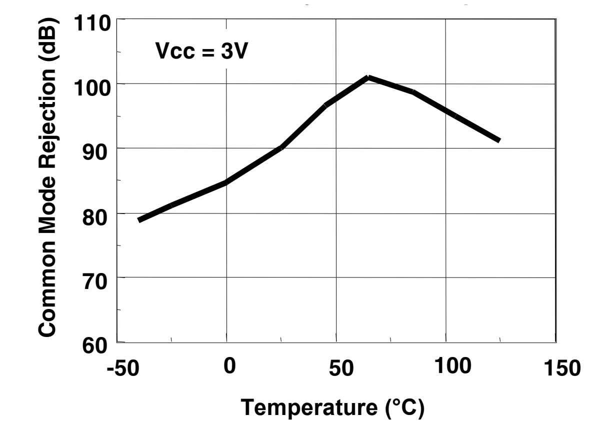


Figure 10. Common mode rejection vs. temperature at Vcc = 5 V

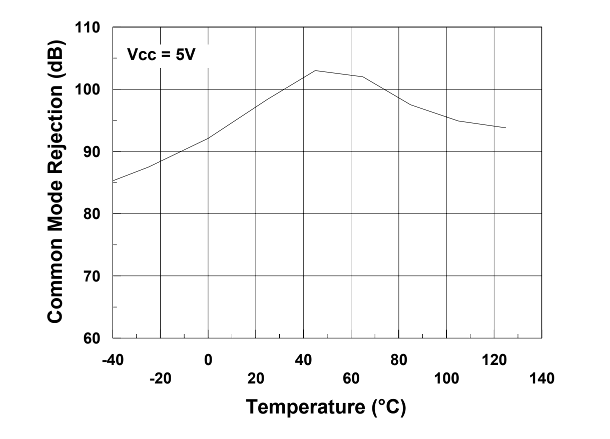


Figure 11. Supply voltage rejection vs. temperature at Vcc = 2 V

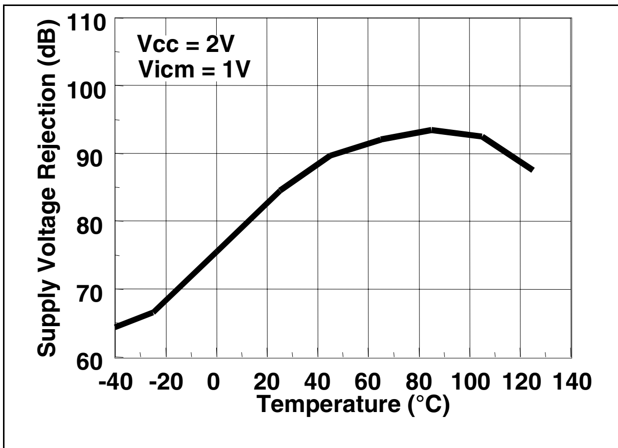


Figure 12. Supply voltage rejection vs. temperature at Vcc = 3 V

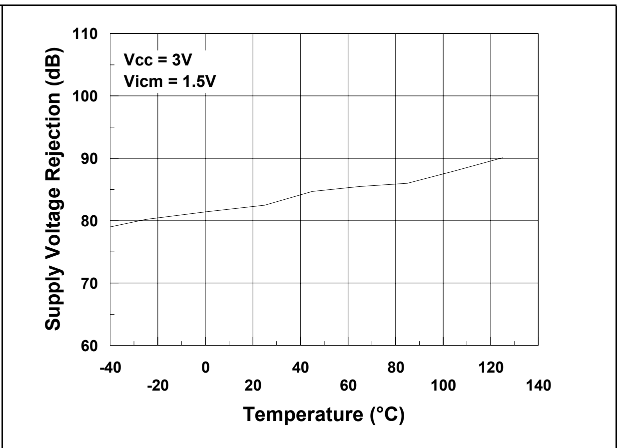


Figure 13. Supply voltage rejection vs. temperature at Vcc = 5 V

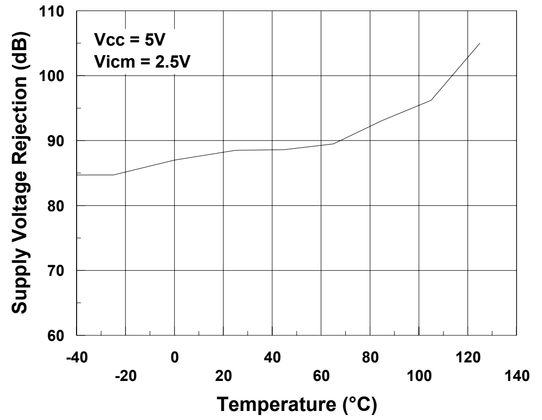


Figure 14. Open loop gain vs. temperature at Vcc = 1.8 V

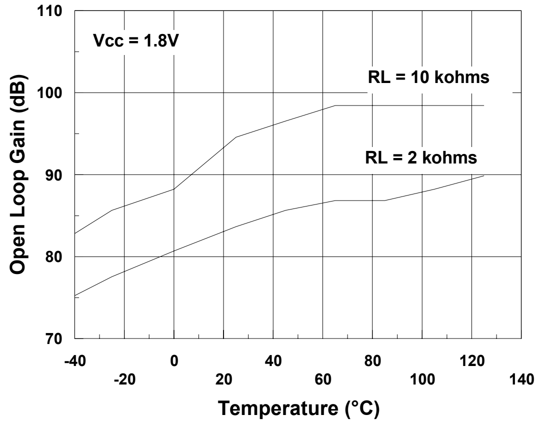


Figure 15. Open loop gain vs. temperature at Vcc = 3 V

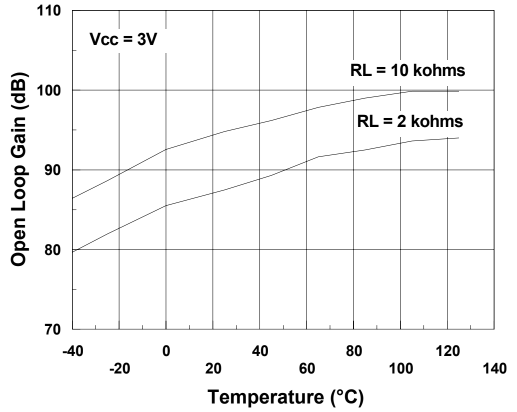


Figure 16. Open loop gain vs. temperature at Vcc = 5 V

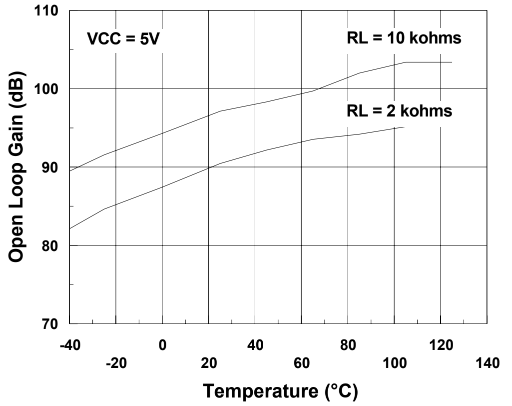


Figure 17. High level output voltage vs. temperature, R_L = 10 kΩ

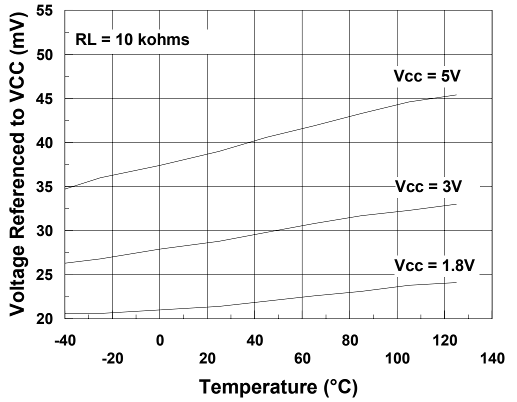


Figure 18. Low level output voltage vs. temperature, R_L = 10 kΩ

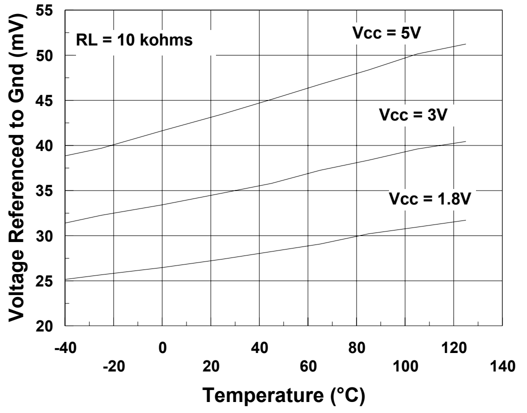


Figure 19. High level output voltage vs. temperature, R_L = 2 kΩ

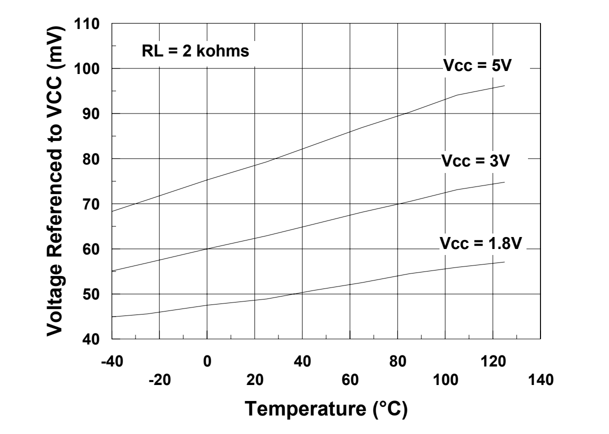


Figure 20. Low level output voltage vs. temperature, R_L = 2 kΩ

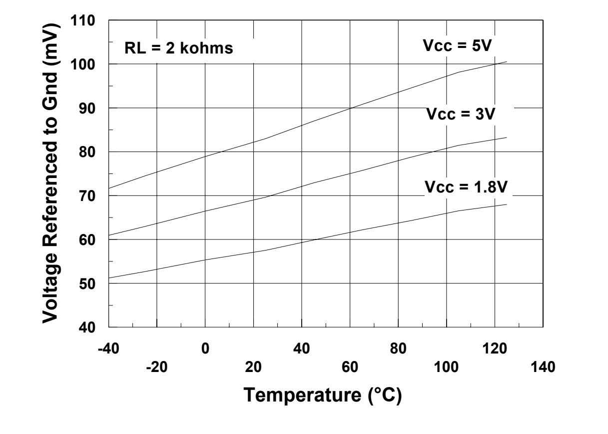


Figure 21. Output current vs. temperature

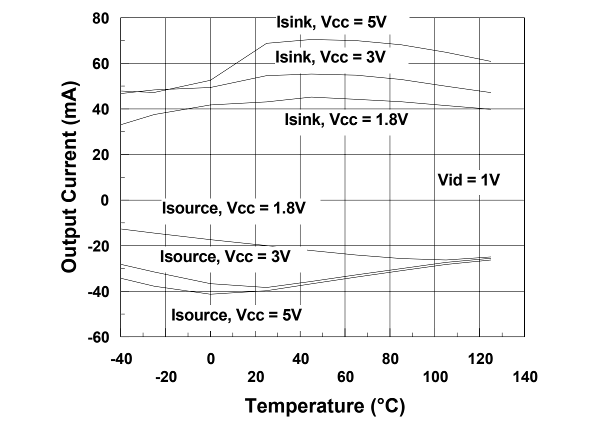


Figure 22. Output current vs. output voltage at Vcc = 1.8 V

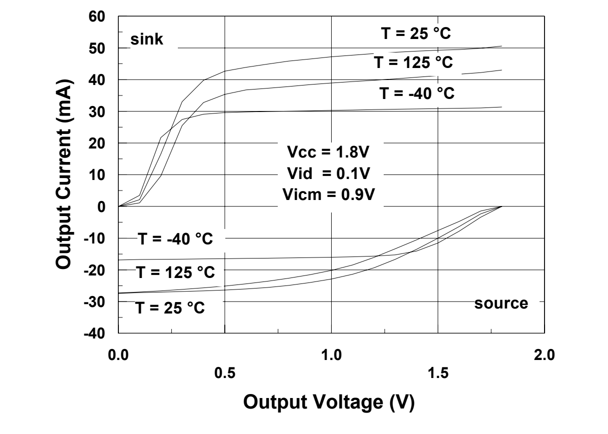


Figure 23. Output current vs. output voltage at Vcc = 3 V

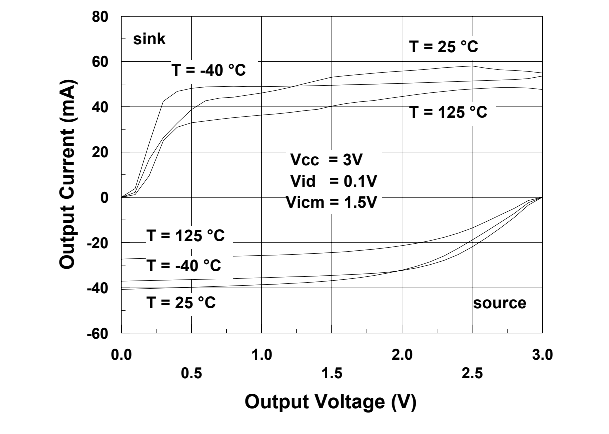


Figure 24. Output current vs. output voltage at Vcc = 5 V

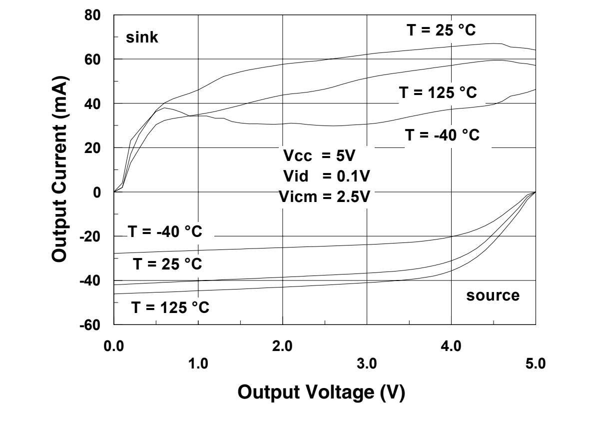


Figure 25. Gain and phase vs. frequency at V_{CC} = 1.8 V

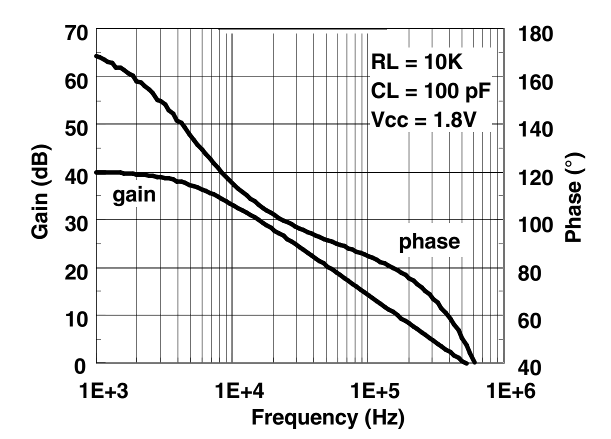


Figure 26. Gain and phase vs. frequency at V_{CC} = 5 V

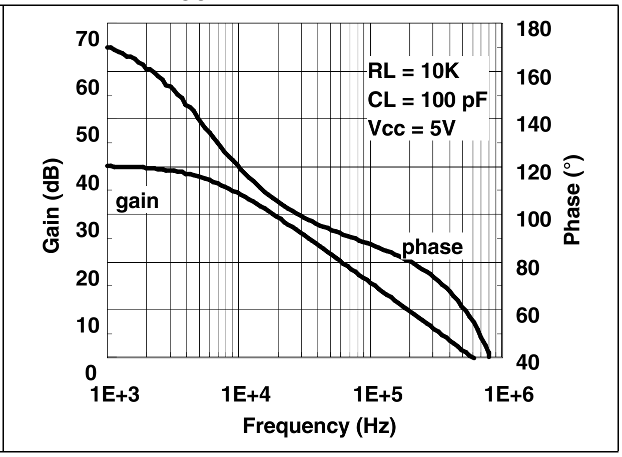


Figure 27. Gain bandwidth product vs. temperature

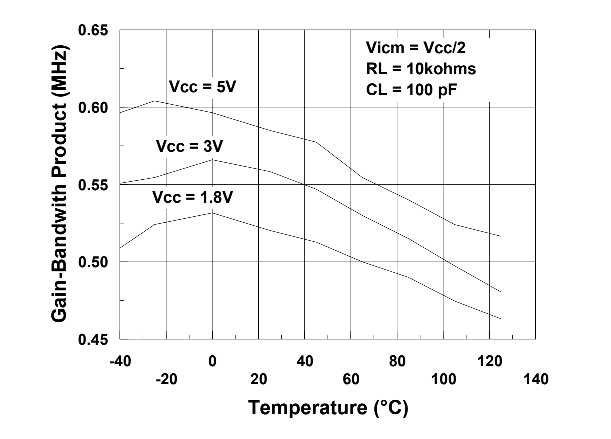


Figure 28. Gain bandwidth product vs. supply voltage

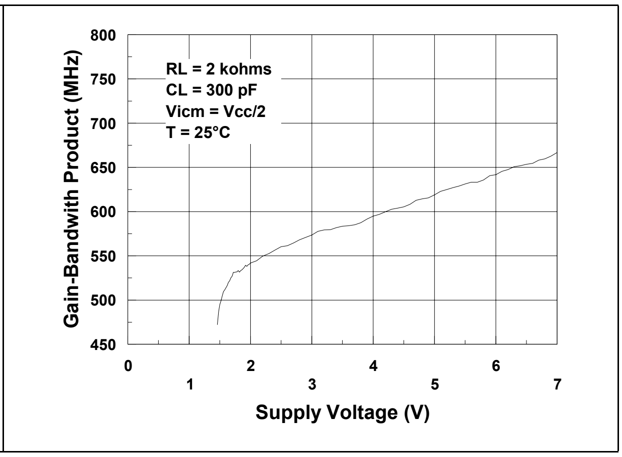


Figure 29. Slew rate vs. temperature at Vcc = 1.8 V

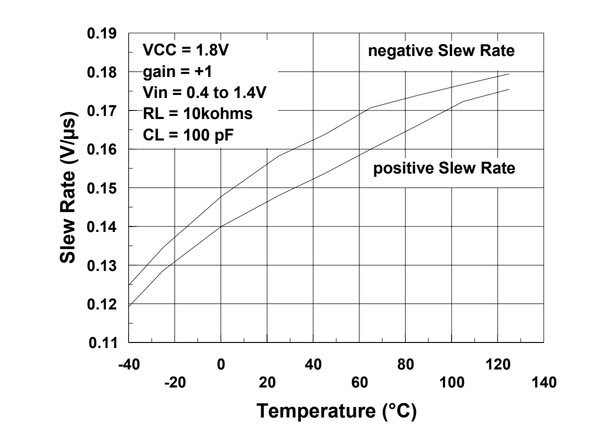


Figure 30. Slew rate vs. temperature at Vcc = 3 V

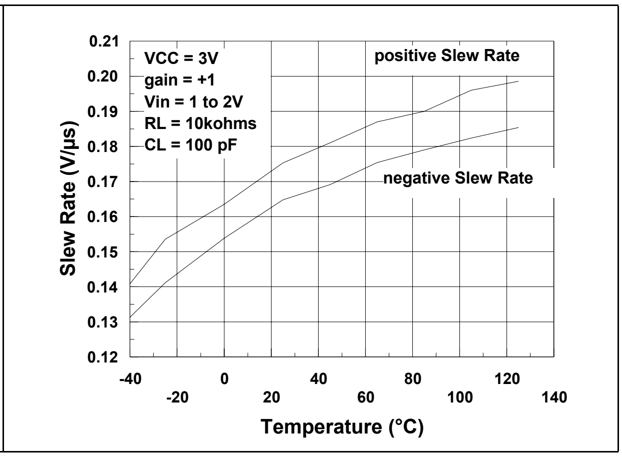


Figure 31. Slew rate vs. temperature at Vcc = 5 V

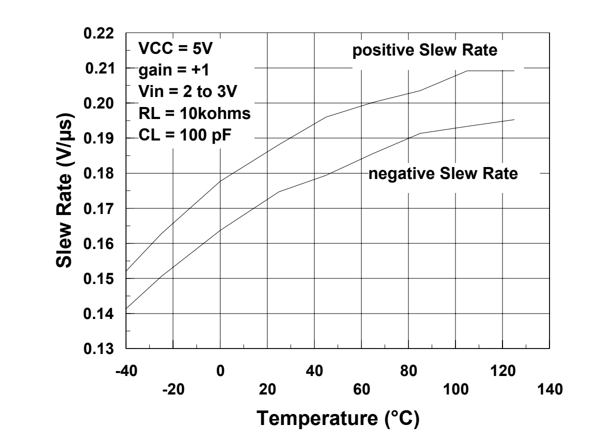


Figure 32. Phase margin vs. load capacitor

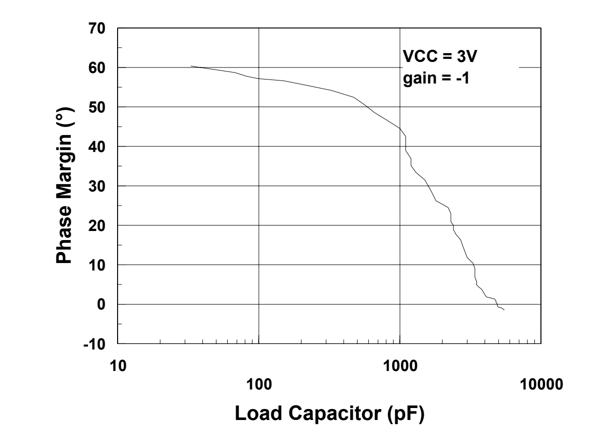


Figure 33. Phase margin vs. output current

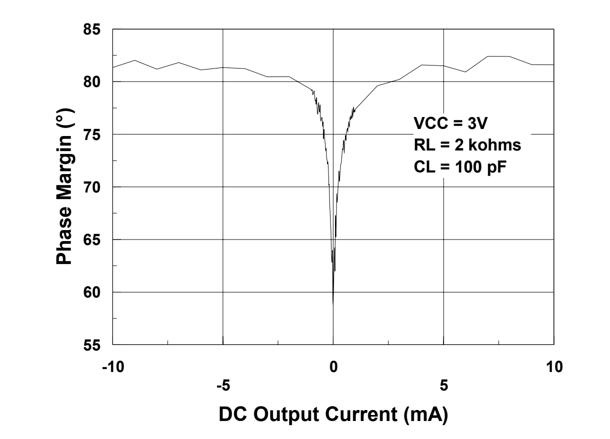


Figure 34. Equivalent input noise vs. frequency

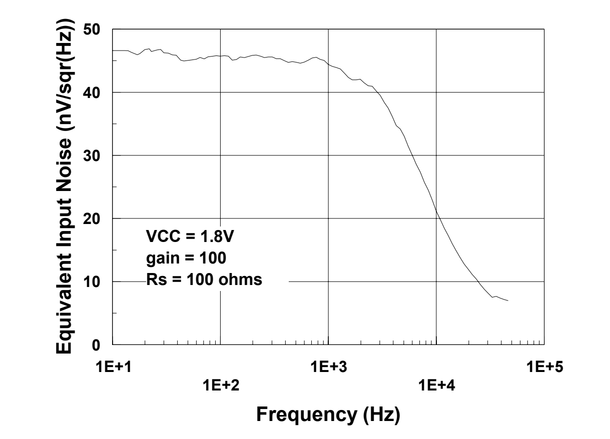


Figure 35. Distortion vs. output voltage at Vcc = 1.8 V

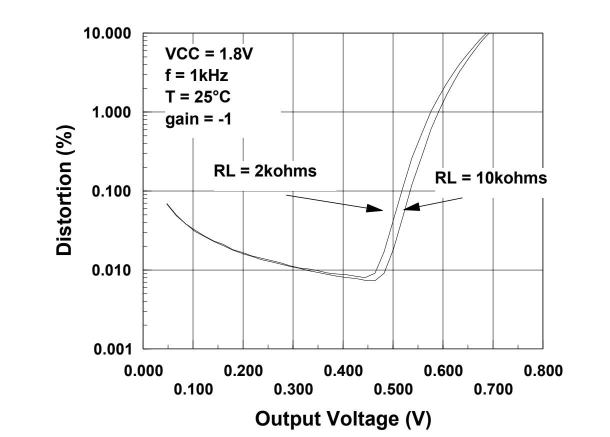


Figure 36. Distortion vs. output voltage at Vcc = 3 V

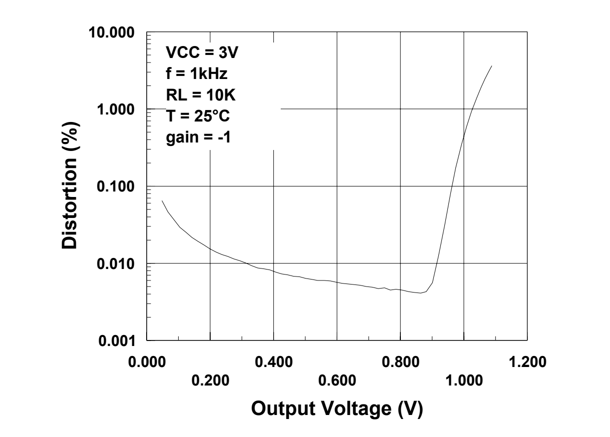


Figure 37. Distortion vs. output voltage at Vcc = 5 V

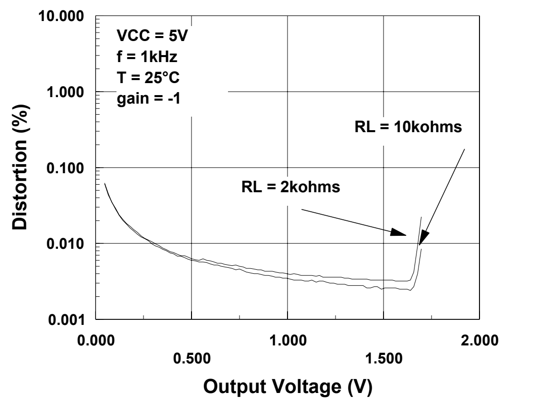
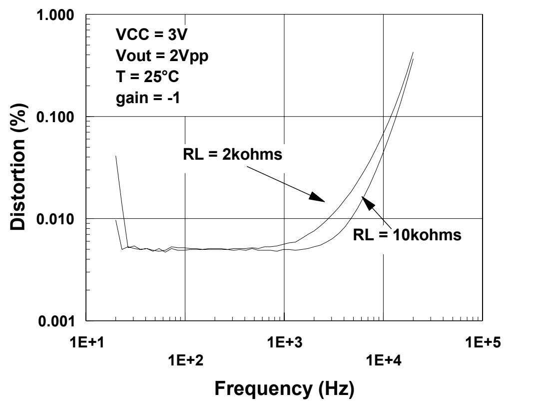


Figure 38. Distortion vs. frequency



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

3.1 SO-8 package information

Figure 39. SO-8 package mechanical drawing

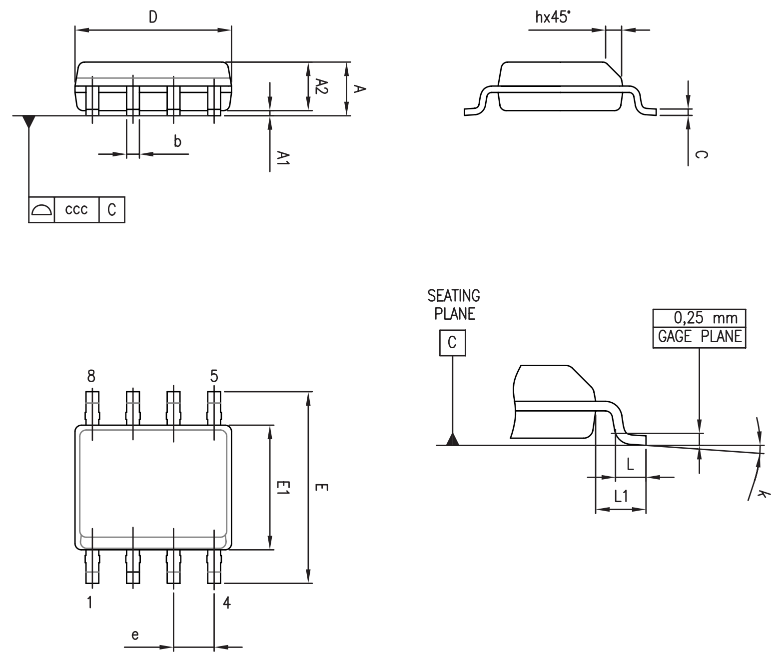


Table 7. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

3.2 TSSOP8 package information

Figure 40. TSSOP8 package mechanical drawing

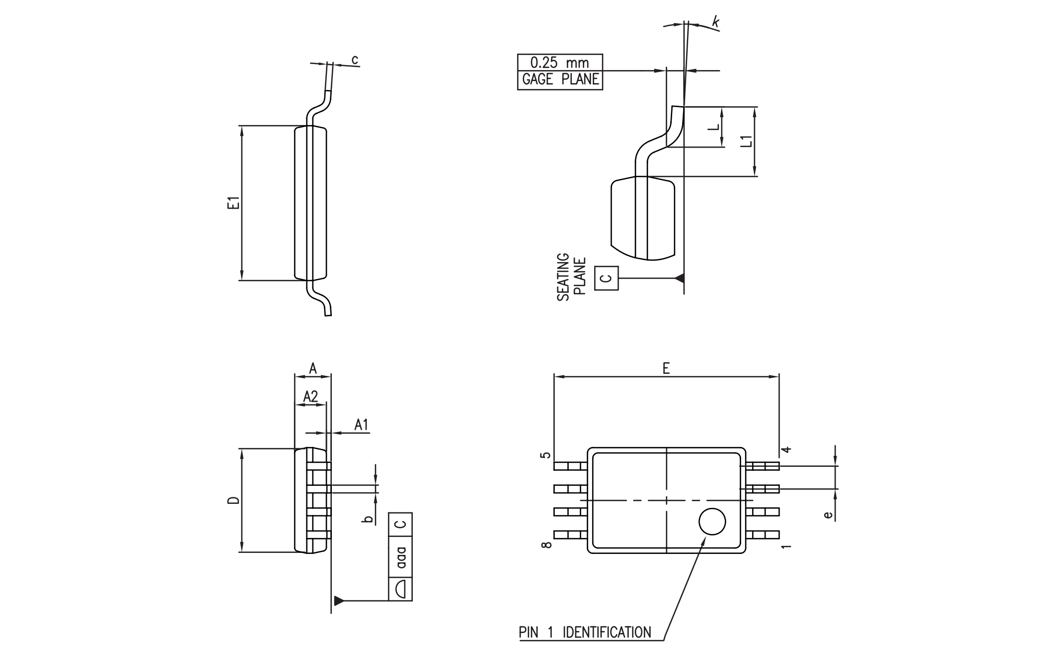


Table 8. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

3.3 MiniSO-8 package information

Figure 41. MiniSO-8 package mechanical drawing

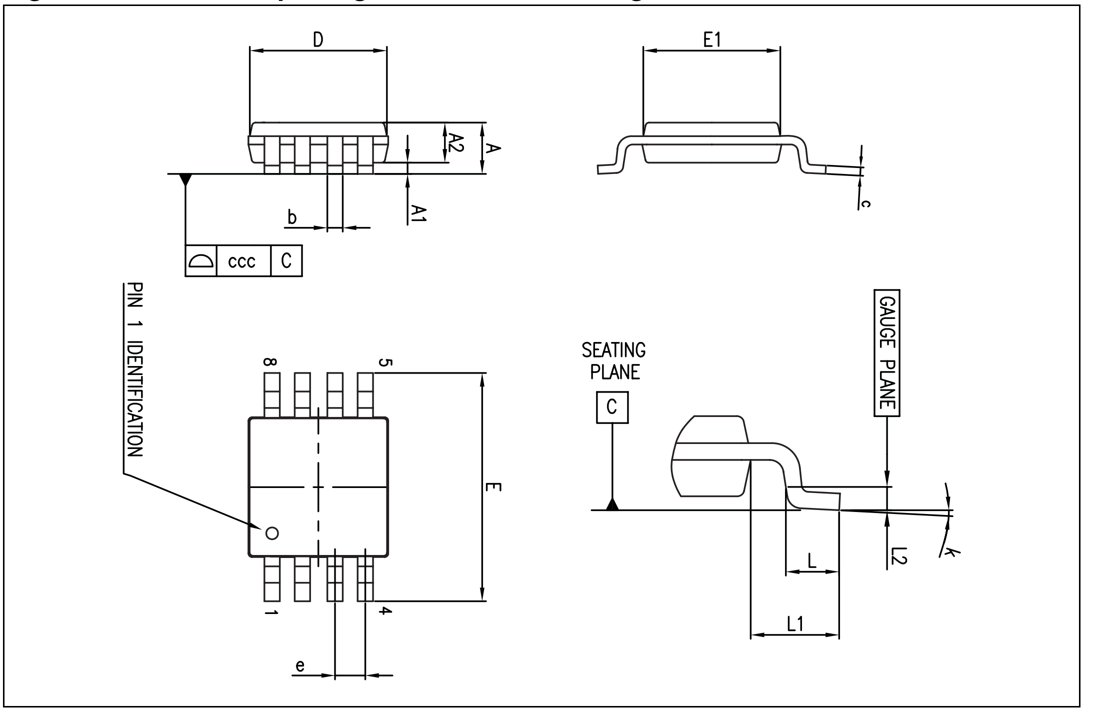


Table 9. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

3.4 SO-14 package information

Figure 42. SO-14 package mechanical drawing

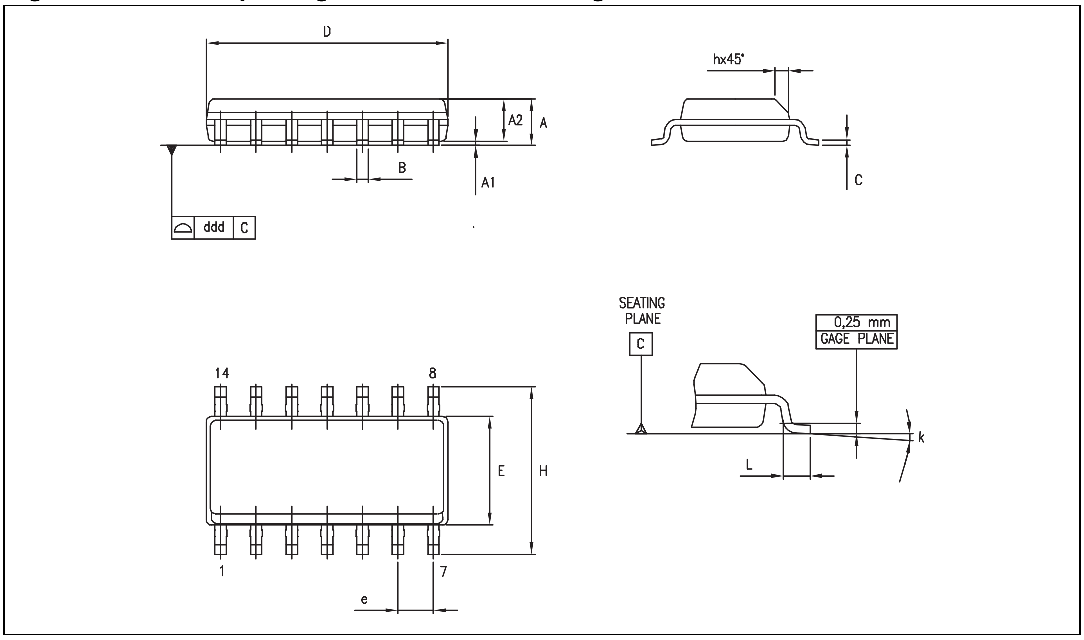


Table 10. SO-14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

3.5 TSSOP14 package information

Figure 43. TSSOP14 package mechanical drawing

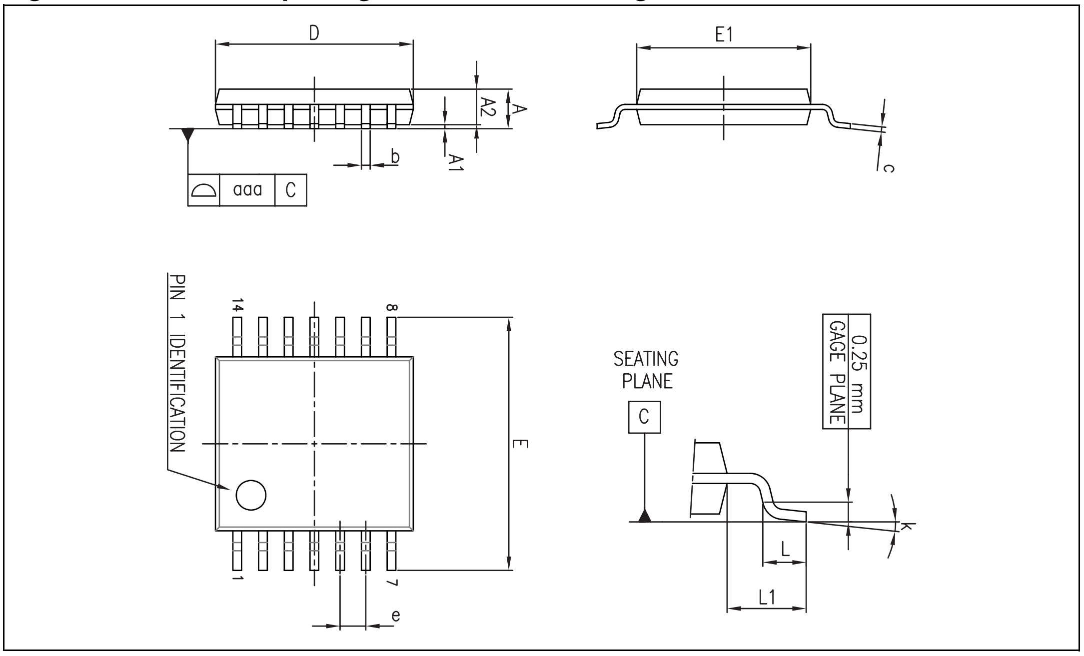


Table 11. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

3.6 SOT23-5 package information

Figure 44. SOT23-5L package mechanical drawing

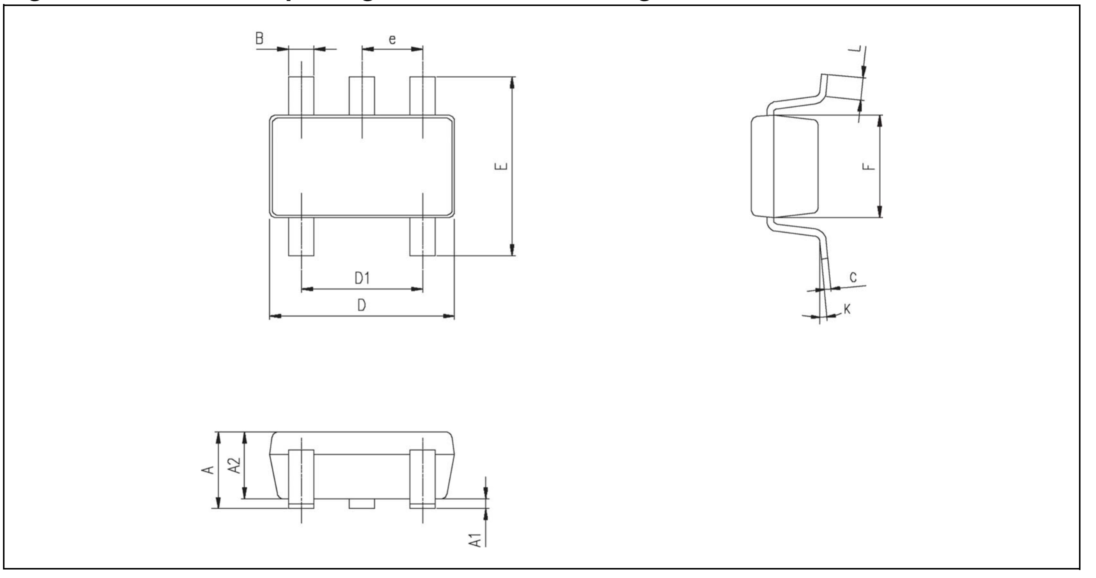


Table 12. SOT23-5L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0°		10°			

4 Ordering information

Table 13. Order codes

Order code	Temperature range	Package	Packing	Marking
TS1851ID/IDT	-40°C to +125°C	SO-8	Tube or tape & reel	1851I
TS1851IAID/AIDT				1851AI
TS1851ILT		SOT23-5L	Tape & reel	K161
TS1851AILT				K162
TS1852ID/IDT		SO-8	Tube or tape & reel	1852I
TS1852AID/AIDT				1852AI
TS1852IPT		TSSOP8 (Thin shrink outline package)	Tape & reel	1852I
TS1852AIPT				1852A
TS1852IST		MiniSO-8	Tape & reel	K161
TS1852AIST				K162
TS1854ID/IDT		SO-14	Tube or tape & reel	1854I
TS1854AID/AIDT				1854AI
TS1854IPT		TSSOP14 (Thin shrink outline package)	Tape & reel	1854I
TS1854AIPT				1854A

5 Revision history

Table 14. Document revision history

Date	Revision	Changes
01-Feb-2002	1	First release.
01-May-2005	2	Modifications on AMR *Table 2 on page 3* (explanation of V_{id} and V_i limits)
22-May-2007	3	Added limits in temperature in *Table 4*, *Table 5*, and *Table 6*. Added SVR in *Table 6* (SVR parameter removed from *Table 4* and *Table 5*). Added equivalent input voltage noise in *Table 4*, *Table 5*, and *Table 6*. Added R_{thjc} values in *Table 2 on page 3*. Updated *Table 13: Order codes*.
12-Mar-2010	4	Updated document format. Modified headings, added root part number TS185xA and added *Table 1: Device summary* on cover page. Modified Iout parameters in temperature, added limits at Tamb and improved typical values of A_{vd} in *Table 4*, *Table 5* and *Table 6*. Updated package information in *Chapter 3*. Removed order codes for DIP package from *Table 13*.