Typical Application Circuit

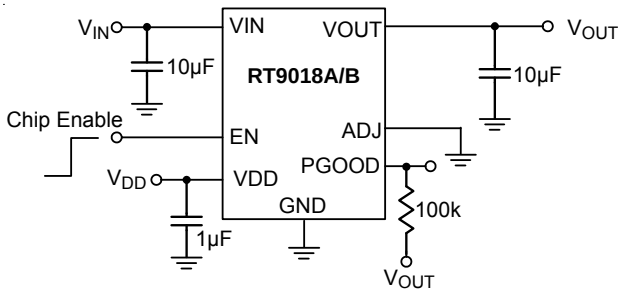


Figure 1. Fixed Voltage Regulator

$$V_{OUT} = 0.8 \times \frac{R1+R2}{R2}$$

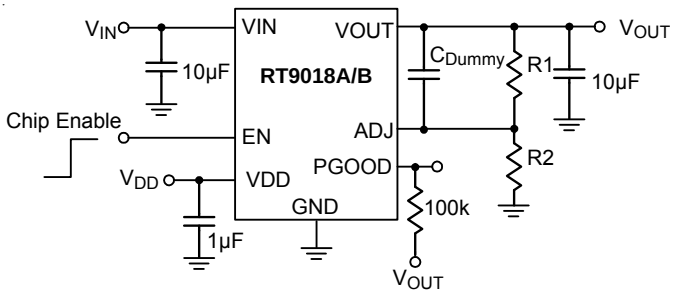
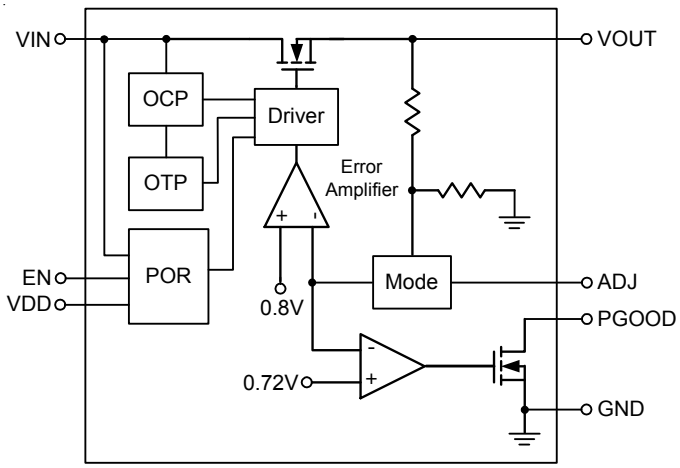


Figure 2. Adjustable Voltage Regulator

Function Pin Description

Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-10L 3x3		
3	7, 8, 9	VIN	Supply Input Voltage.
2	6	EN	Chip Enable (Active-High).
4	10	VDD	Supply Voltage of Control Circuitry.
1	5	PGOOD	Power Good Open Drain Output.
7	4	ADJ	Set the output voltage by the internal feedback resistors when ADJ is grounded. If external feedback resistors is used, V_{OUT} = 0.8V x (R1 + R2)/R2.
6	1, 2, 3	VOUT	Output Voltage.
5	--	NC	No Internal Connection.
8, 9 (Exposed Pad)	11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- 1V to 6V
- Control Voltage, VDD ---------- 3V to 6V
- Output Voltage, VOUT ---------- 0.8 to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.33W
  WDFN-10L 3x3 ---------- 1.67W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
  WDFN-10L 3x3, θ_{JA} ---------- 60°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 1.4V to 5.5V
- Control Voltage, VDD (V_{DD} > V_{OUT} + 1.5V) ---------- 3V to 5.5V
- Control Voltage with PGOOD, VDD (Note 8) ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 500mV, V_{EN} = V_{DD} = 5V, C_{IN} = C_{OUT} = 10µF, T_A = T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POR Threshold			2.4	2.7	3	V
POR Hysteresis			0.15	0.2	--	V
Adjustable Pin Threshold	V_{TH_ADJ}	I_{OUT} = 1mA	--	0.2	0.4	V
Reference Voltage (ADJ Pin Voltage)	V_{ADJ}	I_{OUT} = 1mA	0.788	0.8	0.812	V
Fixed Output Voltage Range	ΔV_{OUT}		–1.5	0	1.5	%
Line Regulation (V_{IN})	ΔV_{LINE_IN}	V_{IN} = V_{OUT} + 0.5V to 5V, I_{OUT} = 1mA	--	0.2	0.6	%
Load Regulation (Note 5)	ΔV_{LOAD}	V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA to 3A	--	0.2	1	%
Dropout Voltage (Note 6)	V_{DROP}	I_{OUT} = 2A	--	150	250	mV
		I_{OUT} = 3A	--	210	350	
Quiescent Current (Note 7)	I_Q	V_{DD} = 5.5V	--	0.6	1.2	mA
Current Limit	I_{LIM}		3.2	4.5	--	A

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Short Circuit Current			V_{OUT} < 0.2V	0.5	1.8	--	A
In-rush Current			C_{OUT} = 10μF, Enable Start-up	--	0.6	--	A
V_{OUT} Pull Low Resistance			V_{EN} = 0V	--	150	--	Ω
Chip Enable							
EN Input Bias Current		I_{EN}	V_{EN} = 0V	--	12	--	μA
VDD Shutdown Current	RT9018A	I_{SHDN}	V_{EN} = 0V	--	10	20	μA
	RT9018B			--	--	1	
EN Threshold Voltage	Logic-Low	V_{ENL}	V_{DD} = 5V	--	--	0.7	V
	Logic-High	V_{ENH}	V_{DD} = 5V	1.2	--	--	
Power Good							
PGOOD Rising Threshold				--	90	93	%
PGOOD Hysteresis				3	10	--	%
PGOOD Sink Capability			I_{PGOOD} = 10mA	--	0.2	0.4	V
PGOOD Delay				0.5	1.5	5	ms
Thermal Protection							
Thermal Shutdown Temperature		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	°C
Thermal Shutdown Temperature Fold-back			V_{OUT} < 0.4V	--	110	--	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 1mA to 3A.

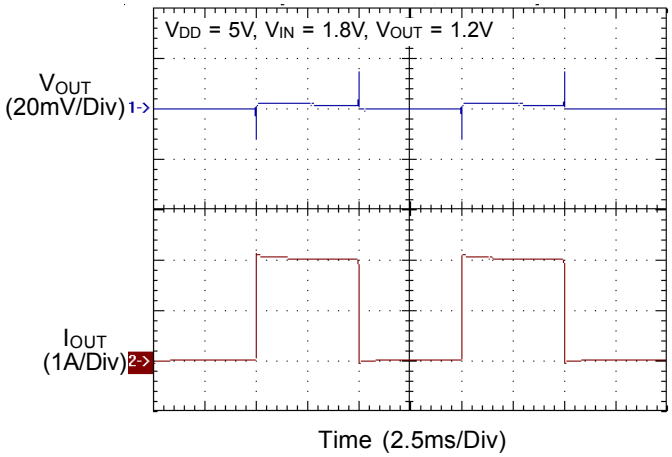
Note 6. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ - 100mV.

Note 7. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

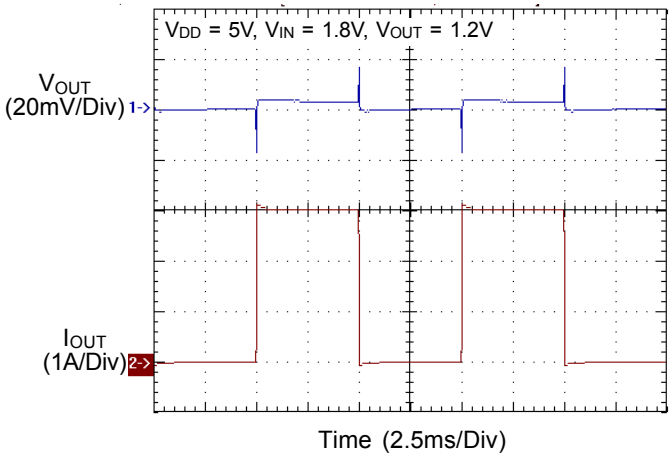
Note 8. The control voltage must within 4.5V to 5.5V when using PGOOD function.

Typical Operating Characteristics

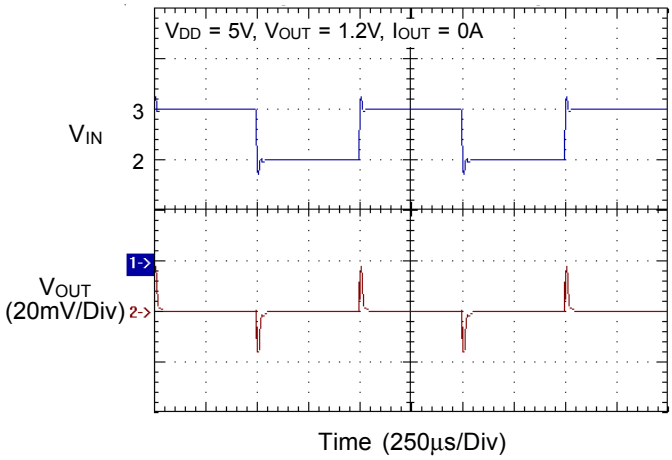
Load Transient Response



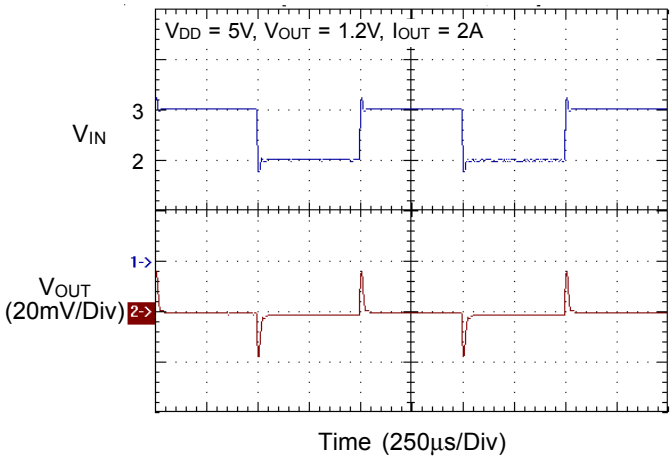
Load Transient Response



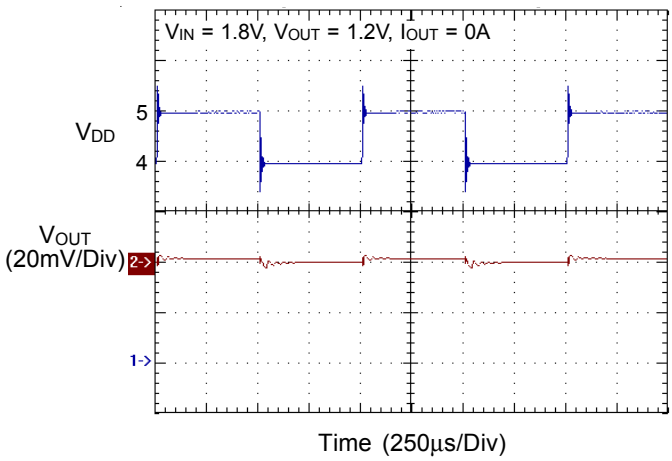
V_{IN} Line Transient Response



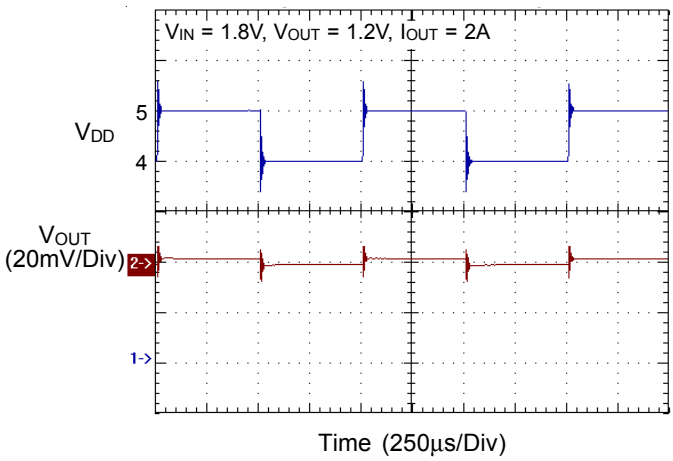
V_{IN} Line Transient Response



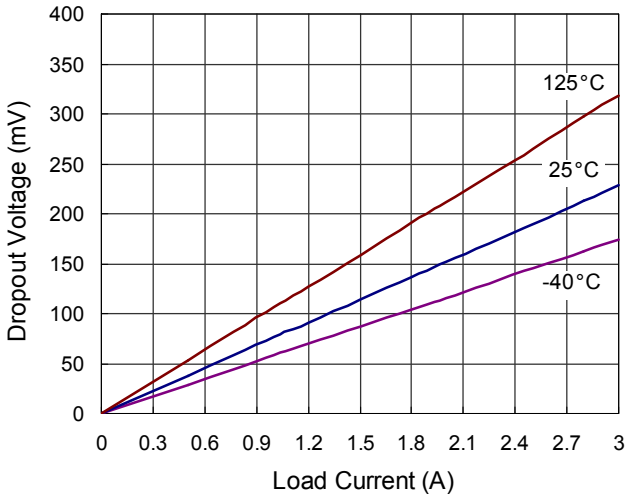
V_{DD} Line Transient Response



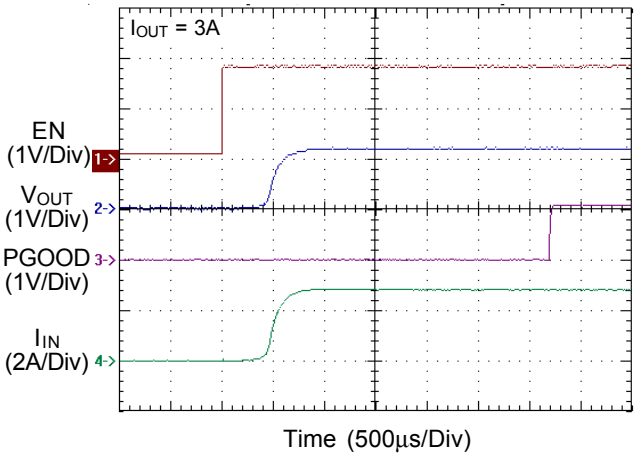
V_{DD} Line Transient Response



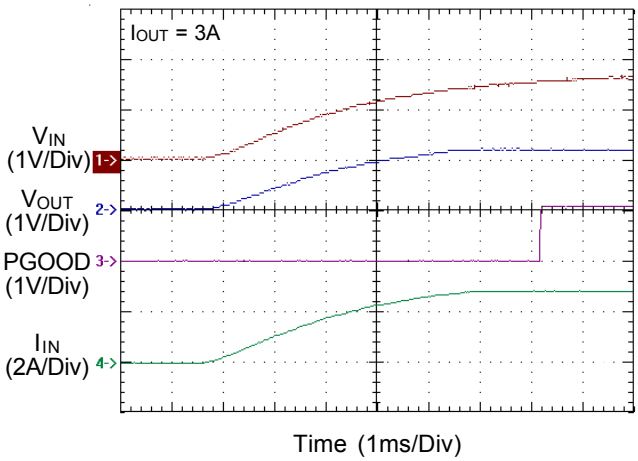
Dropout Voltage vs. Load Current



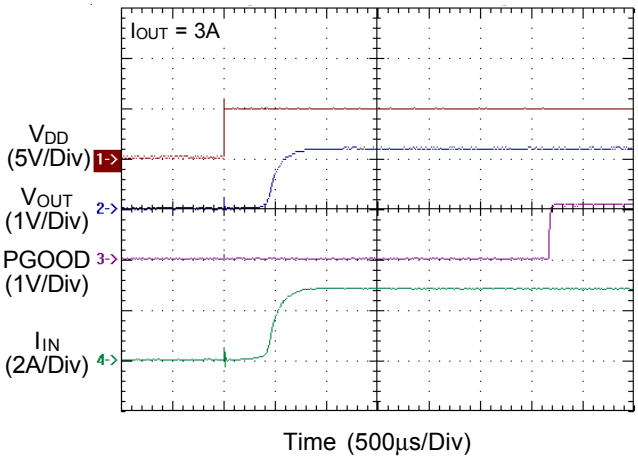
Start Up from Enable



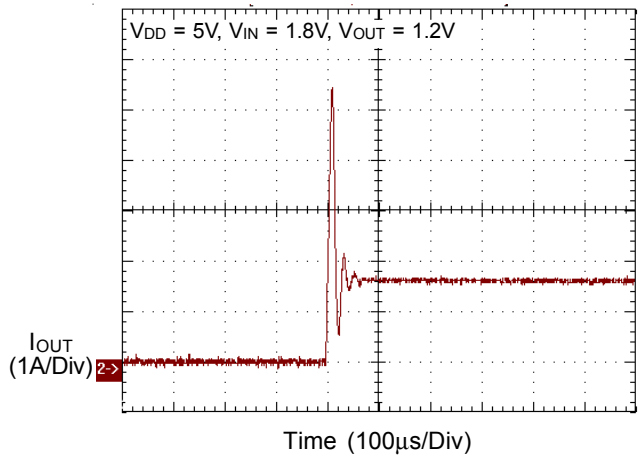
Start Up from V_{IN}



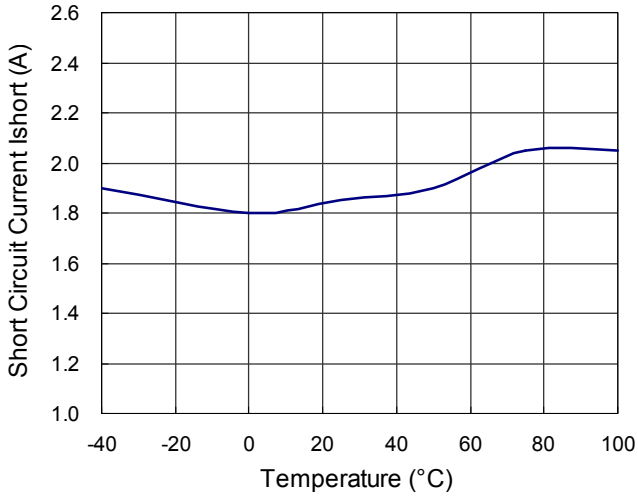
Start Up from V_{DD}



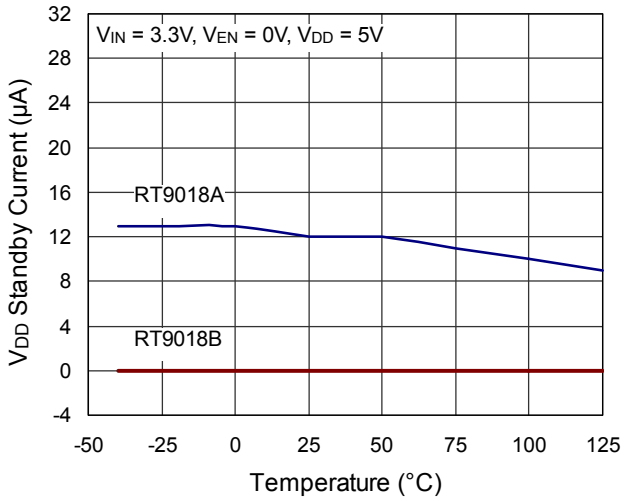
Short Circuit Protection



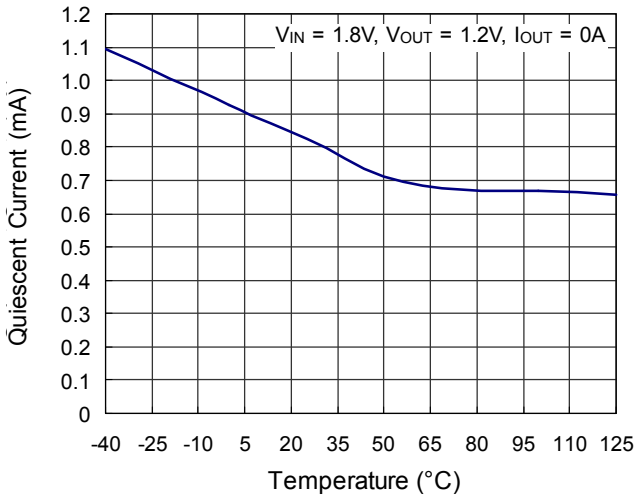
Short Circuit Current vs. Temperature



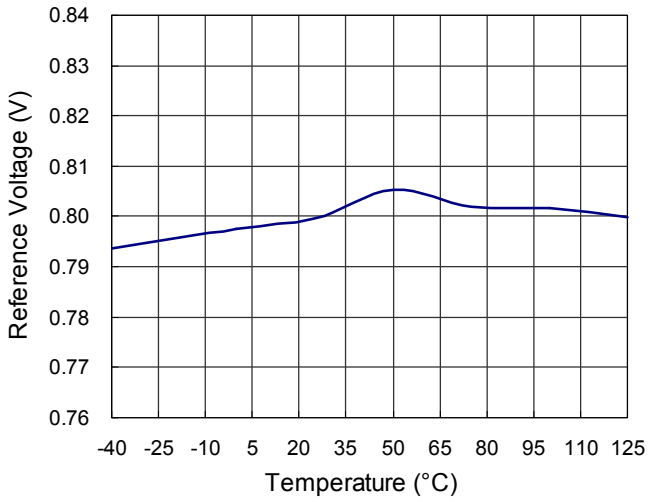
V_{DD} Standby Current vs. Temperature



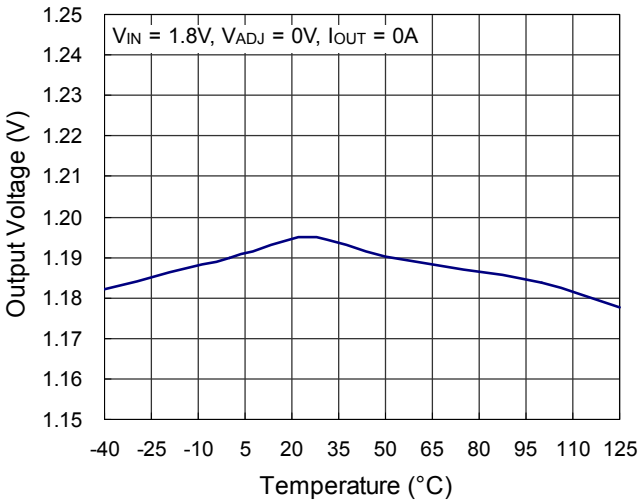
Quiescent Current vs. Temperature



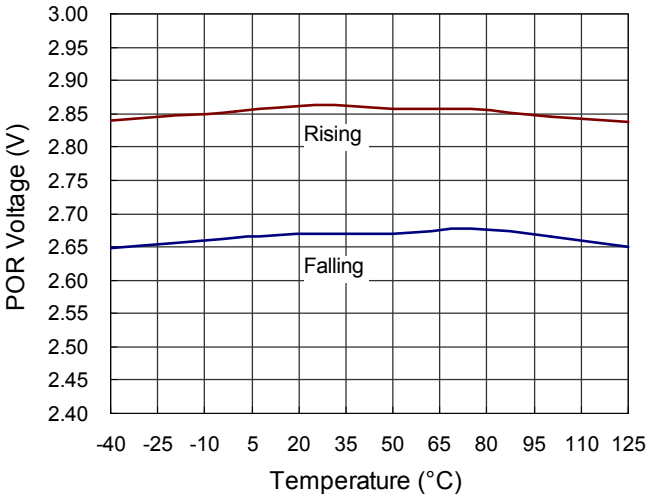
Reference Voltage vs. Temperature



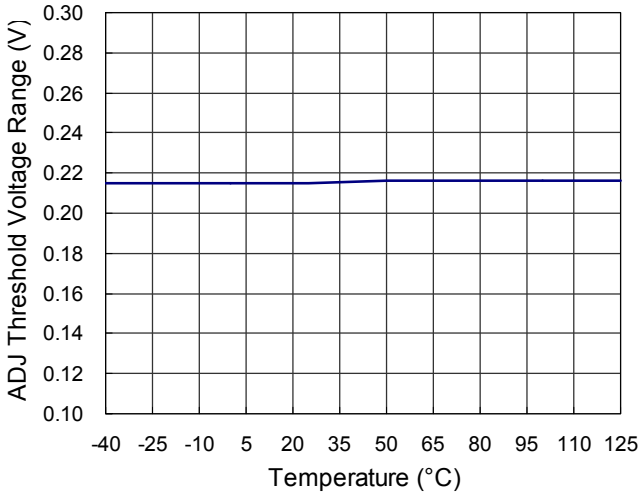
Output Voltage vs. Temperature

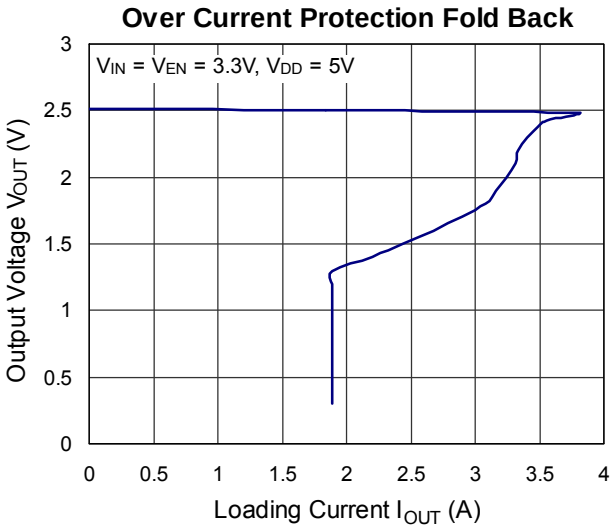


VDD POR Threshold Voltage vs. Temperature



ADJ Threshold Voltage vs. Temperature





Application Information

Adjustable Mode Operation

The output voltage of RT9018A/B is adjustable from 0.8V to (V_{IN} - V_{DROP}) by external voltage divider resisters as shown in Typical Application Circuit (Figure 2). The value of resisters R1 and R2 should be more than 10kΩ to reduce the power loss. The V_{DD} must be greater than (V_{OUT} + 1.5V).

Enable

The RT9018A/B goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 10μA typical. The RT9018A/B goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, NOTE that the RT9018A/B internal initial logic level. For RT9018A, the EN pin function pulls high level internally. So the regulator will be turn on when EN pin is floating. For RT9018B, the EN pin function pulls low level internally. So the regulator will be turn off when EN pin is floating.

Output Capacitor

The RT9018A/B is specifically designed to employ ceramic output capacitors as low as 10μF. The ceramic capacitors offer significant cost and space savings, along with high frequency noise filtering.

Input Capacitor

Good bypassing is recommended from input to ground to help improve AC performance. A 10μF input capacitor or greater located as close as possible to the IC is recommended.

Current Limit

The RT9018A/B contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor' s gate voltage, limiting the output current to higher than 4.5A typical. When the output voltage is less than 0.4V, the short circuit current protection starts the current fold back function and maintains the loading current 1.8A. The output can be shorted to ground indefinitely without damaging the part.

Power Good

The power good function is an open-drain output. Connects 100kΩ pull up resistor to VOUT to obtain an output voltage. The PGOOD pin will output high immediately after the output voltage arrives 90% of normal output voltage. The PGOOD pin will output high with typical 1.5ms delay time.

Thermal-Shutdown Protection

Thermal protection limits power dissipation to prevent IC over temperature in RT9018A/B. When the operation junction temperature exceeds 160°C, the over-temperature protection circuit starts the thermal shutdown function and turns the pass transistor off. The pass transistor turn on again after the junction temperature cools by 30°C. RT9018A/B lowers its OTP trip level from 160°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V). It limits IC case temperature under 100°C and provides maximum safety to customer while output short circuit occurring.

Power Dissipation

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, where $T_{J\,(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance for SOP-8 (Exposed Pad) package is 75°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at T_A = 25°C can be calculated by following

formula :

$P_{D\ (MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.33W (SOP-8 Exposed Pad on the minimum layout)

Layout Considerations

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design had been designed. If possible, it' s useful to increase thermal performance by the PCB design. The thermal resistance θ_{JA} can be decreased by adding a copper under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 3, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 3.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) Figure 3.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm² (Figure 3.e) reduces the θ_{JA} to 49°C/W.

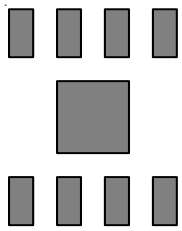


Figure 3 (a). Minimum Footprint, θ_{JA} = 75°C/W

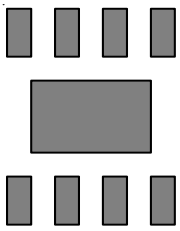


Figure 3 (b). Copper Area = 10mm², θ_{JA} = 64°C/W

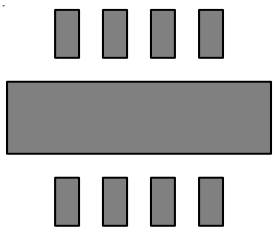


Figure 3 (c). Copper Area = 30mm², θ_{JA} = 54°C/W

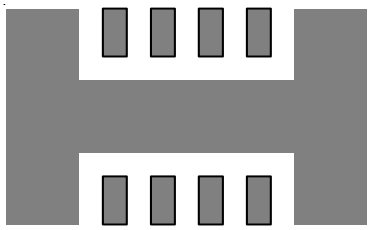


Figure 3 (d). Copper Area = 50mm², θ_{JA} = 51°C/W

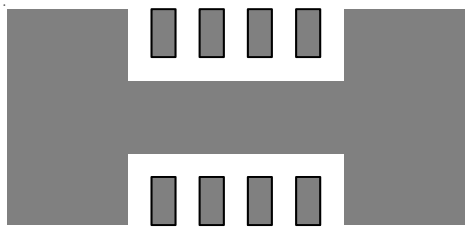


Figure 3 (e). Copper Area = 70mm², θ_{JA} = 49°C/W

Figure 3. Thermal Resistance vs. Different Cooper Area Layout Design

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 4 of de-rating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

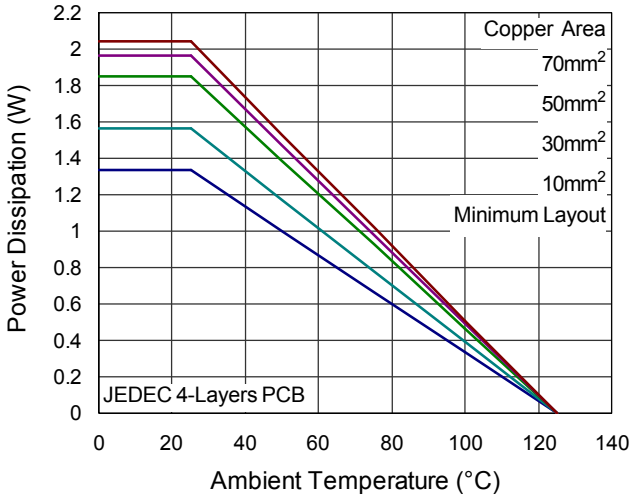
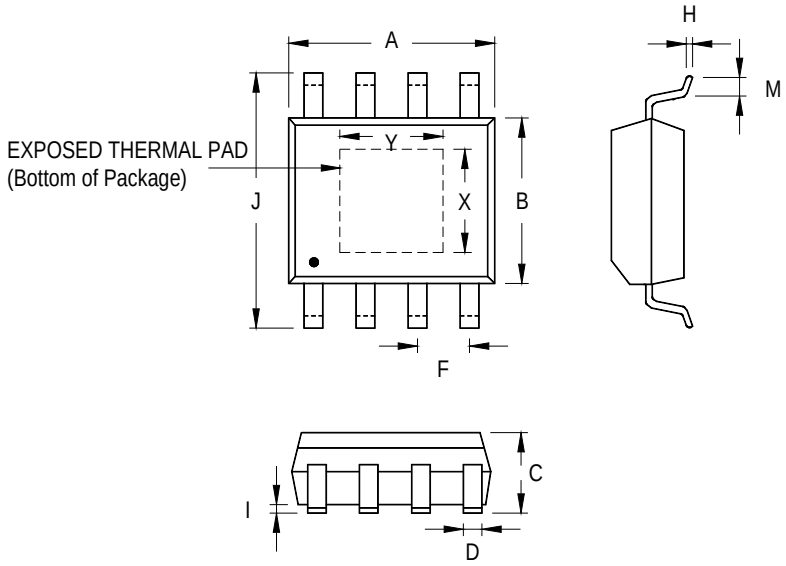


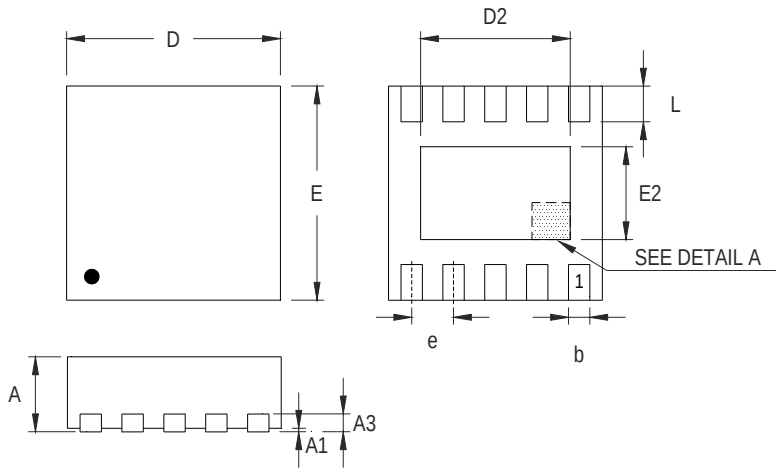
Figure 4. De-rating Curves

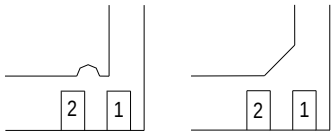
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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Hsinchu, Taiwan, R.O.C.

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