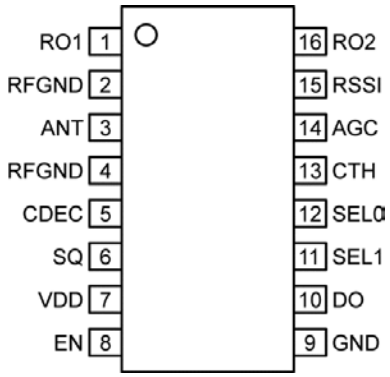
Ordering Information

Part Number	Top Marking	Junction Temperature Range	Package
MICRF230YQS	MICRF230YQS	–40°C to +105°C	16-Pin 4.9mm × 6.0mm QSOP

Pin Configuration



16-Pin 4.9mm × 6.0mm QSOP (QS)
(Top View)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	RO1	Input	Reference resonator connection (to the Pierce oscillator). Can also be driven by external reference signal of 200mV$_{P-P}$ to 1.5V$_{P-P}$ amplitude maximum. Internal capacitance of 7pF to GND during normal operation.
2	RFGND	Supply	Ground connection for ANT RF input. Connect to PCB ground plane.
3	ANT	Input	Antenna input. RF signal input from antenna. Internally AC coupled. It is recommended to use a matching network with an inductor to RF ground to improve ESD protection.
4	RFGND	Supply	Ground connection for ANT RF input. Connect to PCB ground plane.
5	CDEC	Supply	Internal supply decoupling access. Bypass to PCB ground plane with a 0.1µF ceramic capacitor located as close to pin as possible. Maximum operating voltage is 3.6V.
6	SQ	Input	Squelch control logic-level input. An internal pull-up (3µA typical) pulls the logic-input HIGH when the device is enabled. A logic LOW on SQ squelches, or reduces, the random activity on DO pin when there is no RF input signal.
7	VDD	Supply	Positive supply connection (for all chip functions). Bypass with 1µF capacitor located as close to the VDD pin as possible.
8	EN	Input	Enable control logic-level input. A logic-level HIGH enable the device. A logic-level LOW put the device to shutdown mode. An internal pull-down (3µA typical) pulls the logic input LOW. The device is designed to start up in shutdown state. The EN pin should be kept at logic low (shutdown state) until after the supply voltage on VDD is stabilized. If the application is designed to have the EN pin always pulled high, it is recommended to add a shunt capacitor of 0.47µF from the EN pin to ground.
9	GND	Supply	Ground connection for all chip functions except for RF input. Connect to PCB ground plane.

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
10	DO	Output	Demodulation data output. A current limited CMOS output in normal operation. An internal pull-down of 25kΩ is present when device is in shutdown.
11	SEL1	Input	Logic control input with active internal pull-up (3µA typical). It can be used to select the low-pass filter bandwidth in the absence register control (Table 1).
12	SEL0	Input	Logic control input with active internal pull-up (3µA typical). It can be used to select the low-pass filter bandwidth in the absence register control (Table 1).
13	CTH	Input/Output	Demodulation threshold voltage integration capacitor. Capacitor to GND sets the settling time for the demodulation data slice level. Values above 1nF are recommended and should be optimized for data rate and data profile. Connect a 0.1µF capacitor from CTH pin to GND to provide a stable slicing threshold.
14	AGC	Input/Output	AGC filter capacitor connection. Connect a capacitor from this pin to GND. Refer to the "AGC Loop" in the *Receiver Operation* section for information on the capacitor value.
15	RSSI	Output	Received Signal Strength Indicator output. The voltage on this pin is an inversed amplified version of the voltage on AGC. Output is from a buffer with typically 200Ω output impedance.
16	RO2	Output	Pierce Oscillator Output for Crystal Output: Internal capacitance of 7pF to GND during normal operation.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +6.0V
Voltage on all pins except Antenna..... –0.3V to V_{DD} + 0.3V
Antenna Input ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s)..... +300°C
Storage Temperature (T_S) ..... –65°C to +150°C
Maximum Receiver Input Power ..... +10dBm
ESD Rating[3] ..... 2kV HBM

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +3.5V to +5.5V
Antenna Input ..... -0.3V to +0.3V
All Pins (except antenna input) ..... –0.3V to V_{DD} + 0.3V
Ambient Temperature (T_A) ..... –40°C to +105°C
Maximum Input RF Power..... 0dBm
Receive Modulation Duty Cycle ..... 20% to 80%
Frequency Range..... 400MHz to 450MHz

Electrical Characteristics

V_{DD} = 5.0V, V_{EN} = 5V, SQ = Open, C_{AGC} = 4.7µF, C_{CTH} = 0.1µF, unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ +105°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Operating Supply Current	Continuous Operation, f_{RF} = 433.92MHz	4.5	6.0	8.0	mA
I_{SD}	Shutdown Current	V_{EN} = 0V		0.5	1	µA
Receiver						
	Conducted Receiver Sensitivity @ 1kbps[4]	433.92MHz, SEL0:SEL1 = 00, BER = 1%		–112.5		dBm
		433.92MHz, SEL0:SEL1= 00, BER = 0.1%		–110.0		
	Image Rejection	$f_{IMAGE} = f_{RF} – 2f_{IF}$		25		dB
f_{IF}	IF Center Frequency	f_{RF} = 433.92MHz		1.2		MHz
BW_{IF}	-3dB IF Bandwidth	f_{RF} = 433.92MHz		330		KHz
V_{AGC}	AGC Voltage Range	–40dBm RF input level		1.15		V
		–100dBm RF input level		1.55		

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside of its operating rating.
3. Device is ESD sensitive. Use appropriate ESD precautions. Human body model, 1.5kΩ in series with 100pF.
4. In an ON/OFF keyed (OOK) signal, the signal level goes between a “mark” level (when the RF signal is ON) and a “space” level (when the RF signal is OFF). Sensitivity is defined as the input signal level when “ON” necessary to achieve a specified BER (bit error rate). BER measured with the built-in BERT function in Agilent E4432B using PN9 sequence. Sensitivity measurement values are obtained using an input matching network to 433.92MHz.

Electrical Characteristics (Continued)

V_{DD} = 5.0V, V_{EN} = 5V, SQ = Open, C_{AGC} = 4.7µF, C_{CTH} = 0.1µF, unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ +105°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Reference Oscillator						
f_{RF}	Reference Oscillator Frequency	f_{RF} = 433.92MHz		13.52313		MHz
	Reference Buffer Input Impedance	RO1 when driven externally		1.6		kΩ
	Reference Oscillator Bias Voltage	RO2		1.15		V
	Reference Oscillator Input Range	External input, AC couple to RO1	0.2		1.5	V_{P-P}
	Reference Oscillator Source Current	V_{RO1} = 0V		300		µA
Demodulator						
	CTH Source Impedance[5]	f_{REF} = 13.52313MHz		120		KΩ
	CTH Leakage Current In CTH Hold Mode	T_A = +25ºC T_A = +105ºC		1 10		nA
Digital / Control Functions						
	DO Pin Output Current	As output source at 0.8V_{DD} As output sink at 0.2V_{DD}		300 680		µA
	Output Rise Time	15pF load on DO pin, transition time between 0.1V_{DD} and 0.9V_{DD}		600		ns
	Output Fall Time			200		
	Input High Voltage	EN, SQ	0.8V_{DD}			V
	Input Low Voltage	EN, SQ			0.2V_{DD}	V
	Output Voltage High	DO	0.8V_{DD}			V
	Output Voltage Low	DO			0.2V_{DD}	V
RSSI[6]						
V_{RSSI}	RSSI DC Output Voltage Range	–110dBm RF input level		0.4		V
		–50dBm RF input level		2.06		
	RSSI Output Current	5kΩ load to GND, –50dBm RF input level		400		µA
	RSSI Output Impedance			200		Ω
	RSSI Response Time	SEL0:SEL1 = 00, RF input power stepped from no input to –50dBm		9		ms
RF Leakage						
	LO Leakage for 433.92MHz	432.68064MHz (f_{XAL} = 13.52127MHz)		-106		dBm

Notes:

5. CTH source impedance is inversely proportional to the reference frequency. In production test, the typical source impedance value is verified with 12MHz reference frequency.
6. RSSI exhibit variation through manufacturing process, it is recommended that the reading is calibrated by software in system MCU when it is being used.

Electrical Characteristics (Continued)

V_{DD} = 5.0V, V_{EN} = 5V, SQ = Open, C_{AGC} = 4.7µF, C_{CTH} = 0.1µF, unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ +105°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Startup Time[7]						
	From EN To Data Output Time	433.92MHz at –100dBm, AGC capacitor = 4.7µF		48		ms
		433.92MHz at –100dBm, AGC capacitor = 2.2µF		26		
		433.92MHz at –100dBm, AGC capacitor = 1µF[8]		12		
		433.92MHz at –100dBm, AGC capacitor = 0.47 µF[8]		5		

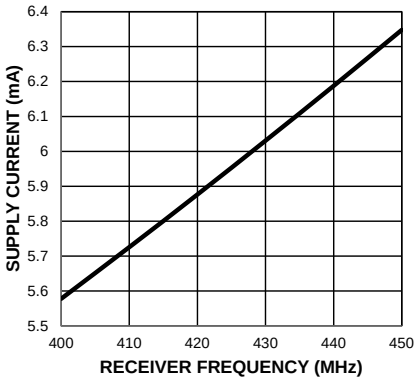
Notes:

7. The startup time is measured from EN pin low to high until steady data output at DO.
8. AGC cap values of 0.47uF and 1µF are not recommended for Auto-poll, it is applicable only for normal reception mode.

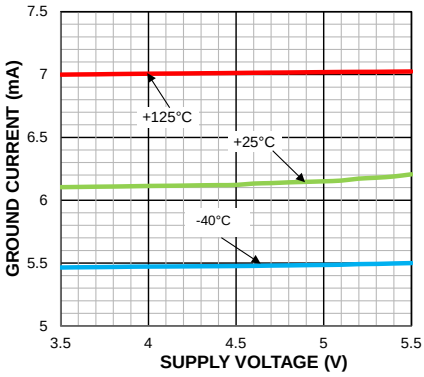
Typical Characteristics

V_{DD} = 5.0 V, T_A =+25°C, BER measured with PN9 sequence, unless otherwise noted.

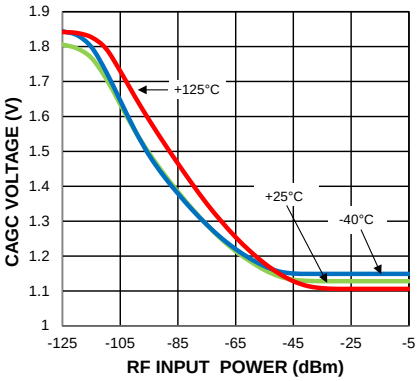
Current Vs. Receiver Frequency



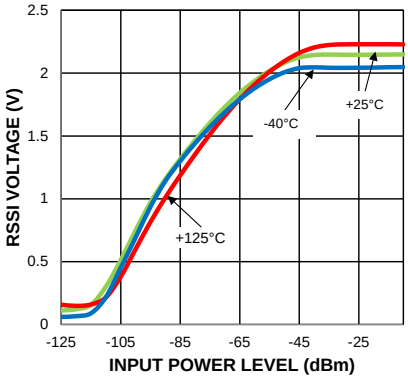
Ground Current vs. Supply Voltage (f_{RF} =433.92MHz)



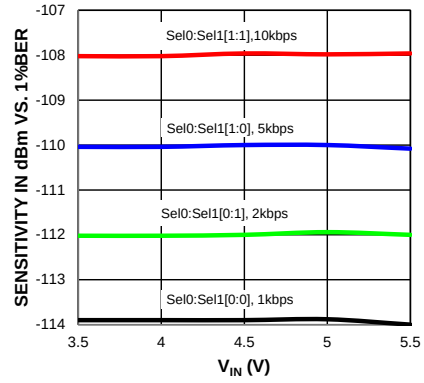
CAGC Volatge vs. Input Power



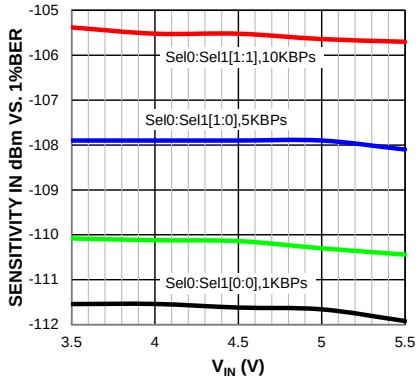
433.92 MHz RSSI Voltage vs. Input Power



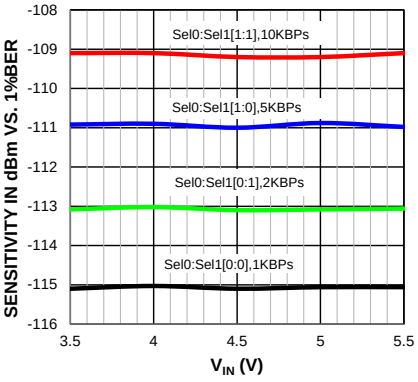
Sensitivity in 433.92MHz vs. V_{IN} at different BW in (+25°C)



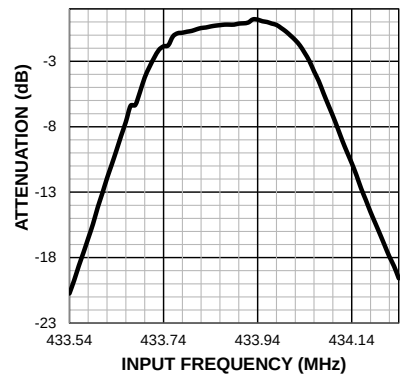
Sensitivity in 433.92MHz vs. VIN at different BW in (+105°C)



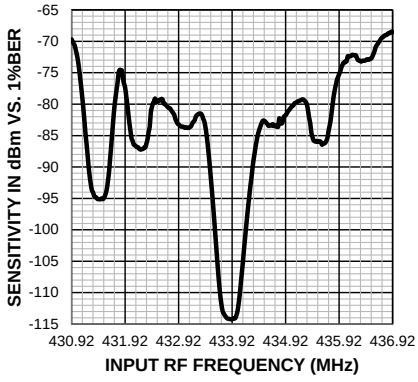
Sensitivity in 433.92MHz vs. V_{IN} at different BW IN (-40°C)



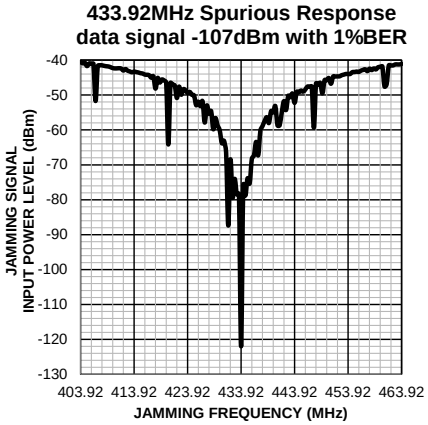
Bandpass Filter Attenuation fxal=13.52127MHz



434MHz Selectivity at 1.625KHz Bandwidth



Typical Characteristics (Continued)



Functional Diagram

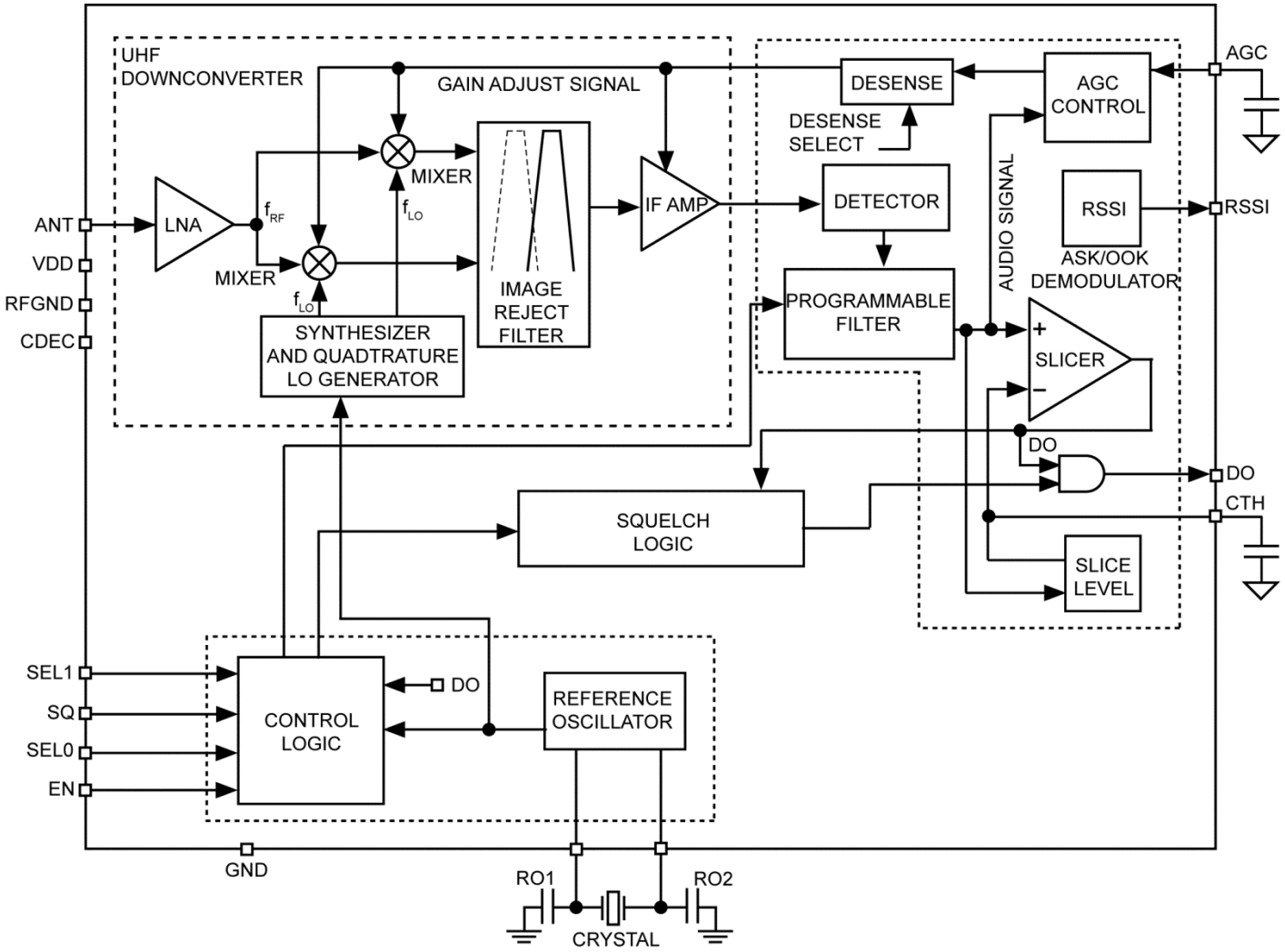


Figure 1. MICRF230 Simplified Functional Block Diagram

Functional Description

The simplified block diagram (Figure 1) illustrates the basic structure of the MICRF230 receiver. It is made up of four sub-blocks:

- UHF down-converter
- ASK/OOK demodulator
- Reference and control logic

Outside the device, the MICRF230 receiver requires just a few components to operate: a capacitor from AGC to GND, a capacitor from CTH to GND, a reference crystal resonator with associated loading capacitors, LNA input matching components, and a power-supply decoupling capacitor.

Receiver Operation

UHF Downconverter

The UHF down-converter has six sub-blocks: LNA, mixers, synthesizer, image reject filter, band pass filter and IF amplifier.

LNA

The RF input signal is AC-coupled into the gate of the LNA input device. The LNA configuration is a cascaded common-source NMOS amplifier. The amplified RF signal is then fed to the RF ports of two double balanced mixers.

Mixers and Synthesizer

The LO ports of the mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal (Figure 2). The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will be demodulated by the detector of the device. The image reject mixer suppresses the image frequency which is below the wanted signal by 2x the IF frequency. The local oscillator frequency (f_{LO}) is set to 32x the crystal reference frequency (f_{REF}) via a phase-locked loop synthesizer with a fully-integrated loop filter (Equation 1):

$$f_{LO} = 32 \times f_{REF} \qquad \text{Eq. 1}$$

MICRF230 uses an IF frequency scheme that scales the IF frequency (f_{IF}) with f_{REF} according to Equation 2:

$$f_{IF} = f_{REF} \times \frac{87}{1000} \qquad \text{Eq. 2}$$

Therefore, the reference frequency f_{REF} needed for a given desired RF frequency (f_{RF}) is approximated in Equation 3:

$$f_{REF} = f_{RF} / \left(32 + \frac{87}{1000}\right) \qquad \text{Eq. 3}$$

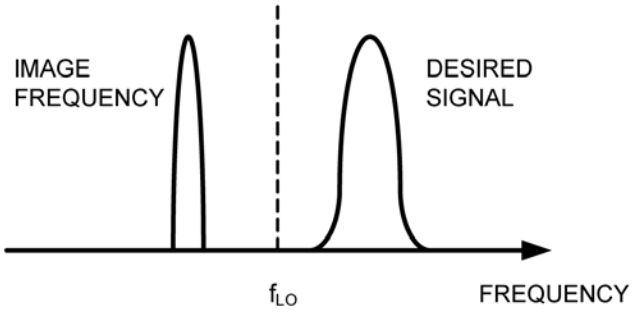


Figure 2. Low-Side Injection Local Oscillator

Image-Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature-down converted IF signals. These IF signals are low-pass filtered to remove higher frequency products prior to the image reject filter where they are combined to reject the image frequency. The IF signal then passes through a third order band pass filter. The IF bandwidth is 330kHz @ 433.92MHz, and will scale with RF operating frequency according to Equation 4:

$$BW_{IF} = BW_{IF@433.92\ MHz} \times \left(\frac{\text{Operating Frequency (MHz)}}{433.92}\right) \qquad \text{Eq. 4}$$

These filters are fully integrated inside the MICRF230.

After filtering, four active gain controlled amplifier stages enhance the IF signal to its proper level for demodulation.

ASK/OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes baseband information. The low-pass filter further enhances the baseband signal.

There are four selectable low-pass filter BW settings: 1625Hz, 3250Hz, 6500Hz and 13000Hz for 433.92MHz operation. The low-pass filter BW is directly proportional to the crystal reference frequency, and RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. Equation 5 illustrates filter Demod BW calculation:

$$BW_{Operating\ Freq} = BW_{@433.92MHz} \times \left(\frac{Operating\ Freqruency\ (MHz)}{433.92} \right)$$

Eq. 5

It is very important to select a suitable low-pass filter BW setting for the required data rate to minimize bit error rate. Use the sensitivity curves that show BER vs. bit rates for different SEL0:SEL1 settings as a guide.

This low-pass filter with –3dB corner frequency bandwidth can be configured by setting the registers as in Table 1 for 433.92MHz.

Table 1. Low-Pass Filter Bandwidth Selection @ 434MHz RF Input

SEL1	SEL0	Low-Pass Filter BW	Maximum Encoded Bit Rate
0	0	1625Hz	2.5KBps
0	1	3250Hz	5KBps
1	0	6500Hz	10KBps
1	1	13000Hz	20KBps

Bit rate refers to the encoded bit rate. Encoded bit rate is 1/(shortest pulse duration) that appears at DO:

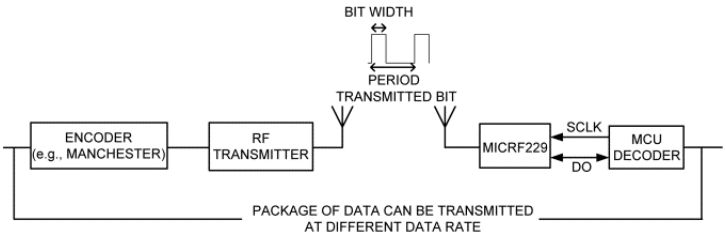


Figure 3. Transmitted Bit Rate through the air

Slicer and CTH

The signal before the slicer, labeled “Audio Signal” in Figure 1, is still a baseband analog signal. The data slicer converts the analog signal into ones and zeros based on 50% of the slicing threshold voltage built up in the CTH capacitor. After the slicer, the signal is demodulated OOK digital data. When there is only thermal noise at ANT pin, the voltage level on CTH pin is about 650mV. This voltage starts to drop when there is RF signal present. When the RF signal level is greater than –100dBm, the voltage is about 400mV.

The capacitor value from the CTH pin to GND is not critical to the sensitivity of MICRF230. However, it should be large enough to provide a stable slicing level for the comparator. The0.1µF value used in the evaluation board is good for all bit rates from 500bps to 20kbps.

CTH Hold Mode

If the internal demodulated signal (DO in Figure 1) is at logic LOW for more than approximately 4ms, the chip automatically enters CTH hold mode, which holds the voltage on CTH pin constant even without a RF input signal. This is useful in a transmission gap, or “dead time”, used in many encoding schemes. When the signal reappears, CTH voltage does not need to resettle. This improves the time to output with no pulse width distortion, or time to good data (TTGD).

AGC Loop

The AGC comparator monitors the signal amplitude from the output of the programmable low-pass filter. The AGC loop in the chip regulates the signal from the output point to be at a constant level when the input RF signal is within the AGC loop dynamic range (about –115dBm to –40dBm).

When the chip first turns on, the fast charge feature charges the AGC node up with 120µA typical current. When the voltage on AGC increases, the gains of the mixer and IF amplifier go up, increasing the amplitude of the audio signal (as labeled in Figure 1), even with only thermal noise at the LNA input. The fast-charge current is disabled when the audio signal crosses the slicing threshold, causing DO’ to go high, for the first time.

When an RF signal is applied, a fast-attack period ensues when 600µA current discharges the AGC node to reduce the gain to a proper level. Once the loop reaches equilibrium, the fast attack current is disabled, leaving only 15µA to discharge AGC or 1.5µA to charge AGC. The fast attack current is enabled only when the RF signal increases faster than the ability of the AGC loop to track it.

The ability of the chip to track to a signal that decreased in strength becomes much slower, since only 1.5µA is available to charge the AGC to increase the gain. When designing a transmitter that communicates with the

MICRF230, ensure that the power level remains constant throughout the transmit burst.

The value of AGC impacts the period between the TTGD, which is defined as the time when signal is first applied, to the pulse width at DO, within 10% of the steady state value. The optimal value of AGC depends on the setting of the D4 and D3 bits.

A smaller AGC value does not always result in a shorter TTGD. This is due to the loop dynamics, the fast discharge current being 600µA, and the charge current being only 1.5µA. For example, if SEL0 = SEL1 = 0, the low pass filter bandwidth is set to a minimum and the AGC capacitance is too small. The TTGD will be longer than if AGC capacitance is properly chosen. This is because when the RF signal first appears, the fast discharge period will reduce V_{AGC} very fast, lowering the gain of the mixer and IF amplifier. Since the low pass filter bandwidth is low, it takes too long for the AGC comparator to see a reduced level of the audio signal, and cannot stop the discharge current. This causes an undershoot in AGC voltage and a corresponding overshoot in RSSI voltage. Once the AGC undershoots, it takes a long time for it to charge back up because the current available is only 1.5µA.

Table 2 lists the recommended minimum AGC values for different SEL0 and SEL1 settings to insure that the voltage on AGC does not undershoot.

Table 2. Minimum Suggested AGC Values

SEL0	SEL1	AGC value
0	0	4.7µF
0	1	2.2µF
1	0	1µF
1	1	1µF

Figure 4 illustrates what occurs if AGC is too small for a given bandwidth setting. In this instance, SEL0 = 1, SEL1 = 0, AGC = 0.47µF, and the RF input level is stepped from no signal to –100dBm. RSSI voltage is shown in place of AGC voltage because RSSI is a buffered version of AGC with an inversion and amplification. Probing AGC directly can affect the loop dynamics through resistive loading from a scope probe, especially in the state where only 1.5µA is available, whereas probing RSSI does not. When the RF signal is first applied, RSSI voltage overshoots due to the fast discharge current on AGC, and the loop is too slow to stop this fast discharge current in time. Since the voltage on AGC is too low, the audio signal level is lower than the slicing threshold (voltage on CTH), and DO pin is low. Once the fast discharge current stops, only the small 1.5µA charge current is available in settling the AGC loop to the correct level, causing the recovery from AGC undershoot/RSSI overshoot condition to be slow. As a result, TTGD is about 9.1ms. It is recommended that Tantalum caps or high voltage ceramic caps are used for AGC to minimize capacitor leakage current which may affect the performance of the AGC.

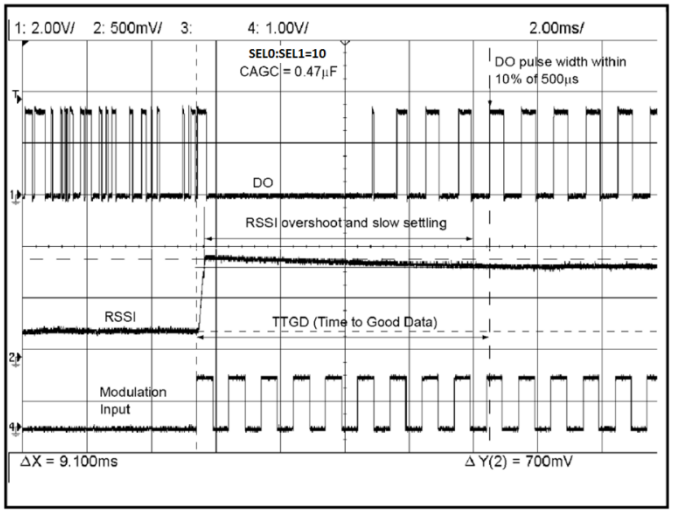


Figure 4. RSSI Overshoot and Slow TTGD (9.1ms)

Figure 5 shows the behavior with a larger capacitor on AGC pin (2.2µF), SEL0:SEL1 = 10. In this case, V_{AGC} does not undershoot (RSSI does not overshoot), and TTGD is relatively short at 1ms.

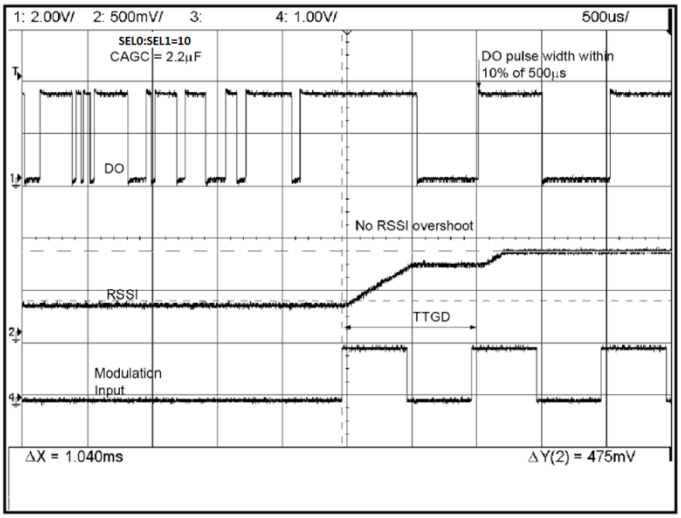


Figure 5. Proper TTGD (1ms) with Sufficient AGC

Reference Oscillator

The reference oscillator in the MICRF230, shown in Figure 6, uses a basic Pierce crystal oscillator

configuration with MOS transconductor. Though the MICRF230 has built-in load capacitors for the crystal oscillator, the external load capacitors are still required for tuning it to the right frequency. RO1 and RO2 are external pins of the MICRF230 to connect the crystal to the reference oscillator.

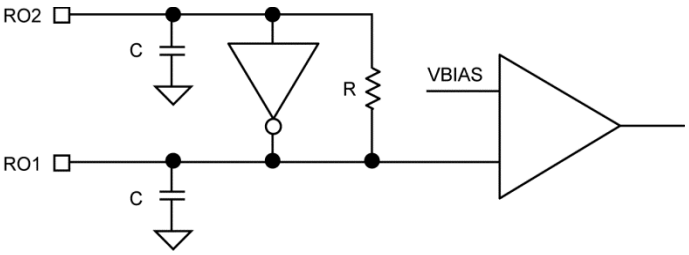


Figure 6. Reference Oscillator Circuit

Table 3. Reference Frequency Examples

RF Input Frequency (MHz)	Reference Frequency (MHz)
418.0	13.02708
433.92	13.52313[9]

Note:

9. Empirically derived, slightly different from Equation 3.

Squelch Operation

Squelch operation can be used to limit the amount of activity on the DO pin during normal operation, which is particularly useful when interrupt generated on DO can interfere with correct operation.

Table 4. Squelch Control

SQ Pin	Squelch Enable
0	Squelch Circuit Enabled
1	Squelch Circuit Disabled (default)

The external pin defaults high via an internal pull-up.

Application Information

Length of Preamble

When the MICRF230 returns to operation from shut down stage, the preamble of the corresponding transmitter should be long enough to guarantee that the MICRF230 becomes fully awake during the preamble portion of the burst. This way the entire data portion will be received.

Figure 7 shows an example of insufficient length preamble. MICRF230 starts demodulating output bits during the data portion of the burst, so by the time it becomes fully awake and releases DO, part of the data portion is lost. In Figure 8, the preamble length is sufficient. The chip has enough preambles to be demodulated with a steady data portion.

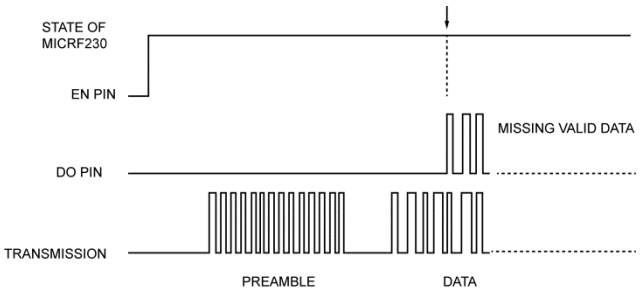


Figure 7. Preamble Length – Too Short

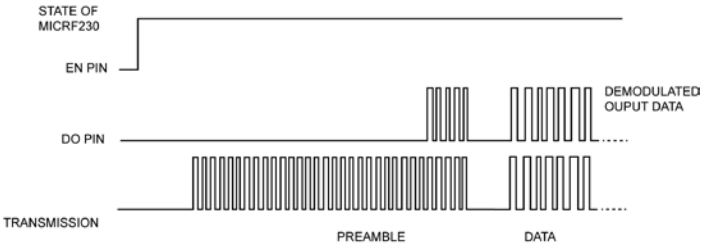


Figure 8. Preamble Length – Sufficient

Antenna and RF Port Connections

The evaluation board offers two options of injecting the RF input signal: through a PCB antenna or through a 50Ω SMA connector. The SMA connection allows for conductive testing, or an external antenna.

Low-Noise Amplifier Input Matching

Capacitor C3 and inductor L2 form the “L” shape input matching network to the SMA connector. The capacitor cancels out the inductive portion of the net impedance after the shunt inductor, and provides additional attenuation for low-frequency outside band noise. The inductor is chosen to over resonate the net capacitance at the pin, leaving a net-positive reactance and increasing the real part of the impedance. It also provides additional ESD protection for the antenna pin. The input impedance of the device is listed in Table 5 to aid calculation of matching values. Note that the net impedance at the pin is easily affected by component pads parasitic due to the high input impedance of the device. The numbers in Table 5 does NOT include trace and component pad parasitic capacitance, which total about 0.75pF on the evaluation board.

The matching components to the PCB antenna (L2 and C2) were empirically derived for best over-the-air reception range.

Table 5. Input Impedance for the Most Used Frequencies

Frequency (MHz)	Z Device (Ω)
418	8.98 – j152
433.92	13.5 – j150

Crystal Selection

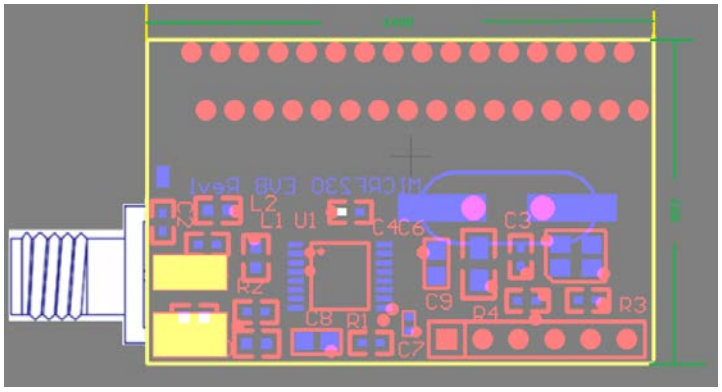
The crystal resonator provides a reference clock for all the device internal circuits. Crystal tolerance needs to be chosen such that the down-converted signal is always inside the IF bandwidth of MICRF230. From this consideration, the tolerance should be ±50ppm on both the transmitter and the MICRF230 side. The ESR should be less than 300Ω, and the temperature range of the crystal should match the range required by the application. With the Abracon crystal listed in the Bill of Materials, a typical MICRF230 crystal oscillator still starts up at 105°C with additional 400Ω series resistance.

The oscillator of the MICRF230 is a pierce-type oscillator. Good care must be taken when laying out the printed circuit board. Avoid long traces and place the ground plane on the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and the crystals used are not verified, the oscillator may not start or takes longer to start. Time-to-good-data will be longer as well.

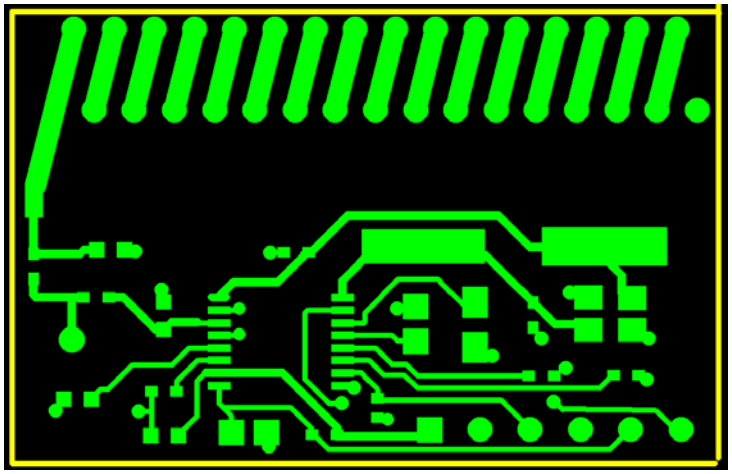
PCB Considerations and Layout

The MICRF230 evaluation board is a good starting point for prototyping of most applications. The Gerber files are downloadable from the Micrel website and contain the remaining layers needed to fabricate this board. When copying or making one's own boards, make the traces as short as possible. Long traces alter the may become invalid. Suggested matching values may vary due to PCB variations. A PCB trace 100 mils (2.5mm) long has about 1.1nH inductance. Optimization should always be done with range tests. Make sure the individual ground connection has a dedicated via rather than sharing a few of ground points by a single via. Sharing ground via will increase the ground path inductance. Ground plane should be solid and with no sudden interruptions. Avoid using the ground plane on the top layer next to the matching elements. It normally adds additional stray capacitance which changes the matching. Do not use Phenolic materials as they are conductive above 200MHz. FR4 or better materials are recommended. The RF path should be as straight as possible to avoid loops and unnecessary turns. Separate ground and V_{DD} lines from other digital or switching power circuits (such as microcontrollers, etc.). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid unnecessary wide traces which would add more distribution capacitance (between top trace to bottom GND plane) and alter the RF parameters.

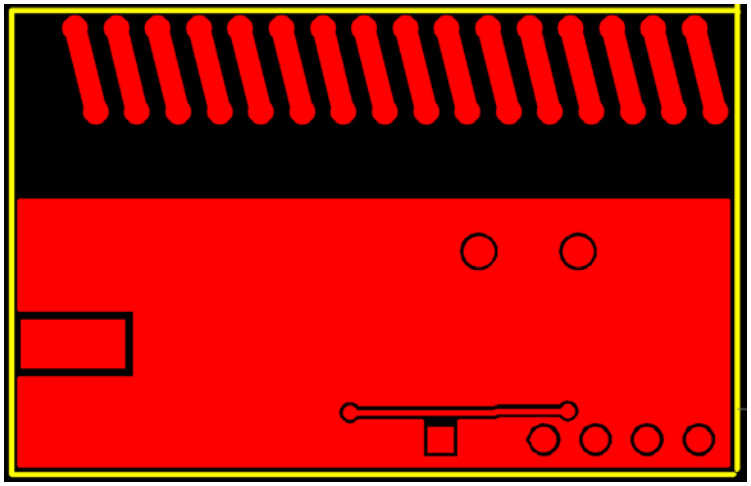
PCB Recommended Layout Considerations



MICRF230 Evaluation Board Assembly

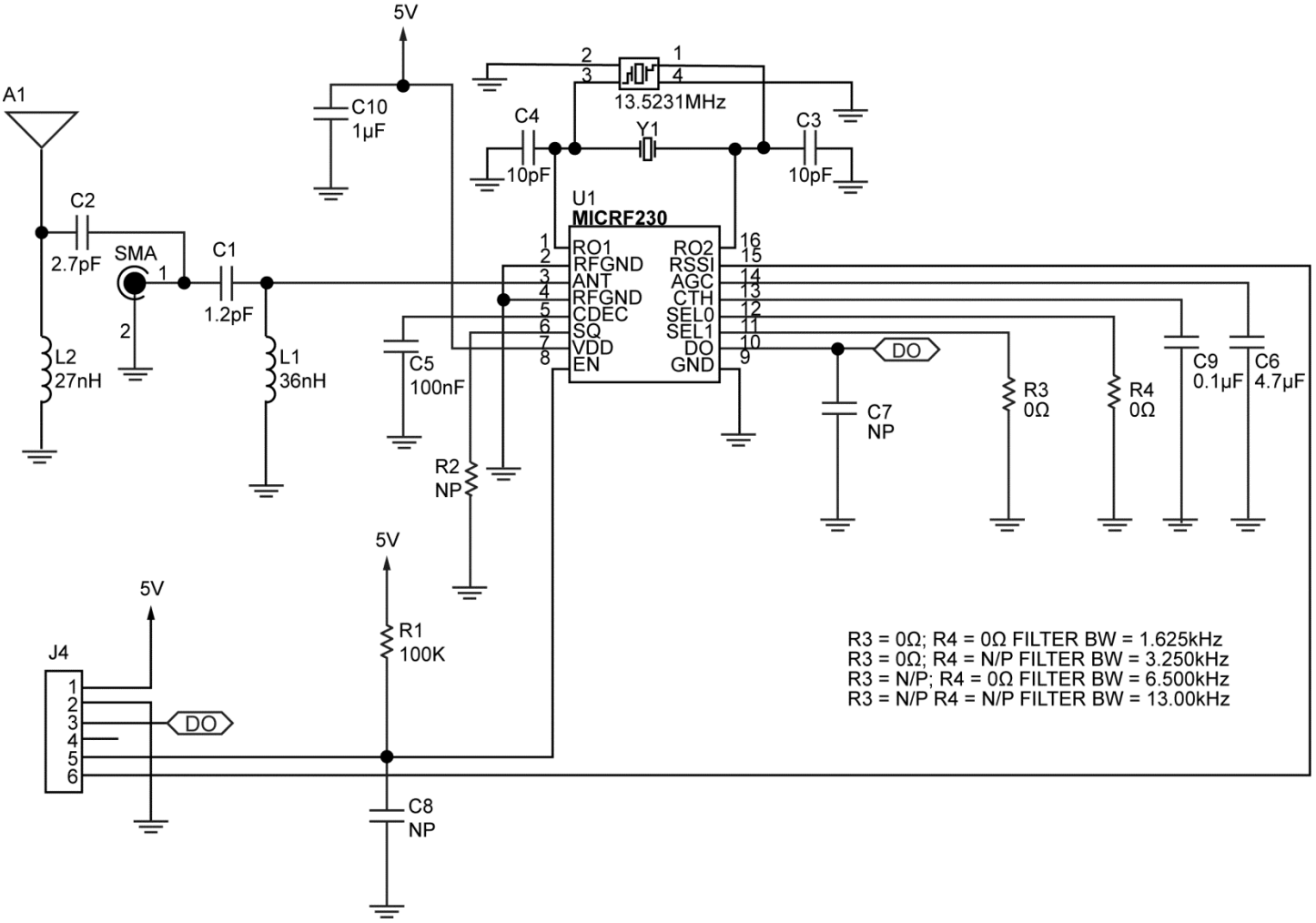


MICRF230 Evaluation Board Top Layer



MICRF230 Evaluation Board Bottom Layer

Evaluation Board Schematic



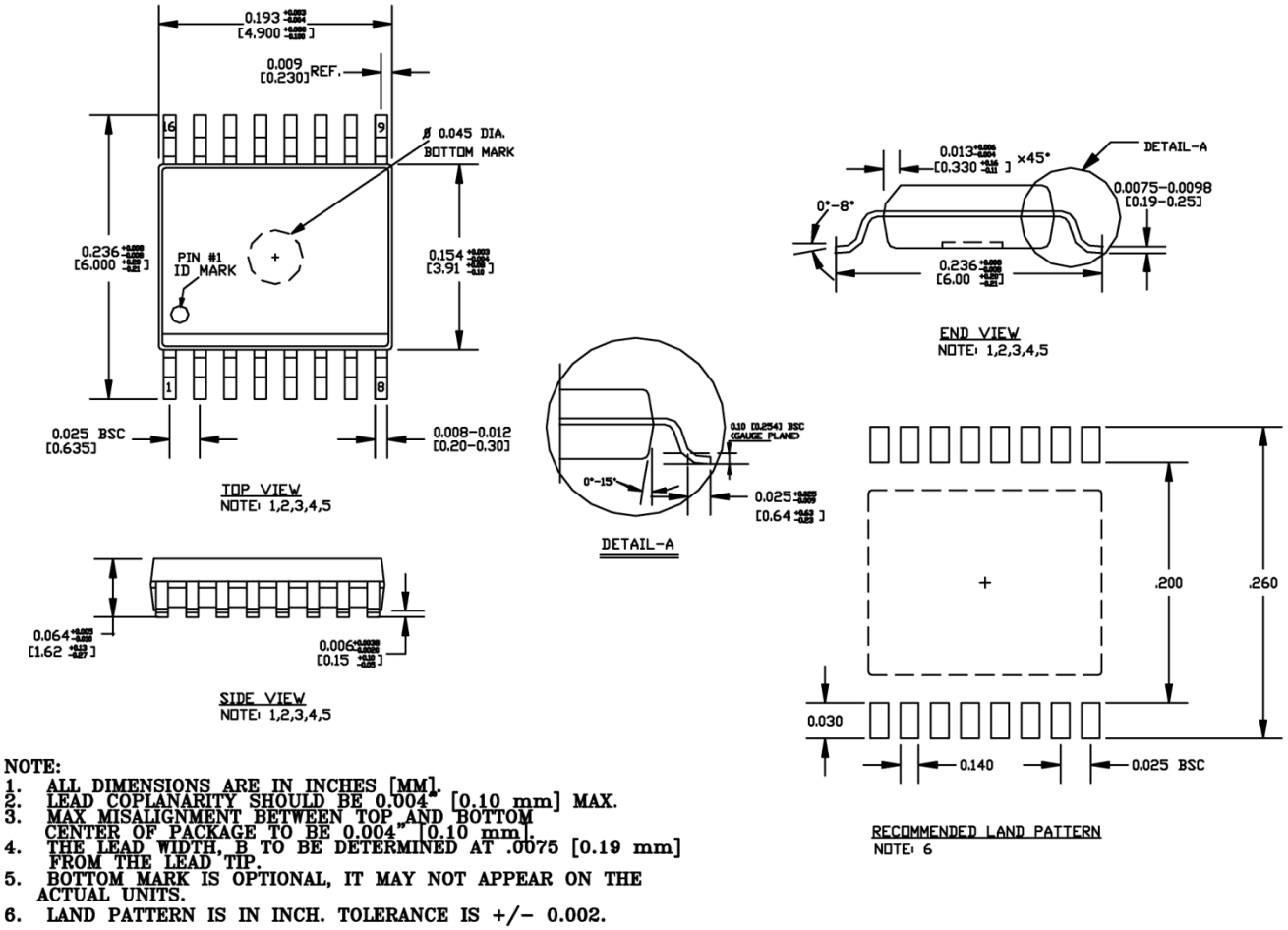
Bill of Materials – MICRF230 Evaluation Board (433.92MHz)

Item	Part Number	Manufacturer	Description	Qty.
C1	GRM1555C1H1R2CA01	Murata[10]	1.2pF ±0.25pF, 0402 Capacitor	1
C6	TAJA475M016RNJ	AVX[11]	4.7µF ±20%, Size A, Tantalum Capacitor	1
C9	GRM188R71E104K	Murata	0.1µF ±10%, 0603 Capacitor	1
C10	GRM188R71E105K	Murata	1µF ±10%, 0603 Capacitor	1
C5	GRM188R71E104K	Murata	0.1µF ±10%, 0603 Capacitor	0
C3, C4	GRM1555C1H100JA01	Murata	10pF ±5%, 0402 Capacitor	2
C2	GRM1555C1H2R7CA01	Murata	2.7pF ±0.25pF, 0402 Capacitor	1
SMA			NP, SMA, Edge Conn.	0
J4	571-41031480	Mouser[12]	AMPMODU Breakaway Headers 40 P(6pos) R/A Header Gold	1
L1	0603CS-36NXJL	Coilcraft[13]	36nH ±5%, 0603 Wire Wound Chip Inductor	1
L2	0603CS-27NXJL	Coilcraft	27nH ±5%, 0603 Wire Wound Chip Inductor	1
R1	CRCW0402100KFKEA	Vishay[14]	100kΩ ±5%, 0402 Resistor	1
R2			NP	3
C7, C8			NP	2
R3, R4	CRCW0402000KFKEA	Vishay	0 OHM +/-5%, 0402 Resistor	2
Y1	ABLS-13.52313MHz-10J4Y	Abracon[15]	13.52313MHz, HC49/US	1
Y2	DSX321GK-13.52313MHz	KDS[16]	NP, (13.52313MHz, –40°C to +105°C), DSX321GK	0
U1	**MICRF230YQS**	**Micrel, Inc[17]**	**400MHz to 450MHz ASK/OOK Receiver with RSSI, and Squelch**	**1**

Notes:

10. Murata: www.murata.com.
11. AVX: www.avx.com.
12. Mouser: www.mouser.com.
13. Coilcraft: www.coilcraft.com.
14. Vishay: www.website.com.
15. Abracon: www.abracon.com.
16. KDS: www.kds.info/index_en.htm.
17. **Micrel, Inc.: www.micrel.com.**

Package Information[18] and Recommended Landing Pattern



NOTE:

1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.
6. LAND PATTERN IS IN INCH. TOLERANCE IS +/- 0.002.

QSOP16 Package (QS)

Note:

18. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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