

Absolute Maximum Ratings

V_{DD} to V_{SS}-0.3V to +6V
 IN_+ or IN_-($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
 OUT_- Shorted to V_{SS} or V_{DD}Continuous
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 6-Bump WLP (derate 10.5mW/ $^\circ C$ above $+70^\circ C$).....840mW

Operating Temperature Range..... $-40^\circ C$ to $+85^\circ C$
 Junction Temperature..... $+150^\circ C$
 Storage Temperature Range..... $-65^\circ C$ to $+150^\circ C$
 Lead Temperature (soldering, 10s)..... $+300^\circ C$
 Soldering Temperature (reflow)..... $+260^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{DD} = +5V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR tests	1.8		5.5	V
Supply Current (per Amplifier)	I_{DD}	$V_{DD} = +1.8V$		0.6		μA
		$V_{DD} = +5.0V$		0.75	1.2	
Input Offset Voltage	V_{OS}			± 0.5	± 7.0	mV
Input Bias Current	I_B			± 200	± 1500	pA
Input Offset Current	I_{OS}			± 12.5		pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the CMRR test	V_{SS}		$V_{DD} - 1.1$	V
Common-Mode Rejection Ratio	CMRR	Specified with $V_{SS} \leq V_{CM} \leq (V_{DD} - 1.1V)$	70	95		dB
Power-Supply Rejection Ratio	PSRR	$+1.8V \leq V_{DD} \leq +5.5V$	70	90		dB
Large-Signal Voltage Gain	A_{VOL}	$R_L = 1M\Omega$, $V_{OUT} = 50mV$ to $V_{DD} - 50mV$	90	120		dB
		$R_L = 100k\Omega$, $V_{OUT} = 200mV$ to $V_{DD} - 200mV$	90	112		
		$R_L = 10k\Omega$, $V_{OUT} = 200mV$ to $V_{DD} - 200mV$		100		
Output Voltage Swing	V_{OH}	Swing high specified as $V_{DD} - V_{OH}$	$R_L = 1M\Omega$	1	4	mV
			$R_L = 100k\Omega$	4	10	
			$R_L = 10k\Omega$	40		
	V_{OL}	Swing low specified as $V_{OL} - V_{SS}$	$R_L = 1M\Omega$	0.5	5	
			$R_L = 100k\Omega$	1	5	
			$R_L = 10k\Omega$	10		
Gain-Bandwidth Product	GBW			9		kHz
Phase Margin	Φ_M			90		degrees

Electrical Characteristics (continued)(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

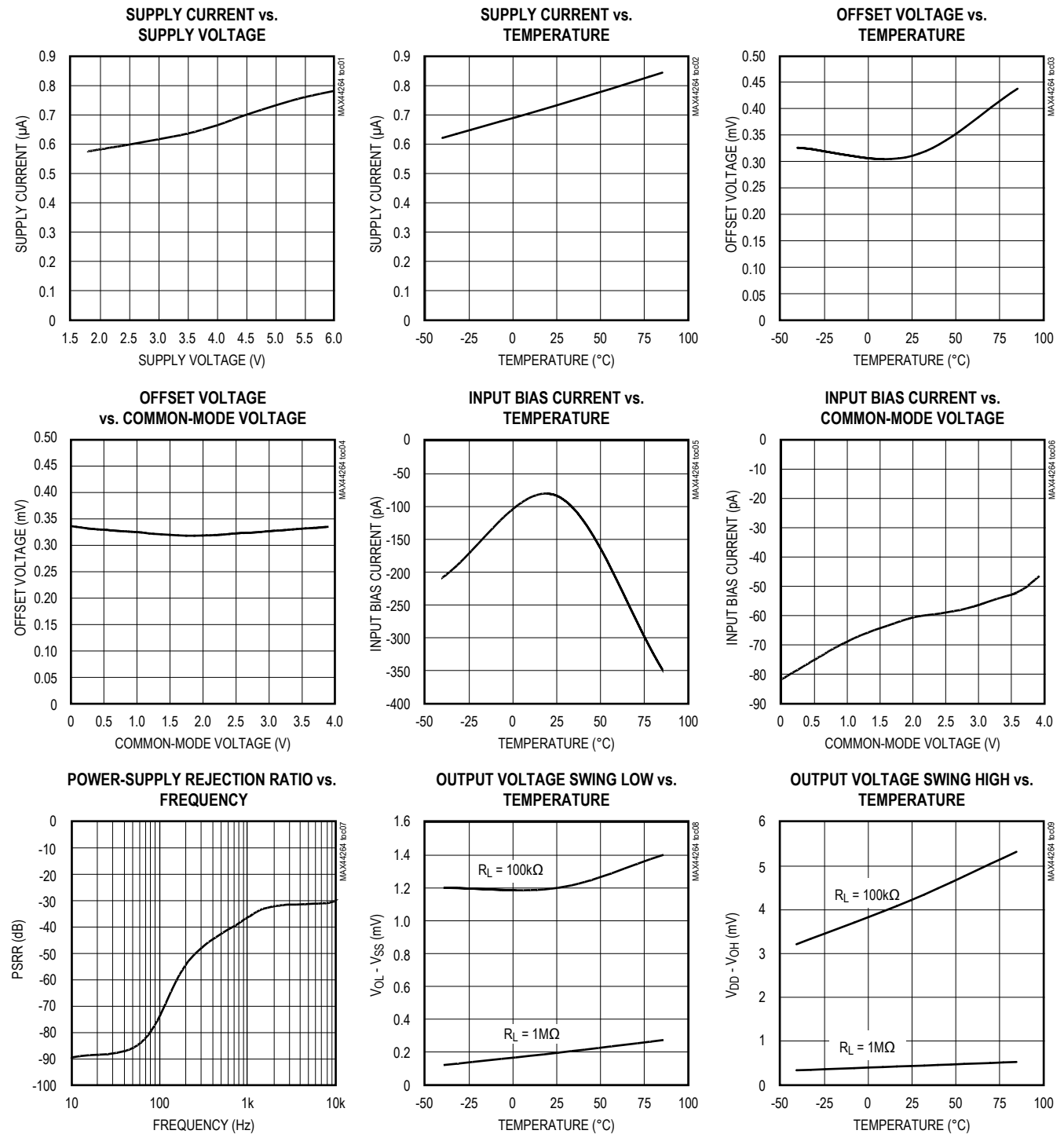
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR	V _{OUT} = 4V step		2		V/ms
Input Voltage Noise	e _n	f = 1kHz		150		nV/√Hz
		f = 10kHz		120		
Output Short-Circuit Current		Shorted to V _{SS} (sourcing)		11		mA
		Shorted to V _{DD} (sinking)		36		
Power-On Time	t _{ON}			2		μs
Power-Off Time	t _{OFF}			2		μs
Capacitive Load	C _{LOAD}	No sustained oscillations	250			pF

Electrical Characteristics(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ to V_{DD}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

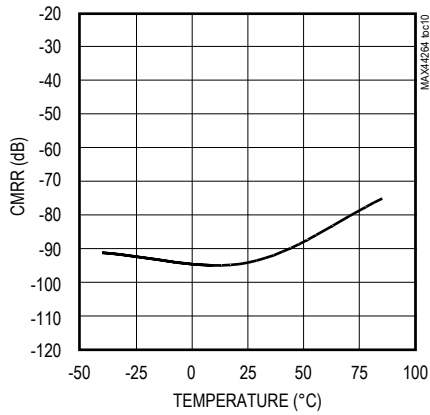
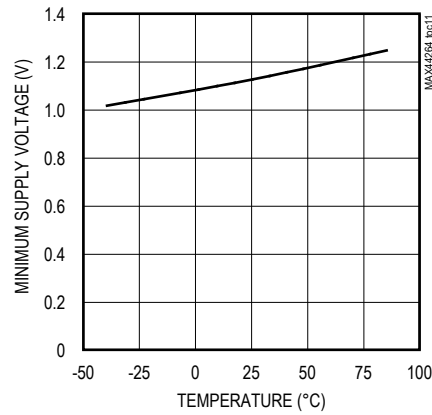
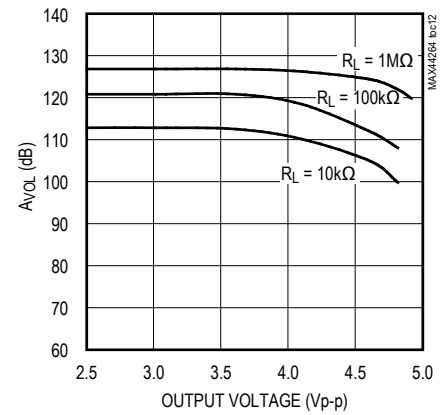
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V _{DD}	Guaranteed by PSRR tests	1.8		5.5	V
Supply Current (per Amplifier)	I _{DD}	V _{DD} = +5.0V			1.5	μA
Input Offset Voltage	V _{OS}				±15	mV
Input Offset Voltage Temperature Coefficient	TCV _{OS}			8		μV/°C
Input Bias Current	I _B				4.25	nA
Input Common-Mode Voltage Range	V _{CM}	Guaranteed by the CMRR test	V _{SS}		V _{DD} - 1.1	V
Common-Mode Rejection Ratio	CMRR	V _{SS} ≤ V _{CM} ≤ (V _{DD} - 1.1V)	56			dB
Power-Supply Rejection Ratio	PSRR	+1.8V ≤ V _{DD} ≤ +5.5V, 0°C ≤ T _A ≤ +85°C	65			dB
		+2V ≤ V _{DD} ≤ +5.5V, -40°C ≤ T _A ≤ +85°C	65			
Large-Signal Voltage Gain	A _{VOL}	V _{OUT} = 50mV to V _{DD} - 50mV, R _L = 1MΩ	75			dB
		V _{OUT} = 200mV to V _{DD} - 200mV, R _L = 100kΩ	75			
Output Voltage Swing	V _{OH}	Swing high specified as V _{DD} - V _{OH}	R _L = 1MΩ		5	mV
			R _L = 100kΩ		15	
	V _{OL}	Swing low specified as V _{OL} - V _{SS}	R _L = 1MΩ		5	
			R _L = 100kΩ		5	

Note 1: All devices are production tested at T_A = +25°C. All temperature limits are guaranteed by design.

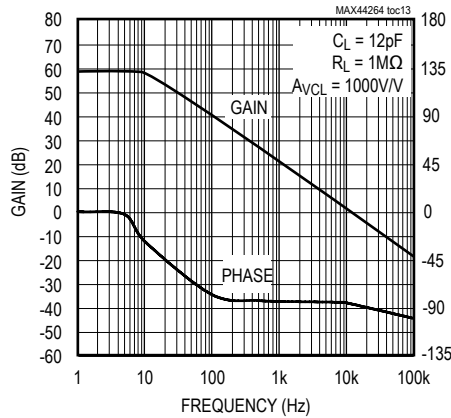
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

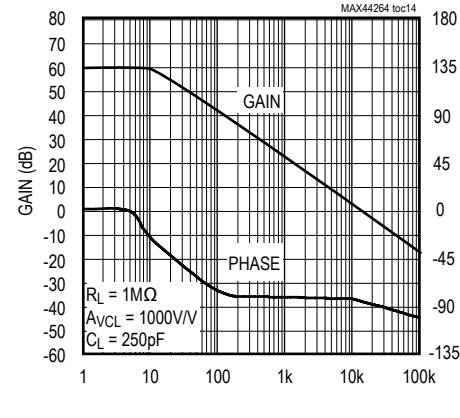
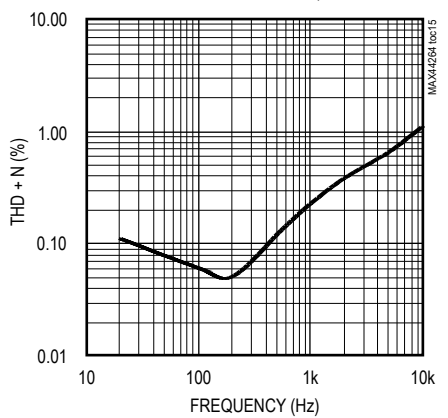
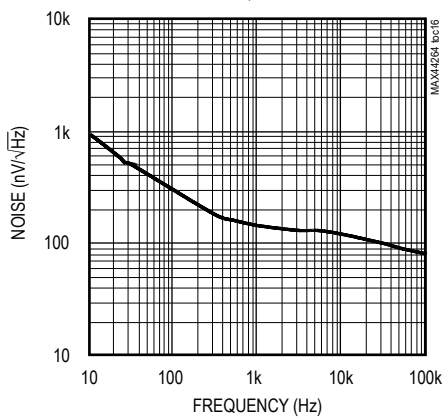
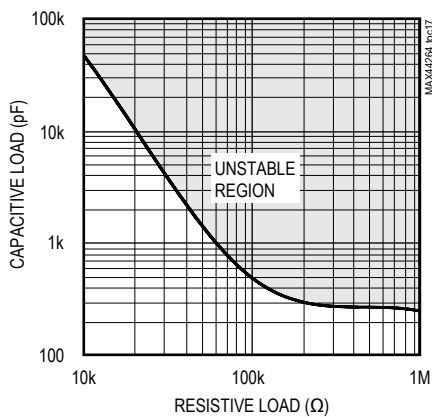
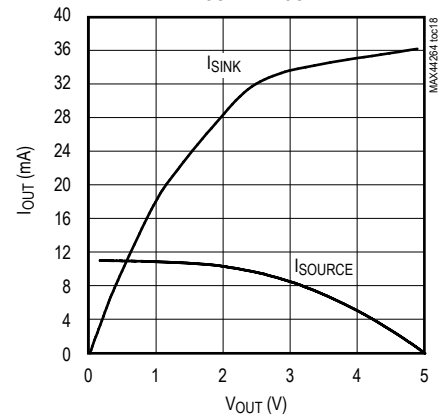
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)COMMON-MODE REJECTION RATIO vs.
TEMPERATUREMINIMUM SUPPLY VOLTAGE
vs. TEMPERATUREA_{voL} vs. OUTPUT VOLTAGE SWING

GAIN AND PHASE vs. FREQUENCY



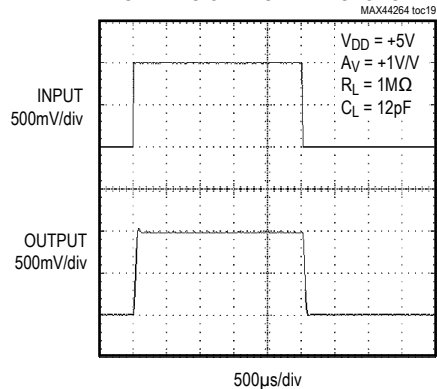
GAIN AND PHASE vs. FREQUENCY

TOTAL HARMONIC DISTORTION
PLUS NOISE vs. FREQUENCYVOLTAGE NOISE DENSITY vs.
FREQUENCYSTABILITY vs. CAPACITIVE
AND RESISTIVE LOADSI_{OUT} vs. V_{OUT}

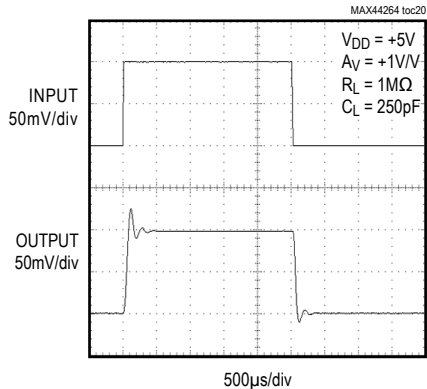
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

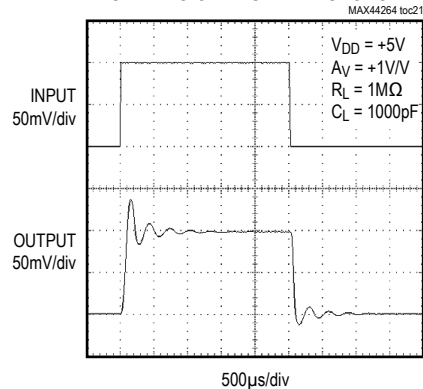
SMALL-SIGNAL STEP RESPONSE



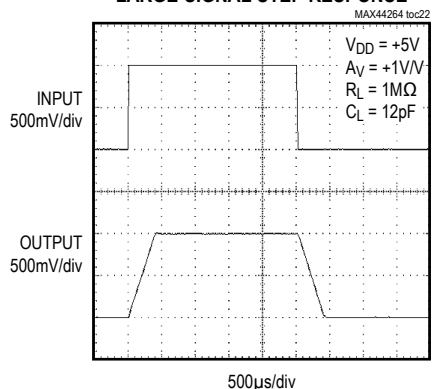
SMALL-SIGNAL STEP RESPONSE



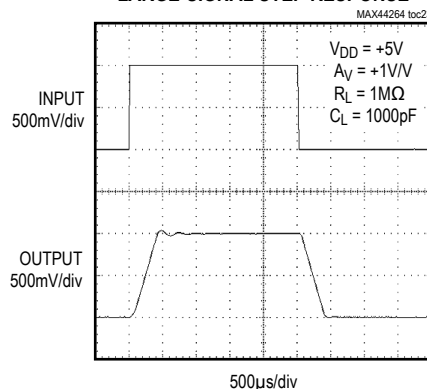
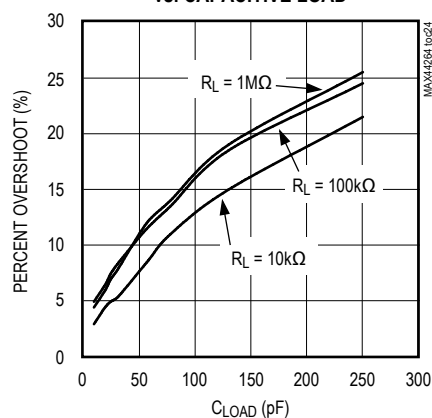
SMALL-SIGNAL STEP RESPONSE



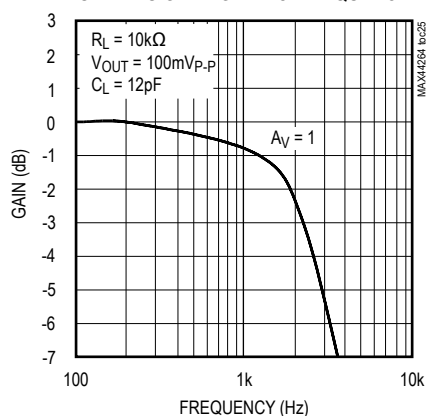
LARGE-SIGNAL STEP RESPONSE



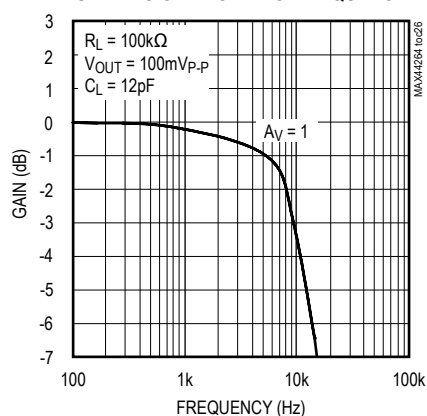
LARGE-SIGNAL STEP RESPONSE

PERCENT OVERSHOOT
vs. CAPACITIVE LOAD

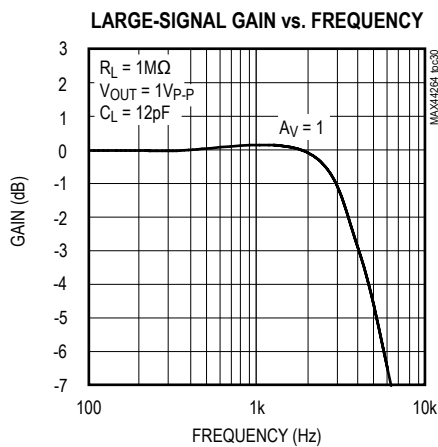
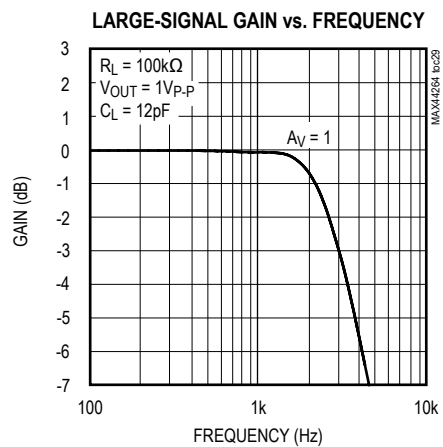
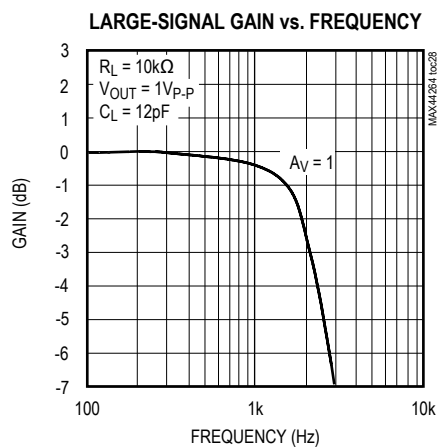
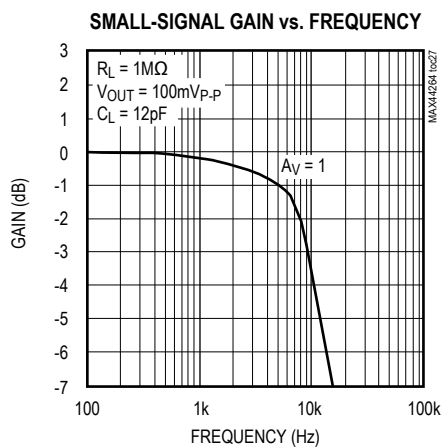
SMALL-SIGNAL GAIN vs. FREQUENCY



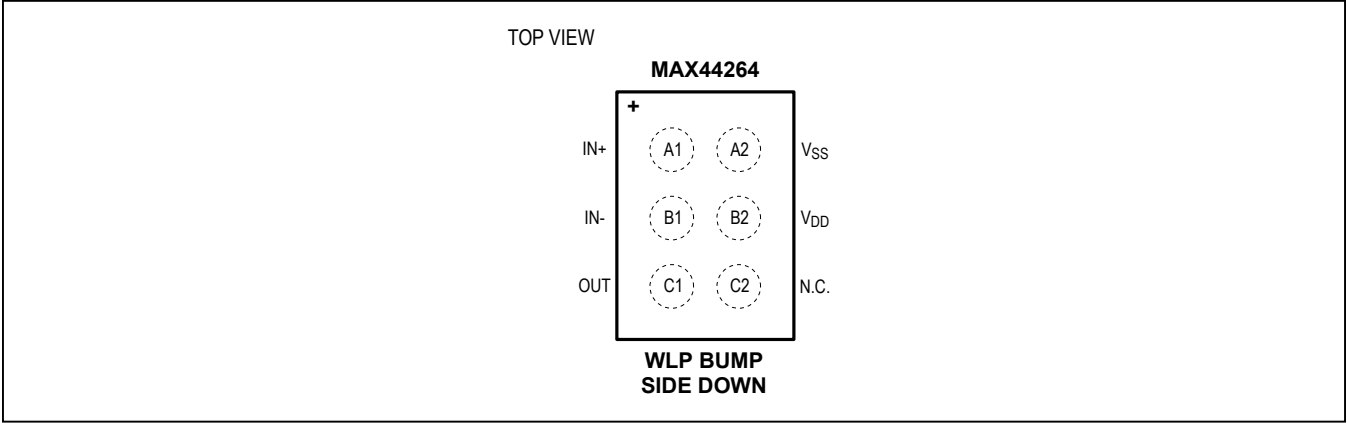
SMALL-SIGNAL GAIN vs. FREQUENCY



Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	IN+	Noninverting Amplifier Input
A2	V _{SS}	Negative Power-Supply Voltage
B1	IN-	Inverting Amplifier Input
B2	V _{DD}	Positive Power-Supply Voltage
C1	OUT	Amplifier Output
C2	N.C.	No Connection. Not internally connected.

Applications Information

Ground Sensing

The common-mode input range of the MAX44264 extends down to ground, and offers excellent common-mode rejection. These devices are guaranteed not to undergo phase reversal when the input is overdriven.

Power Supplies and Layout

The IC operates from a single +1.8V to +5.5V power supply. Bypass power supplies with a 0.1μF ceramic capacitor placed close to the V_{DD} pin.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components close to the op amps' pins.

Bandwidth

The IC is internally compensated for unity-gain stability and has a typical gain-bandwidth of 9kHz.

Stability

The IC maintains stability in their minimum gain configuration while driving capacitive loads. Although this product family is primarily designed for low-frequency applications,

good layout is extremely important because low-power requirements demand high-impedance circuits. The layout should also minimize stray capacitance at the amplifier inputs. However some stray capacitance may be unavoidable, and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor as shown in [Figure 1](#). Select the smallest capacitor value that ensures stability.

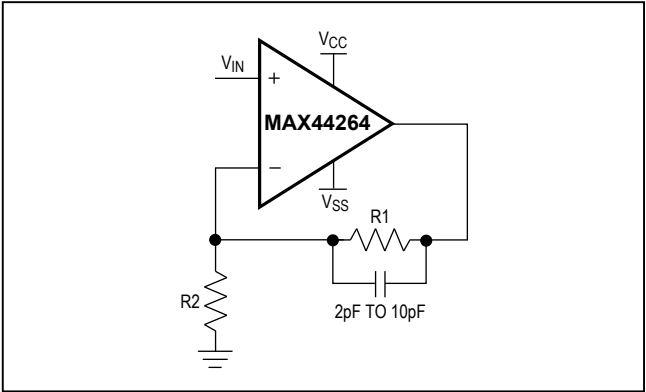
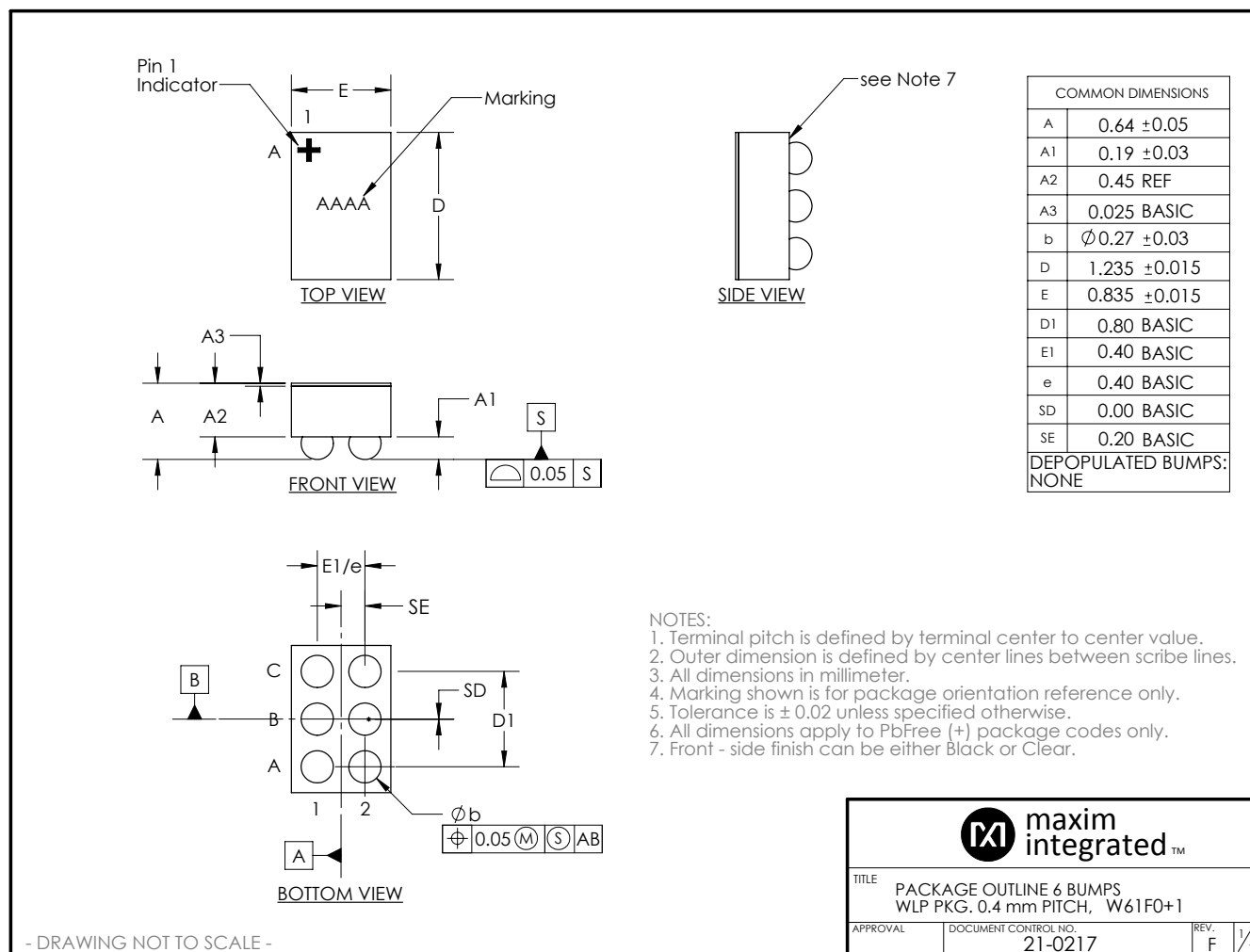


Figure 1. Compensation for Feedback Node Capacitance

Chip Information
PROCESS: BiCMOS

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 WLP	W61B1+1	21-0217	—



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	3/17	Updated title to include “nanoPower”	1–10

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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