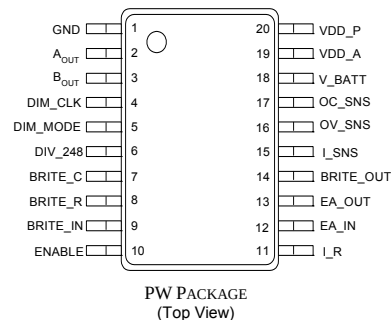


**ABSOLUTE MAXIMUM RATINGS**

|                                                                                               |                                  |
|-----------------------------------------------------------------------------------------------|----------------------------------|
| Supply Voltage (V <sub>BATT</sub> ).....                                                      | 30V                              |
| Digital Input (ENABLE).....                                                                   | -0.3V to 7V                      |
| Analog Inputs Transient Peak (I <sub>SNS</sub> , OC <sub>SNS</sub> , OV <sub>SNS</sub> )..... | -25V to +25V                     |
| Analog Inputs (BRITE_IN, EA_IN).....                                                          | -0.3V to 5.5V                    |
| Digital Inputs (DIM_CLK, DIM_MODE, DIV_248) .....                                             | -0.3V to 5.5V                    |
| Digital Output (A <sub>OUT</sub> , B <sub>OUT</sub> ) .....                                   | -0.3V to V <sub>DD_P</sub> +0.5V |
| Analog Outputs (BRITE_C, I <sub>R</sub> , BRITE_OUT, BRITE_R, EA_OUT) ...                     | -0.3V to V <sub>DD_A</sub> +0.5V |
| Storage Temperature Range .....                                                               | -65°C to 150°C                   |
| Maximum Operating Junction Temperature.....                                                   | 150°C                            |
| RoHS / Pb-free Peak Package Solder Reflow Temperature<br>(40 second maximum exposure).....    | 260°C (+0,-5)                    |

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

**PACKAGE PIN OUT**


RoHS / Pb-free 100% Matte Tin Lead Finish

**THERMAL DATA**
**PW Plastic TSSOP 20-Pin**

**THERMAL RESISTANCE-JUNCTION TO AMBIENT,  $\theta_{JA}$**  **144°C/W**

Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .

The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

**FUNCTIONAL PIN DESCRIPTION**

| PIN NAME          | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND               | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| V <sub>DD_P</sub> | Power VDD_P Supply Output. This output pin is used to connect an external capacitor to stabilize and filter the on chip VDD_P LDO regulator. The input of the LDO is the switched V <sub>BATT</sub> supply. LDO output is normally 5.3V and is used only to drive the output buffers at A <sub>OUT</sub> and B <sub>OUT</sub> . The external capacitor will be a 100 to 1000nF ceramic dielectric. Up to 5mA DC additional load may be imposed by external circuitry. External load must be reduced if the combination of output current and input voltage exceeds power dissipation capability of the die.                                                      |
| A <sub>OUT</sub>  | A buffer N-FET driver output. The pin includes a internal 10K pull down resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| V <sub>DD_A</sub> | Analog VDD_A Supply Output. This output pin is used to connect an external capacitor to stabilize and filter the on chip VDD_A LDO regulator. The input of the LDO is the switched V <sub>BATT</sub> supply. LDO output is normally 2.95V and is used to drive all circuitry except the output buffers at A <sub>OUT</sub> and B <sub>OUT</sub> . Average internal load is 6mA. Up to 5mA DC additional load may be imposed by external circuitry. External load must be reduced if the combination of output current and input voltage exceeds power dissipation capability of the die. The external capacitor will be a 100 to 1000nF ceramic dielectric type. |
| B <sub>OUT</sub>  | B buffer N-FET driver output. The pin includes a internal 10K pull down resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| V <sub>BATT</sub> | Voltage Input, 3 to 28V input range. V <sub>BATT</sub> is switched (see ENABLE) to remove power from chip. Two LDO regulators follow the switch, one generates VDD_P (see VDD_P) and the other VDD_A (see VDD_A). Care must be taken in power distribution design to minimize transients and noise coupling from the VDD_P output to the VDD_A output. The external capacitor will be a 100 to 1000nF ceramic dielectric type.                                                                                                                                                                                                                                   |

**FUNCTIONAL PIN DESCRIPTION (CONTINUED)**

| PIN NAME | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIM_CLK  | Digital Dimming Clock / Dimming Polarity. An input pin that may be selected to control burst frequency for external Digital Dimming. This input can be any clock signal up to 200KHz. This pin is also used to control the dimming polarity when operating in the analog or internal digital mode. If DIM_MODE is in the open condition (Analog Dimming Mode) the DIM_CLK input should be connected to VDD_A for conventional dimming polarity or set to Ground for reverse polarity. Conventional polarity means that lamp brightness increases with increasing voltage on the BRITE_IN pin. Reverse polarity means that brightness decreases with increasing voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| OC_SNS   | Over Current Sense Input. A full wave AC voltage input centered on ground that is proportional to total high voltage transformer secondary winding current. The OC_SNS input is full wave rectified, then applied to a digital comparator with a 2V reference to cause peak voltages greater than 2V to digitally reset the PWM logic on a pulse by pulse basis.<br>Frequency range of the input signal is 10kHz to 500KHz. Normal operating voltage levels should be under max $\pm 1.8\text{V}_{\text{PK}}$ , and abnormal voltage can operate continuously as high as $\pm 10\text{V}$ peak under load fault conditions. Transients under fault conditions can reach $\pm 25\text{V}_{\text{PK}}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| DIM_MODE | Dimming Mode Input. This three state input pin places the IC in Analog Dimming Mode, internal Digital Dimming Mode, or external Digital Dimming Mode. If the input is left open or forced to VDD_A / 2 Analog mode is selected.<br>If connected to VDD_A, Digital Dimming with a external clock source applied to the DIM_CLK input is selected to the burst timing generator. If connected to Ground, Digital Dimming with a internal clock is selected. The internal clock is equivalent to the frequency at AOUT divided by two, both the internal or external clock frequency can be divided down by setting the DIV_248 pin. (see DIV_248)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| OV_SNS   | Over Voltage Sense Input. A full wave AC voltage input centered around ground that is proportional to lamp voltage. The OV_SNS input will be full wave rectified, then applied to a digital comparator with a 2V reference to cause peak voltage greater than 2V to digitally reset the PWM logic on a pulse by pulse basis.<br>Frequency range of the input signal is 10KHz to 500KHz. Normal operating voltage levels should be under $\pm 1.8\text{V}_{\text{PK}}$ , and abnormal voltage can operate continuously as high as $\pm 10\text{V}$ peak under load fault conditions. Transients under fault conditions can reach $\pm 25\text{V}_{\text{PK}}$ .<br>The input has a 10K pull down resistor that serves as a DC restorer to the external capacitor that divides down lamp voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| DIV_248  | Divide Digital Dimming clock by 2, 4, or 8. This three state input pin causes the internal or external digital dimming clock source to be divided by one of the three values, 2, 4, or 8. Its purpose is to allow a selection of three possible burst rates for any given external or internal clock source. A high (VDD_A) selects divide by 2, open selects divide by 4, and ground selects divided by 8. We advise keeping burst above 95Hz and below about 400HZ. This will minimize visible flicker and possible audible noise from the power supply components.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| I_SNS    | Current Sense Input. A full wave AC voltage input centered around ground that is proportional to lamp current. The I_SNS input is full wave rectified and amplified, then presented to the inverting input of the current error amplifier through a 100K resistor.<br>Frequency range of the input signal is 10KHz to 500KHz. Normal operating voltage levels will be in the range of $\pm 0.5$ to $2.5\text{V}_{\text{PK}}$ , and abnormal voltage can operate continuously as high as $\pm 10\text{V}$ peak under load fault conditions. Transient under fault conditions can reach $\pm 25\text{V}_{\text{PK}}$ . We strongly recommend a 10K resistor be placed in series with the pin to limit current from voltage spikes that can occur by intermittent lamp connectors, or arcing from a faulty high voltage transformer. This resistor will eliminate the possibility of IC damage under these fault conditions.<br>The open lamp fault logic monitors the I_SNS pin voltage and number of lamp current cycles. If the number of lamp current cycles with amplitude below fault threshold are less than 8 in a given fault checking period then the strike latch will not be reset and a fault is declared, which shuts down the A/B outputs. In the strike mode, if no lamp current is detected after 15 attempts a fault is likewise declared. ( See further LX1689 operation section) |

**FUNCTIONAL PIN DESCRIPTION (CONTINUED)**

| PIN NAME  | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BRITE_C   | BRITE Filter Capacitor and FAULT Output. Used to convert higher frequency digital PWM inputs to proportional DC currents at the BRITE_OUT pin. The capacitor forms a low pass filter with an internal 200K resistor. This pin will be driven to VDD_A if a lamp fault is detected by the LX1689. If no fault is present the voltage at this pin will vary from 50mV to 1.05V as BRITE_IN varies from 0 to 2V. A CMOS gate may be connected to this pin to sense the fault condition. TTL gates or other low impedance (less than 20 megohm) must not be connected to this node as their DC resistance will load the internal 200K resistor and create error in the BRITE_OUT current level.                                                             |
| EA_IN     | Error Amp Inverting Input. Frequency Compensation input for the Error Amplifier. See EA_OUT below. A 100K, negative TC on chip resistor connected between the inverting input of the error amplifier and the output of the I_SNS full wave rectifier is the resistor in an R/C loop compensation network.                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| BRITE_R   | Dedicated Bias resistor for BRITE_OUT current source.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| EA_OUT    | Error Amp Output. Error amplifier is a GM type and does not require a external capacitor for stability. An external capacitor is connected from this pin to EA_IN to adjust the loop response of the inverter module. This capacitor value can vary from 100pF to 5000pF in various applications. This capacitor may also be connected from the EA_OUT to ground.                                                                                                                                                                                                                                                                                                                                                                                       |
| BRITE_IN  | Brightness Control Input. The input signal can be a DC voltage, a low frequency pulse width modulated digital signal, or a high frequency pulse width modulated digital signal. Active DC voltage range is 0.5 to 2.0V. Signals above 2V are clipped and signals below 0.5V make output current from the BRITE_OUT pin near zero. Low frequency digital PWM signals up to 500Hz can be applied to affect Digital Dimming. Higher frequency PWM signals, up to 100KHz are filtered to an equivalent DC current at the BRITE_OUT pin by adding a capacitor at the BRITE_C pin. On chip signal conditioning amplifiers clip inputs above 2V so that lamp current amplitude is not sensitive to the voltage level variations of a digital PWM input signal. |
| BRITE_OUT | <p>Brightness Reference Current Output. This variable current source is the mirror of BRITE_R current multiplied by the voltage at BRITE_C (0 to 1.0V) when analog dimming is selected, or by 1.0V when digital dimming is selected. It becomes the reference voltage to the lamp current error amplifier when applied to an external precision resistor connected from the BRITE_OUT pin to ground. BRITE_OUT current:</p> $I_{BRITE\_OUT} = I_{BRITE\_R} \times 1.0 \text{ (Digital Dimming Mode)}$ $I_{BRITE\_OUT} = I_{BRITE\_R} \times V_{BRITE\_C} \text{ (Analog Dimming Mode)}$ $V_{BRITE\_OUT} = I_{BRITE\_R} \times R_{BRITE\_OUT}$ $I_{BRITE\_R} = \frac{1.00V}{R_{BRITE\_R}}$                                                               |
| ENABLE    | <p>Chip Enable Input. If logic high, all functions are enabled. If logic low, internal power is disconnected from the V_BATT pin, disabling all functions. Logic threshold is about 1.2V. Maximum current into V_BATT when ENABLE &lt; 0.3V, V_BATT &lt; 28V, is 28 <math>\mu</math>A. ENABLE may be connected to V_BATT through a series resistor if the disable function is not used. Resistor tolerance is <math>\pm 10\%</math>; and R value is:</p> $R = \frac{[V_{BATT\_MIN} - 1.5V]}{30 \times 10^{-6} \text{ Amp}}$ <p>The Enable pin can be connected directly to 3.3/5V logic.</p>                                                                                                                                                            |
| I_R       | <p>Current Reference Resistor Input. Connects to an external resistor that determines the magnitude of internal bias currents. The nominal lamp frequency can be adjusted by varying this resistor value in the range of 10K to 150K Ohms.</p> $I_{I\_R} = \frac{1.00V}{R_{I\_R}}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                                             | LX1689 |     |     | Units    |
|-------------------------------------------------------|--------|-----|-----|----------|
|                                                       | Min    | Typ | Max |          |
| Supply Voltage ( $V_{BATT}$ )                         | 3      |     | 28  | V        |
| Digital Input (ENABLE)                                | 0      |     | 6.5 | V        |
| Analog Inputs ( $I_{SNS}$ , $OC_{SNS}$ , $OV_{SNS}$ ) | -3     |     | 3   | $V_{PK}$ |
| BRITE_IN Linear DC Voltage Range                      | 0.5    |     | 2   | V        |
| BRITE_IN PWM Logic Signal Voltage Range               | 0      |     | 5   | V        |
| Digital Inputs (DIM_MODE, DIV_248, DIM_CLK)           | 0      |     | 5.5 | V        |
| Maximum Output Gate Charge ( $A_{OUT}$ , $B_{OUT}$ )  |        | 10  | 20  | nC       |

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, the following specifications apply over the operating ambient temperature: LX1689CPW:  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ , LX1689IPW:  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , except where otherwise noted.

Test conditions:  $V_{BATT} = 3.3$  to  $28 V_{DC}$ ,  $I_R = 80.6\text{K}\Omega$ ,  $BRITE_R = BRITE_{OUT} = 10\text{K}\Omega$ ,  $BRITE_C = \text{open}$ ,  $ICOMP = 100\text{pF}$

| Parameter                          | Symbol                  | Test Conditions                                                  | LX1689 |      |      | Units |
|------------------------------------|-------------------------|------------------------------------------------------------------|--------|------|------|-------|
|                                    |                         |                                                                  | Min    | Typ  | Max  |       |
| POWER                              |                         |                                                                  |        |      |      |       |
| Regulator Output Voltage           | V <sub>DD_P</sub>       | V <sub>BATT</sub> = 6 to 28 V, I Load = 0 – 5mADC                | 5.05   | 5.3  | 5.55 | V     |
| V <sub>DD_P</sub> Drop Out Voltage | ΔV <sub>DD_P</sub>      | ΔV <sub>DD_P</sub> = -1% , I Load = 5mADC; T <sub>A</sub> = 25°C |        | 50   |      | mV    |
| Regulator Output Voltage           | V <sub>DD_A</sub>       | V <sub>BATT</sub> = 3.5 to 28V, I Load = 0 – 5mADC               | 2.75   | 2.95 | 3.15 | V     |
| V <sub>DD_A</sub> Dropout Voltage  | ΔV <sub>DD_A</sub>      | ΔV <sub>DD_A</sub> = -1% , I Load = 5mADC; T <sub>A</sub> = 25°C |        | 100  |      | mV    |
| V <sub>BATT</sub> Static Current   | I <sub>BATT</sub>       |                                                                  |        | 5.5  | 9    | mA    |
| V <sub>BATT</sub> Dynamic Current  | I <sub>BATT</sub>       | C <sub>AO</sub> UT = C <sub>BO</sub> UT = 1000pF                 |        | 10   | 17   | mA    |
| Sleep Mode Current                 | I <sub>BATT_SLEEP</sub> | V <sub>ENABLE</sub> ≤ 0.4V; V <sub>BATT</sub> = 5V               |        | 2.8  | 5    | μA    |
| Sleep Mode Current                 | I <sub>BATT_SLEEP</sub> | V <sub>ENABLE</sub> ≤ 0.4V; V <sub>BATT</sub> = 28V              |        | 22   | 35   | μA    |
| ENABLE INPUT                       |                         |                                                                  |        |      |      |       |
| Run Threshold                      | V <sub>TH_ENRUN</sub>   |                                                                  |        | 1.1  | 1.4  | V     |
| Shutdown Threshold                 | V <sub>TL_ENSHDN</sub>  |                                                                  | 0.4    | 1.1  |      | V     |
| Input High Current                 | I <sub>IH_ENABLE</sub>  | ENABLE = 2V                                                      |        | 2    | 12   | μA    |
| Input High Current                 | I <sub>IH_ENABLE</sub>  | ENABLE = 5V                                                      |        | 35   | 80   | μA    |
| Input Low Current                  | I <sub>IL_ENABLE</sub>  | ENABLE = 0V                                                      | -1     | 0    | 1    | μA    |
| UNDER VOLTAGE LOCKOUT              |                         |                                                                  |        |      |      |       |
| Startup Threshold                  | V <sub>T_UVLO</sub>     | Run Mode                                                         |        | 2.55 | 2.8  | V     |
| UVLO Threshold                     |                         | Shutdown Mode                                                    | 2.1    | 2.35 |      | V     |
| UVLO Hysteresis                    | V <sub>H_UVLO</sub>     |                                                                  |        | 200  |      | mV    |


**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Parameter                                            | Symbol                   | Test Conditions                                                                       | LX1689 |       |      | Units |
|------------------------------------------------------|--------------------------|---------------------------------------------------------------------------------------|--------|-------|------|-------|
|                                                      |                          |                                                                                       | Min    | Typ   | Max  |       |
| RAMP GENERATOR                                       |                          |                                                                                       |        |       |      |       |
| Max Strike / Run Frequency Ratio                     | F <sub>RAMP_STK</sub>    | Ratio to run frequency, I <sub>SNS</sub> = 0V, V <sub>SNS</sub> = 0V                  | 4      | 5     | 6    |       |
| Maximum Lamp Run Frequency                           | F <sub>RAMP_RUNMAX</sub> | Lamp is ignited; I <sub>R</sub> =10K                                                  | 250    | 450   |      | KHz   |
| Lamp Run Frequency                                   | F <sub>LAMP_RUN</sub>    | Lamp is ignited ;T <sub>A</sub> = 25°C                                                | 63     | 65    | 67   | KHz   |
| Lamp Run Frequency                                   | F <sub>LAMP_RUN</sub>    | Lamp is ignited                                                                       | 61     | 65    | 69   | KHz   |
| Lamp Run Frequency Regulation over V <sub>BATT</sub> | F <sub>LAMP_REG</sub>    | 3.3 ≤ V <sub>BATT</sub> ≤ 28V                                                         |        | 0.1   |      | %     |
| Internal Digital Dimming Burst Frequency             | F <sub>BURST</sub>       | DIV <sub>248</sub> = VDD <sub>A</sub> , DIM <sub>MODE</sub> = 0V                      |        | 254   |      | Hz    |
|                                                      |                          | DIV <sub>248</sub> = Floating, DIM <sub>MODE</sub> = 0V                               |        | 127   |      | Hz    |
|                                                      |                          | DIV <sub>248</sub> = Gnd, DIM <sub>MODE</sub> = 0V                                    |        | 63.5  |      | Hz    |
| BIAS BLOCK                                           |                          |                                                                                       |        |       |      |       |
| Voltage at Pin I <sub>R</sub>                        | V <sub>IR</sub>          | V <sub>BATT</sub> = 2.8V to 28V, I <sub>OUT</sub> = 0 to 100uA, T <sub>A</sub> = 25°C | 0.95   | 1.0   | 1.05 | V     |
| Pin I <sub>R</sub> Max Source Current                | I <sub>MAX_IR</sub>      | I <sub>R</sub> = 0V                                                                   | 100    | 700   |      | µA    |
| Voltage Reference Voltage (Internal node)            | V <sub>2P0</sub>         | T <sub>A</sub> = 25°C, reference use only                                             | 1.99   | 2     | 2.01 | V     |
| PWM BLOCK                                            |                          |                                                                                       |        |       |      |       |
| Error Amp Transconductance                           | G <sub>M_EAMP</sub>      |                                                                                       | 90     | 180   |      | µmho  |
| Error Amp Output Source Current                      | I <sub>S_EAMP</sub>      |                                                                                       | 5      | 12    |      | µA    |
| Error Amp Output Sink Current                        | I <sub>SK_EAMP</sub>     |                                                                                       | 5      | 12    |      | µA    |
| Error Amp Output High Voltage                        | V <sub>H_EAMP</sub>      | BRITE_OUT – EA_IN = 50mV                                                              | 2.5    | 2.9   |      | V     |
| Error Amp Output Low Voltage                         | V <sub>L_EAMP</sub>      | EA_IN – BRITE_OUT = 50mV                                                              |        | 0.015 | 0.5  | V     |
| Error Amp Input Offset Voltage                       | V <sub>OS_EAMP</sub>     |                                                                                       |        |       | 70   | mV    |
| Max Duty Cycle                                       | DC <sub>MAX</sub>        |                                                                                       |        | 44    |      | %     |
| Ramp Valley Voltage                                  | R <sub>VV</sub>          |                                                                                       |        | 200   |      | mV    |
| Ramp Peak Voltage                                    | R <sub>PV</sub>          |                                                                                       |        | 1.95  |      | V     |
| OUTPUT BUFFER BLOCK                                  |                          |                                                                                       |        |       |      |       |
| Output Sink Current                                  | I <sub>SK_OUTBUF</sub>   | V <sub>AOUT</sub> , V <sub>BOUT</sub> = V <sub>DD_P</sub>                             |        | 100   |      | mA    |
| Output Source Current                                | I <sub>S_OUTBUF</sub>    | V <sub>AOUT</sub> , V <sub>BOUT</sub> = 0V                                            |        | 100   |      | mA    |
| Output Rise Time                                     | T <sub>R</sub>           | C <sub>OUT</sub> = 1000pF                                                             |        | 25    | 200  | nS    |
| Output Fall Time                                     | T <sub>F</sub>           | C <sub>OUT</sub> = 1000pF                                                             |        | 25    | 200  | nS    |
| DIM_CLK INPUT                                        |                          |                                                                                       |        |       |      |       |
| Pull-up Resistance                                   |                          | To VDDA                                                                               |        | 50    |      | KΩ    |
| Input High Threshold                                 | V <sub>TH_DIM_CLK</sub>  | Conventional Dimming                                                                  |        | 0.9   | 1.4  | V     |
| Input Low Threshold                                  | V <sub>TL_DIM_CLK</sub>  | Reverse Dimming                                                                       | 0.4    | 0.9   |      | V     |
| Input High Current                                   | I <sub>IH_DIM_CLK</sub>  | DIM_CLK = 5V                                                                          |        | 45    | 70   | µA    |
| Input Low Current                                    | I <sub>IL_DIM_CLK</sub>  | DIM_CLK = 0V                                                                          |        | -65   | -100 | µA    |
| TRI-STATE LOGIC INPUTS (DIM_MODE,DIV_248)            |                          |                                                                                       |        |       |      |       |
| Low State                                            | V <sub>TL_TRI</sub>      |                                                                                       | 0.4    | 0.6   |      | V     |
| Floating State                                       | V <sub>TF_TRI</sub>      |                                                                                       | 1.2    | 1.35  | 1.8  | V     |
| High State                                           | V <sub>TH_TRI</sub>      |                                                                                       |        | 2.1   | 2.8  | V     |
| Input High Current                                   | I <sub>IH_TRI</sub>      | DIM_MODE = DIV_248 = 5V                                                               |        | 70    | 120  | µA    |
| Input Low Current                                    | I <sub>IL_TRI</sub>      | DIM_MODE = DIV_248 = 0V                                                               |        | -25   | -50  | µA    |

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Parameter                                                | Symbol                  | Test Conditions                                      | LX1689 |      |       | Units            |
|----------------------------------------------------------|-------------------------|------------------------------------------------------|--------|------|-------|------------------|
|                                                          |                         |                                                      | Min    | Typ  | Max   |                  |
| ANALOG DIMMER BLOCK                                      |                         |                                                      |        |      |       |                  |
| BRITE_IN Input Current                                   | BRITE_IN <sub>II</sub>  | BRITE_IN = 0 to 5V                                   | -1     |      | 1     | μA               |
| Conventional Dimming<br>BRITE_OUT                        |                         | BRITE_IN ≤ 0.45V                                     | 20     | 52   | 100   | mV               |
|                                                          |                         | BRITE_IN ≥ 2.05V; T <sub>A</sub> = 25°C              | 0.96   | 1.04 | 1.12  | V                |
|                                                          |                         | BRITE_IN ≥ 2.05V                                     | 0.94   | 1.04 | 1.14  | V                |
| Reverse Dimming<br>BRITE_OUT                             |                         | BRITE_IN ≤ 0.45V; T <sub>A</sub> = 25°C              | 0.98   | 1.06 | 1.14  | V                |
|                                                          |                         | BRITE_IN ≤ 0.45V                                     | 0.96   | 1.06 | 1.16  | V                |
|                                                          |                         | BRITE_IN ≥ 2.05V                                     | 10     | 62   | 120   | mV               |
| DIGITAL DIMMER BLOCK                                     |                         |                                                      |        |      |       |                  |
| Conventional Dimming<br>Duty Cycle                       |                         | Minimum Duty Cycle; BRITE_IN ≤ 0.55V                 | 2      | 10   | 15    | %                |
|                                                          |                         | Maximum Duty Cycle; BRITE_IN =1.90V                  | 85     | 92   | 100   | %                |
|                                                          |                         | Maximum Duty Cycle; BRITE_IN ≥ 1.95V                 | 100    |      |       | %                |
| Reverse Dimming<br>Duty Cycle                            |                         | Maximum Duty Cycle; BRITE_IN ≤ 0.55V                 | 100    |      |       | %                |
|                                                          |                         | Maximum Duty Cycle; BRITE_IN = 0.6V                  | 85     | 92   | 100   | %                |
|                                                          |                         | Minimum Duty Cycle; BRITE_IN ≥ 1.95V                 | 2      | 10   | 15    | %                |
| TIMING GENERATOR BLOCK                                   |                         |                                                      |        |      |       |                  |
| Number of Lamp Return Current<br>Cycles before Run Mode  | N <sub>IGNITE</sub>     | To switch to Run Mode                                |        | 8    |       | Cycles           |
| I_SNS Run Mode Checking Interval                         |                         | Lamp return current cycles, 8192 x 1 /f <sub>o</sub> |        | 126  |       | mS               |
| Fault Comparator Threshold Voltage                       |                         | I_ SNS Open Lamp Fault Detect, T <sub>A</sub> =25°C  | 250    | 305  | 350   | mV <sub>PK</sub> |
| Number of Strike sweep Attempts<br>Before Fault Shutdown | N <sub>STRK_FAULT</sub> | FLAMP Sweep Cycles, I_ SNS = 0V_SNS = 0V             |        | 15   |       |                  |
| Power On Delay Before Strike                             | T <sub>D_PWRON</sub>    | 16384 X Lamp Run Period                              |        | 252  |       | ms               |
| Number of Sweeping Strike Frequency<br>Steps per Attempt |                         |                                                      |        | 1024 |       | Steps            |
| Number of Output Pulses per Striking<br>Step             |                         |                                                      |        | 16   |       | Cycles           |
| LAMP FEEDBACK CONDITIONING BLOCK                         |                         |                                                      |        |      |       |                  |
| I_SNS Input Current                                      | I_SNS <sub>IIN</sub>    | I_SNS =10V                                           |        | 80   | 150   | μA               |
|                                                          |                         | I_SNS = -10V                                         |        | -200 | -350  | μA               |
| OV_SNS Input High Threshold                              | V <sub>TH_OV_SNS</sub>  | Active Over Voltage Protection                       |        | ± 2  | ± 2.2 | V <sub>PK</sub>  |
| OV_SNS Input Low Threshold                               | V <sub>TL_OV_SNS</sub>  | Inactive Over Voltage Protection                     | ± 1.8  | ± 2  |       | V <sub>PK</sub>  |
| OV_SNS Input Current                                     | OV_SNS <sub>IIN</sub>   | OV_SNS = 10V                                         |        | 260  | 400   | μA               |
|                                                          |                         | OV_SNS = -10V                                        |        | -320 | -450  | μA               |
| OC_SNS Input High Threshold                              | V <sub>TH_OC_SNS</sub>  | Active Over Current Protection                       |        | ± 2  | ± 2.2 | V <sub>PK</sub>  |
| OC_SNS Input Low Threshold                               | V <sub>TL_OC_SNS</sub>  | Inactive Over Voltage Protection                     | ± 1.8  | ± 2  |       | V <sub>PK</sub>  |
| OC_SNS Input Current                                     | OC_SNS <sub>IIN</sub>   | OC_SNS = 10V                                         |        | 45   | 80    | μA               |
|                                                          |                         | OC_SNS = -10V                                        |        | -110 | -180  | μA               |
| Full Wave Rectifiers RMS Transfer                        | I_SNS <sub>RMS</sub>    | I_SNS = 0.3VDC, T <sub>A</sub> = 25°C                | 0.27   | 0.31 | 0.35  | V                |
|                                                          |                         | I_SNS = 2.0VDC, T <sub>A</sub> = 25°C                | 1.95   | 2    | 2.05  | V                |
|                                                          |                         | I_SNS = -0.3VDC, T <sub>A</sub> = 25°C               | 0.24   | 0.3  | 0.36  | V                |
|                                                          |                         | I_SNS = -2.0VDC, T <sub>A</sub> = 25°C               | 1.75   | 1.9  | 2.05  | V                |





### Third Generation CCFL Controller

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## BLOCK DIAGRAM





## TYPICAL APPLICATION

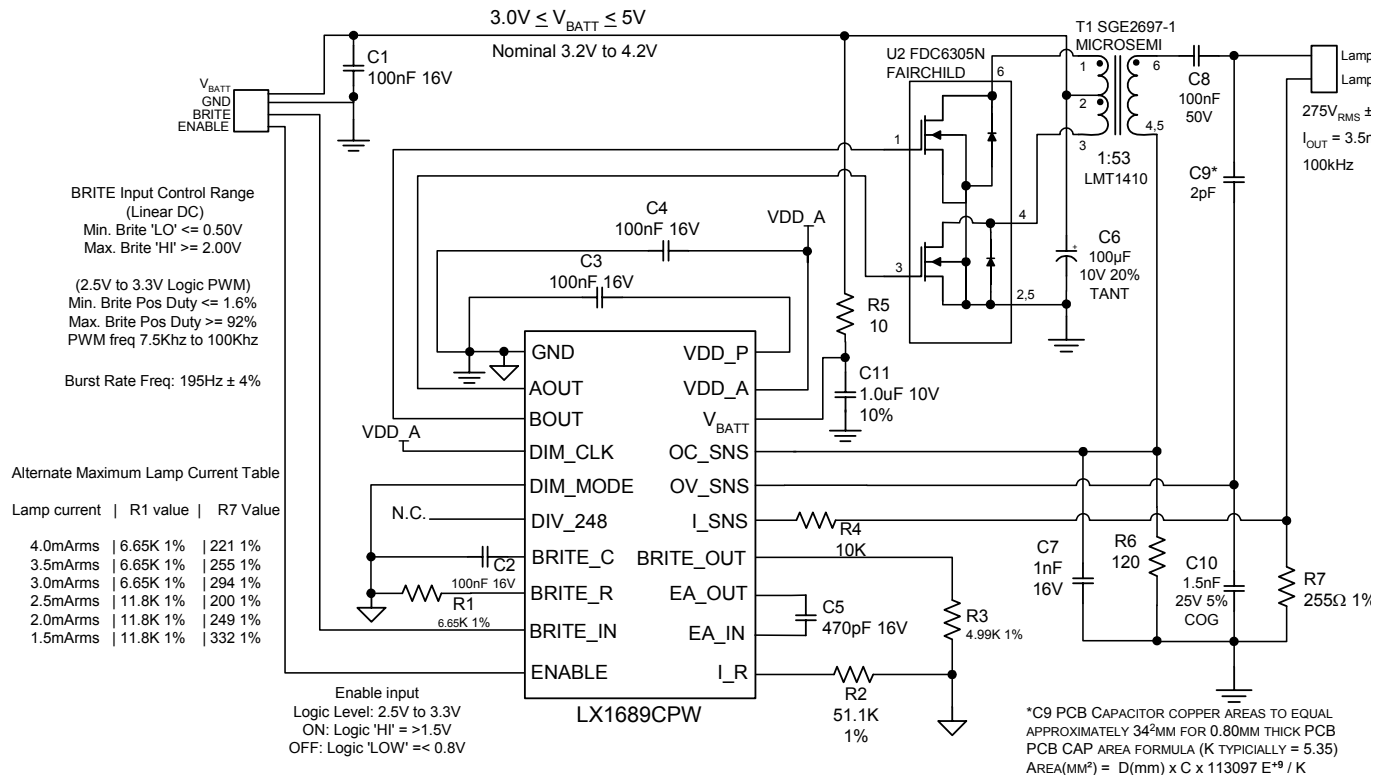


FIGURE 2 – LX1689 Typical 1W Application

## DIMMING TABLE

| DIM_MODE            | DIM_CLK               | DIMMING MODE                                      | DIMMING POLARITY* |
|---------------------|-----------------------|---------------------------------------------------|-------------------|
| VDD_A               | External Clock Source | External Burst Dimming from divided DIM_CLK input | Conventional      |
| Floating or VDD_A/2 | VDD_A                 | Analog Dimming                                    | Conventional      |
| Floating or VDD_A/2 | GND                   | Analog Dimming                                    | Reverse           |
| GND                 | VDD_A                 | Internal Burst Dimming from divided Run Frequency | Conventional      |
| GND                 | GND                   | Internal Burst Dimming from Divided Run Frequency | Reverse           |

\* Conventional polarity means that the lamp brightness increases with increasing voltage on the BRITE\_IN pin. Reverse polarity means that brightness decreases with increasing voltage.





## PRODUCTION DATA SHEET

## APPLICATION



**DESCRIPTION**
**FEATURE REVIEW**
**On-Chip LDO Regulators**

Two LDO regulators extend the input voltage range of the IC up to 28 Volts without using external circuitry as was required with our previous controllers.

**Under Voltage Lockout**

If the battery input voltage is too low for the controller to function properly, it will turn itself off, preventing spurious operation. If the battery voltage falls to less than 1V where UVLO is no longer guaranteed, 10K pull down resistors on the A<sub>OUT</sub> and B<sub>OUT</sub> pins insure the external power FETs cannot be biased on.

**Power On Delay**

A power up reset delays A<sub>OUT</sub> and B<sub>OUT</sub> turn on for approximately 16384 x 1/f<sub>O</sub> milliseconds after power is applied. This gives extra time for the BRITE\_IN source voltage to stabilize so the lamp is not inadvertently powered up at high brightness and then suddenly lowered, creating an undesirable light flash.

**Enhanced BRITE Conditioning Circuitry**

The BRITE\_IN input is now enhanced to accept either DC voltage or logic PWM signals. When PWM signals are input, their levels are clipped at 2V and 0.5V so lamp current will not be affected by variations in logic signal level. In addition, the BRITE\_C pin permits filtering DC inputs and converting high frequency PWM inputs to DC voltages with the addition of only a single external capacitor. A low frequency (less than 500Hz) PWM signal can be used to directly modulate the duty cycle of the lamp current. In this case the capacitor at BRITE\_C is not installed.

**Digital or Analog Dimming Modes**

A DIM\_MODE input pin selects either Analog or Digital mode. In Analog mode DC voltage at BRITE\_IN controls lamp current amplitude. In Digital mode it controls digital dimming duty cycle with amplitude fixed at a value set by the external current scaling resistor (BRITE\_R). When in Digital mode, the dimming burst frequency can be synchronous to lamp current by selecting internal clocking, or to an external clock that may be a multiple of the video vertical frame rate. With an external clock source, three burst rate selections are available by programming the DIV\_248 input to divide the source clock by 2,4, or 8. This clock source is further divided by 64 generating the internal burst ramp waveform. Using the internal clock as source the DIV\_248 input changes to divide by 4, 8, or 16. This feature allows the designer to set a burst frequency in the range of 100 to 500Hz. The external clock source must not be interrupted unless the BRITE\_IN is set ≥ 2V or the lamp will extinguish.

**Brightness Polarity Control**

In Analog dimming mode or internal Digital Dimming, the IC can be programmed to either increase or decrease lamp current amplitude as a function of increasing signal at the BRITE\_IN pin by simply connecting the DIM\_CLK input to ground or VDD\_A or open(see Dimming Table). If External Digital dimming mode is used, lamp current amplitude is constant and its duty cycle is always directly proportional to DC input voltage and / or PWM duty cycle at the BRITE\_IN pin.

**Lamp Current Compensation**

The BRITE\_OUT pin outputs a precision current that is proportional to the BRITE\_IN signal. This current can be applied to a precision resistor to develop the brightness control voltage at the error amplifiers non-inverting input. Since the output is constant current, designers can easily compensate lamp current with respect to temperature, input voltage, ambient or lamp light output, and combinations of these conditions by using various temperature or light sensitive components in combination with resistors. This capability is very useful in automotive and outdoor applications where operating temperatures and ambient light vary over wide ranges. See functional pin description for details.

**Strike Voltage Generation**

Improved strike voltage generation circuits ramp strike voltage to 5X f<sub>O</sub> and repeats it's cycle unless excessive high voltage is sensed at OV\_SNS. If OV\_SNS is detected during strike, strike voltage will not ramp and will hold the current voltage until total strikes lamp cycles numbers reach 245,760. Strike potential is removed immediately when the lamp strikes or if the time limit is reached.

**Strike Detection**

The LX1689 includes a new lamp strike detection scheme that saves a package pin and three external components. Internal circuits monitor lamp current pulses at the I\_SNS input to determine if the lamp strikes and if it stays ignited once operational.

**Fault Time Out**

If the lamp fails to ignite with in approximately 1.6 seconds (depending on Run Frequency) at maximum strike potential, or if it extinguishes while enabled, or the external clock frequency at the DIM\_CLK pin terminates, the output drive is shut down and the BRITE\_C pin is driven high. This pin can be monitored with a CMOS gate to obtain a logical indication that a lamp fault has occurred. It is especially useful in multiple lamp applications or for system diagnostic input.

The voltage on pin BRITE\_C will vary directly with BRITE input voltage, but does not exceed 1.2V unless a fault condition occurs.

**On Chip Rectifier**

Integrating full wave rectifiers for each of three lamp inputs has significantly reduced lamp feedback component count. Current Sense (I\_SNS), Over Current Sense (OC\_SNS) and Over Voltage Sense (OV\_SNS) signals are now detected using only one external scaling resistor or capacitor each. Rectification accuracy is improved with high performance on chip rectifiers to provide better lamp current and voltage regulation.

**Complete Fault Protection**

In addition to the faulty lamp time out, lamp open, lamp shorted, and either lamp terminal shorted to ground are detected. Open circuit voltage can never go higher than the preset maximum strike potential and total current from the circuit is safely limited with a scaling resistor. UL safety specifications can now be easily met in any application.

**DESCRIPTION (CONTINUED)**
**LX1689 OPERATION**

Four operating modes: Power On Delay, Strike, Run, and Fault modes are employed by the LX1689. Upon power up or ENABLE going true, Power On Delay is automatically invoked. Immediately after termination of Power On Delay, or ENABLE going true, strike mode is entered. After a successful strike, e.g. lamp is ignited, run mode is entered. If ignition is unsuccessful, or if the lamp extinguishes while running, Fault mode is entered. Lamp ignition is determined by monitoring the lamp current feedback voltage at pin I\_SNS. Lamp current cycles are counted from the beginning of Strike mode. If 8 or more complete cycles occur the lamp is declared ignited. If less than 8, the lamp is considered not ignited and Strike mode continues until ignition is detected or strike time out is reached.

After run mode is entered lamp current cycles are sampled every  $8192 \times 1/f_o$  to determine that the lamp has not inadvertently extinguished. If at least 8 lamp current pulses are counted in each sample, Run mode is maintained. Otherwise, Fault mode is entered. Strike mode can be entered only once for each on/off cycle of either V\_BATT or ENABLE. This insures that even intermittent lamp failures cannot cause the module to continuously output maximum strike voltage.

**Power ON Delay Mode**

All functions are activated except that AOUT and BOUT are inhibited. Delay is  $16384 \times 1/f_o$  determined by counting Ramp clocks. The first of 16 sweeps is decoded as the power on delay period. The subsequent 15 sweeps are used for controlling the Ramp generator during Strike Mode. Power on delay is activated at every V\_BATT power up sequence and ENABLE sequence.

**Strike Mode**

Entered from Power On Delay, or upon an ENABLE sequence. Control of the Ramp Generator frequency is switched to a DAC output. Frequency is increased in a saw tooth fashion from normal run value to as high as five times that value, for up to 15 sweeps. If while strike frequency is ramping up, the over voltage set point at OV\_SNS is detected, strike frequency will freeze at that value until either the lamp strikes or the timeout is reached. Strike Mode is terminated by reaching 15 sweep counts or by detecting lamp ignition. If strike is successful, Run Mode is entered. If unsuccessful, Fault mode is entered, a fault is declared and the A & B outputs are shut off.

The purpose of sweeping lamp frequency up during strike is to operate at the unloaded resonant frequency of the transformer and lamp load. This generates the high lamp striking voltage required, since at resonance, output voltage from the transformer will increase to any value needed to cause ignition. A capacitive voltage divider provides output voltage feedback to the OV\_SNS pin, which freezes Strike Frequency to limit maximum output voltage to a safe value.

Since strike frequency is held constant once the LX1689 senses maximum safe output voltage, maximum strike potential is continuously impressed across the lamp for the entire strike period.

Because strike frequency is ramped up rather than simply stepped, the entire range of possible self-resonant frequencies is covered. Transformer manufacturing is simplified and parasitic panel capacitance values are no longer critical. The 5:1 strike frequency range easily covers the self-resonant frequency of all practical lamp assembly and transformer combinations.

The only way to re-initiate the strike process is to either cycle V\_BATT or ENABLE off and on.

If ignition is successful, ramp frequency immediately returns to its normal run value.

**Run Mode**

Entered only by detection of a successful Strike. Ramp generator frequency control is immediately switched from DAC output to a fixed reference that sets the normal run frequency. During Run mode, the Fault Detect Counter is reset approximately every  $8192 \times 1/f_o$ . The lamp current cycle counter is monitored to insure at least 8 current cycles received during each period. If less than 8, the lamp is considered extinguished and the Fault Mode is entered.

**Fault Mode**

Fault Mode may be entered from either Strike or Run Mode as described above. In Fault Mode, the A & B output drivers are forced low and the BRITE\_C pin is driven to VDD\_A to indicate the fault condition. Fault mode may be cleared by cycling ENABLE off then on, or by removing and applying V\_BATT. External load on the BRITE\_C pin is limited to a filter capacitor and single CMOS gate input.

**DESIGN PROCEDURE**
**Selecting the I\_R resistor value**

This resistor determines the frequency of the on chip oscillator. The output of the oscillator, RAMP\_C, controls all timing functions. It must be chosen first, and will be in the range of 10K to 150K ohms. The output frequency approximated by the following formula:  $R_{I\_R} = 5.24E^9 / FLAMP_{OUT(Hz)}$

RAMP\_C frequency is twice lamp output current frequency.

**Driving the BRITE\_IN Input**

BRITE\_IN can be a DC voltage, a low frequency PWM signal that produces direct digital dimming, or a higher frequency PWM signal that is converted to a proportional DC level by adding a filter capacitor at the BRITE\_C pin. 100% duty cycle corresponds to 1.1 volt, and 0% duty cycle corresponds to zero volts at the BRITE\_C pin. Maximum BRITE\_IN input frequency for PWM inputs is 100 KHz, but when converting frequencies above 25 KHz to DC, some accuracy is lost. The BRITE\_IN input circuitry includes on-chip active voltage clamps that ignore input voltage greater than 2.0V and less than 0.5V. This allows the use of digital PWM input signals where brightness is dependent only on duty cycle, with no contribution

**DESCRIPTION (CONTINUED)**

due to varying input signal amplitude. Input impedance is very high so BRITE\_IN can also be driven from a 100K potentiometer with no offset error.

**BRITE\_R and BRITE\_OUT Resistor values.**

The BRITE\_OUT pin is the output from the BRITE\_IN signal processor. It is a linear current source that varies from 0 to the current value established at pin BRITE\_R multiplied by the DC voltage at pin BRITE\_C. The optimum value for BRITE\_R is usually 10K ohms. The BRITE\_OUT voltage range can be scaled from 300mV to 2.0V. However, it is recommended that the scaling of BRITE\_OUT (including Analog mode BRITE\_IN range) be within 400mV to 1.2V. Maximum voltage correlates to full brightness settings. It is the ratio of the two resistors multiplied by the voltage at BRITE\_C:

$$V_{BRITE\_OUT} = V_{BRITE\_C} (R_{BRITE\_OUT} / R_{BRITE\_R})$$

In some applications, a precision 10K resistor is connected from BRITE\_OUT and BRITE\_R to ground to develop 1.0V to represent maximum lamp brightness. In Analog mode the BRITE\_OUT voltage potential is proportional to BRITE\_IN. The minimum brightness setting at BRITE\_IN corresponds to the minimum voltage at BRITE\_OUT. In digital mode, BRITE\_IN has no effect on BRITE\_OUT.

Because the BRITE\_OUT output is a linear current source, you can place other components, such as a thermistor or photo resistor, at this pin to generate complex functions for controlling brightness. For example; use a PWM input at the BRITE\_IN pin to control dimming, and boost analog lamp current amplitude at cold lamp temperature with a thermistor at the BRITE\_OUT pin. This will help warm the lamp faster at start up so final brightness is reached sooner.

**SETTING THE OUTPUT CURRENT.**

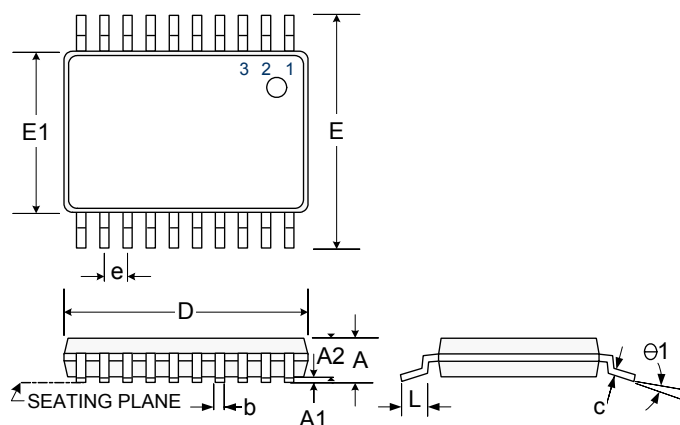
Referring to the application examples figures 2 and 3. The current setting resistor(s) are R7, and R19 and R20 respectively. The value these resistor(s) are in the range of 200 to 400ohms. The following formula can be used to determine the current setting resistor value. Use 1180 for Digital mode and 1260 for analog dim.

$$R_{SNS} = 1180 \text{ or } 1260 \times R_{BRITE\_OUT} / I_{OUT}(mA_{RMS}) \times R_{BRITE\_R}$$

In the 1W burst dimming application example shown in figure 2 the output current is set for nominally 3.5mA.  $R_{SNS}$  is calculated using the formula above as follows:

$$R_{SNS} = 1180 \times 4990 / 3.5 \times 6550 = 256.8 \text{ ohms}$$

A standard value of 255 ohms was chosen. It is recommended to keep the value of the sense resistor in the range of 200 to 400 ohms as stated above. If calculated value exceeds 400 ohms its best to increase the value of the  $R_{BRITE\_R}$  resistor.

**MECHANICAL DRAWING**
**PW 20-Pin Thin Small Shrink Outline (TSSOP)**


| Dim    | MILLIMETERS |      | INCHES    |       |
|--------|-------------|------|-----------|-------|
|        | MIN         | MAX  | MIN       | MAX   |
| A      | -           | 1.10 | -         | 0.043 |
| A1     | 0.05        | 0.15 | 0.002     | 0.006 |
| A2     | 0.80        | 1.05 | 0.031     | 0.041 |
| b      | 0.19        | 0.30 | 0.007     | 0.012 |
| c      | 0.09        | 0.20 | 0.004     | 0.008 |
| D      | 6.40        | 6.60 | 0.252     | 0.260 |
| E      | 6.25        | 6.55 | 0.246     | 0.258 |
| E1     | 4.30        | 4.50 | 0.169     | 0.177 |
| e      | 0.65 BSC    |      | 0.026 BSC |       |
| L      | 0.45        | 0.75 | 0.018     | 0.030 |
| theta1 | 0°          | 8°   | 0°        | 8°    |
| *LC    | -           | 0.10 | -         | 0.004 |

\* Lead Coplanarity

**Note:**

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.



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