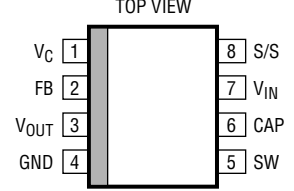


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ Voltage .....	10V
S/S Voltage .....	7V
FB Voltage .....	10V
$V_{OUT}$ Voltage .....	5.5V
Junction Temperature .....	125°C
Operating Temperature Range (Note 2) ..	–40°C to 85°C
Storage Temperature Range .....	–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p><math>V_C</math> 1 8 S/S FB 2 7 <math>V_{IN}</math> <math>V_{OUT}</math> 3 6 CAP GND 4 5 SW</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 90^{\circ}\text{C/W}</math></p>	ORDER PART NUMBER
	LT1306ES8
	S8 PART MARKING
	1306

Consult factory for Industrial and Military grade parts.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{IN} = 2.5\text{V}$ ,  $V_{S/S} = V_{IN}$ ,  $V_C$  open unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage	Measured at the FB Pin ●	1.22	1.24	1.26	V
Reference Line Regulation	$1.8\text{V} \leq V_{IN} \leq 7\text{V}$		0.002	0.1	%/V
FB Input Bias Current	$V_{FB} = V_{REF}$ ●		10	25	nA
Error Amplifier Transconductance	$\Delta I = \pm 0.2\mu\text{A}$	80	150	220	$\mu\Omega^{-1}$
Error Amplifier Output Source Current	$V_{FB} = 1\text{V}$ , $V_C = 0.8\text{V}$	5	7.5	11	$\mu\text{A}$
Error Amplifier Output Sink Current	$V_{FB} = 1.5\text{V}$ , $V_C = 0.8\text{V}$	5	7.5	11	$\mu\text{A}$
Error Amplifier Output Clamp Voltage	$V_{FB} = 1\text{V}$	1.18	1.28	1.38	V
$V_{IN}$ Undervoltage Lockout Threshold		1.55		1.8	V
Idle Mode Output Leakage Current	$V_{FB} = 1.5\text{V}$ , $V_{OUT} = 5.5\text{V}$ , $V_{SW} = 1.7\text{V}$ ●		6	15	$\mu\text{A}$
Output Source Current in Shutdown	$V_{OUT} = 0\text{V}$ , $V_{IN} = V_{SW} = 7\text{V}$ , $V_{CAP} = 7.2\text{V}$ , $V_{S/S} = 0\text{V}$ ●			–3	$\mu\text{A}$
Switching Frequency	$1.8\text{V} \leq V_{IN} \leq 7\text{V}$ , $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ●	260	310	415	kHz
	$1.8\text{V} \leq V_{IN} \leq 7\text{V}$ , $T_A = -40^{\circ}\text{C}$	225	305	390	kHz
Maximum Duty Cycle	$V_{FB} = 1\text{V}$ , $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	80	90		%
	$V_{FB} = 1\text{V}$ , $T_A = -40^{\circ}\text{C}$	65	80		%
Switch Current Limit	Duty Cycle = 0.1 (Note 3)	2.3			A
	Duty Cycle = 0.8 (Note 3)	2.0			A
Burst Mode Operation Switch Current Limit			250		mA
Switch $V_{CESAT}$	$I_{SW} = 2\text{A}$		0.45	0.575	V
Rectifier $V_{CESAT}$	$I_{SW} = 2\text{A}$		0.49	0.675	V
Stepdown Mode Rectifier Voltage	$V_{OUT} = 0\text{V}$ , $I_{SW} = 1\text{A}$	$0.3 + V_{IN}$		$0.7 + V_{IN}$	V
	$V_{OUT} = 2.2\text{V}$ , $I_{SW} = 1\text{A}$	1.3		1.8	V
Switch and Rectifier Leakage Current	$V_{OUT} = 0\text{V}$ , $V_{IN} = V_{SW} = 7\text{V}$ , $V_{CAP} = 7.2\text{V}$ , $V_{S/S} = 0\text{V}$ ●		0.1	20	$\mu\text{A}$

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 2.5\text{V}$ ,  $V_{S/S} = V_{IN}$ ,  $V_C$  open unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/S Pin Current	$V_{S/S} = V_{IN}$ $V_{S/S} = 0\text{V}$			6 -3	$\mu\text{A}$ $\mu\text{A}$
Shutdown Pin Input High Voltage		1.2			V
Shutdown Pin Input Low Voltage				0.45	V
Shutdown Delay		12	20	50	$\mu\text{s}$
Synchronization Frequency Range		425		500	kHz
Operating Supply Current			4.5	8	mA
Quiescent Supply Current	$V_{S/S} = V_{IN}$ , $V_{FB} = 1.5\text{V}$	●	160	250	$\mu\text{A}$
Shutdown Supply Current	$V_{S/S} = 0\text{V}$		9	16	$\mu\text{A}$
CAP Pin Leakage Current	$V_{IN} = V_{CAP} = 7\text{V}$ , $V_{S/S} = 2.5\text{V}$ , $I_{SW} = 0$	●		10	$\mu\text{A}$
Output Boost-to-Stepdown Threshold			$V_{IN}$		V
Output Stepdown-to-Boost Threshold			$V_{IN} - 0.1$		V

**Note 1:** Absolute Maximum Ratings are those values beyond which the life to the device may be impaired.

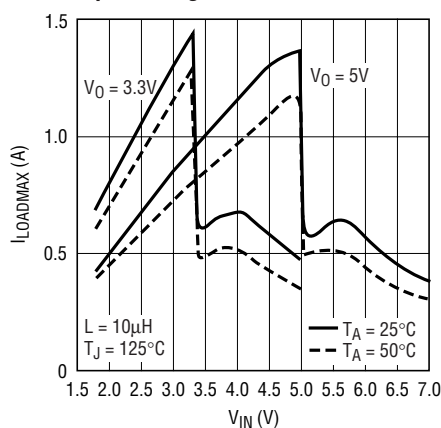
**Note 2:** The LT1306E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating

temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Switch current limit guaranteed by design/correlation to static tests.

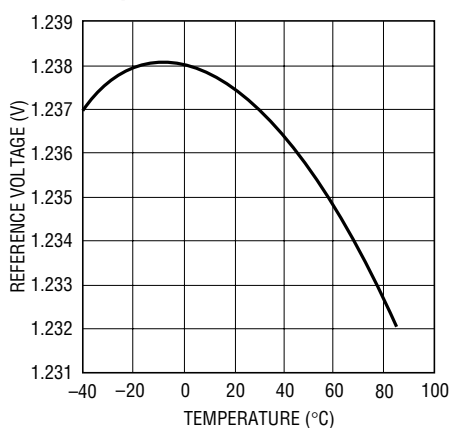
## TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Load Current vs Input Voltage



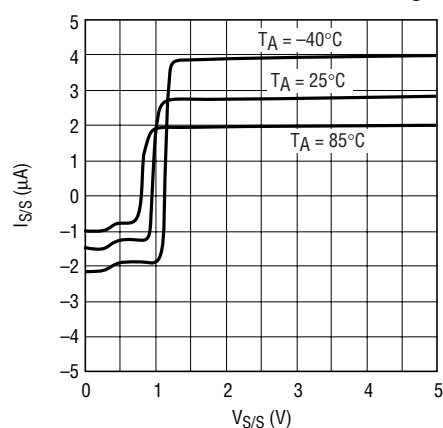
1306 • G01

Reference Voltage vs Temperature



1306 • G02

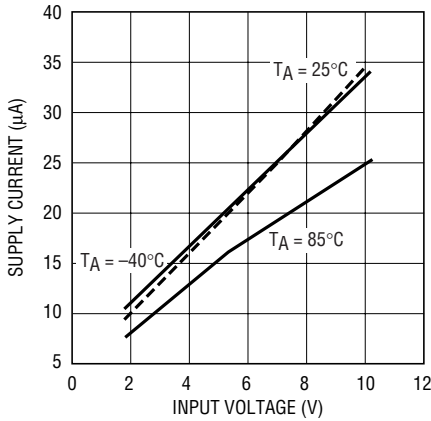
S/S Pin Current vs S/S Pin Voltage



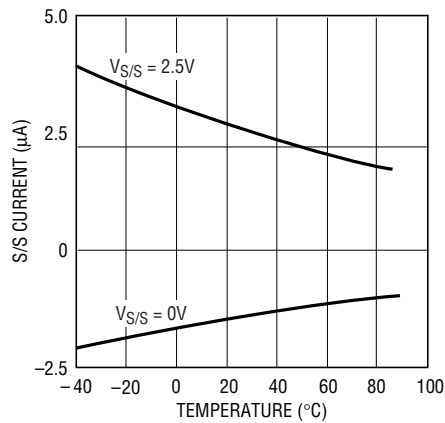
1306 • G03

# TYPICAL PERFORMANCE CHARACTERISTICS

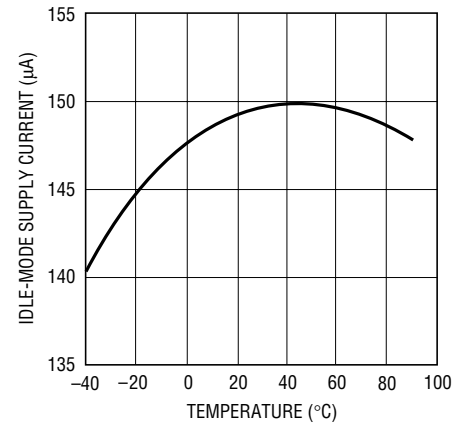
**Shutdown Supply Current vs Input Voltage**



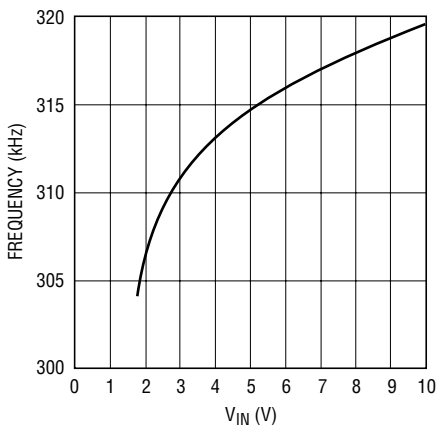
**S/S Pin Current vs Temperature**



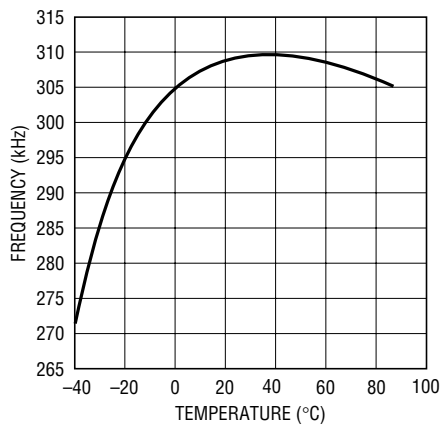
**Idle-Mode Supply Current vs Temperature**



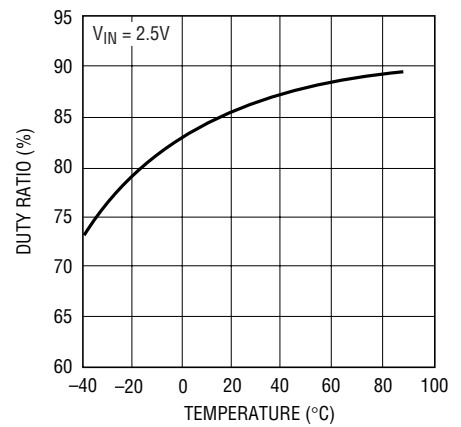
**Oscillator Frequency Line Regulation**



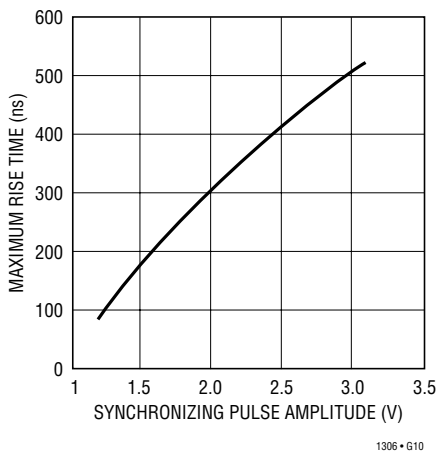
**Frequency vs Temperature**



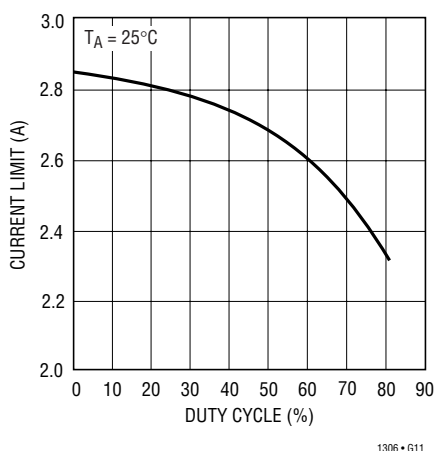
**Maximum Duty Ratio**



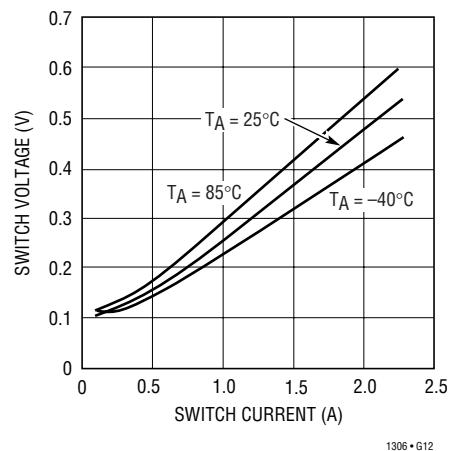
**Maximum Allowable Rise Time of Synchronizing Pulse**



**Current Limit vs Duty Cycle**

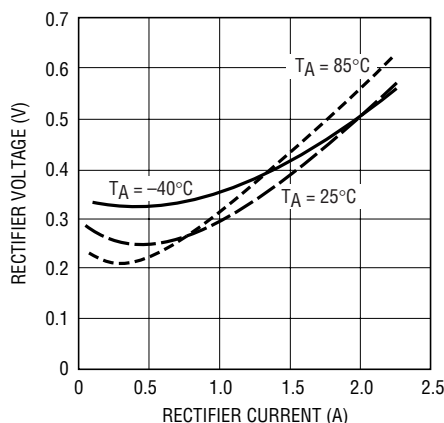


**Switch Saturation Voltage vs Current**



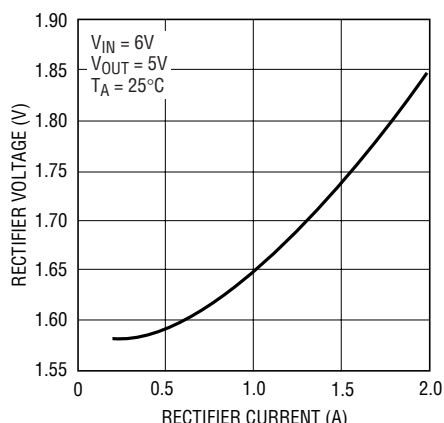
# TYPICAL PERFORMANCE CHARACTERISTICS

**Rectifier Saturation Voltage vs Current**



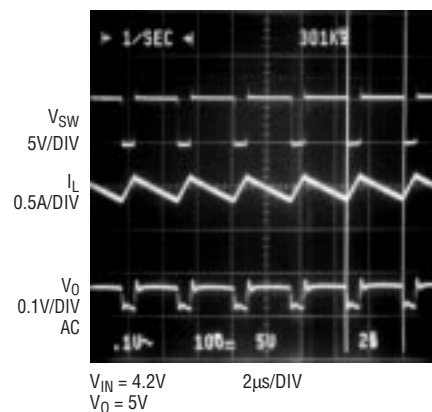
1306 • G13

**Stepdown-Mode Rectifier Voltage vs Current**

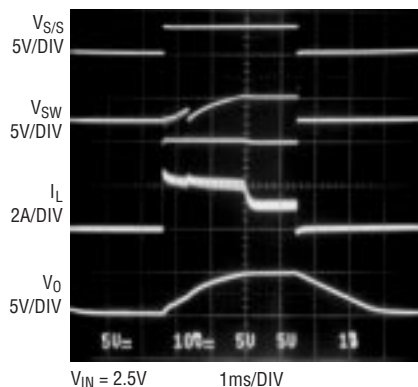


1306 • G14

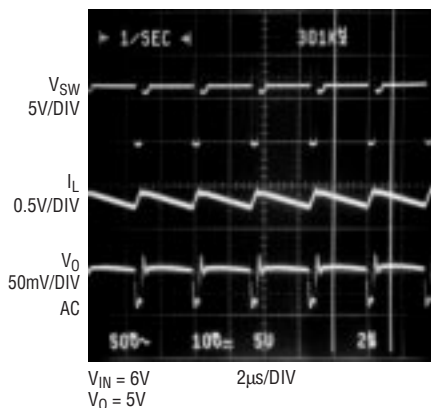
**Continuous-Conduction Mode Switching Waveforms in Boost Operation**



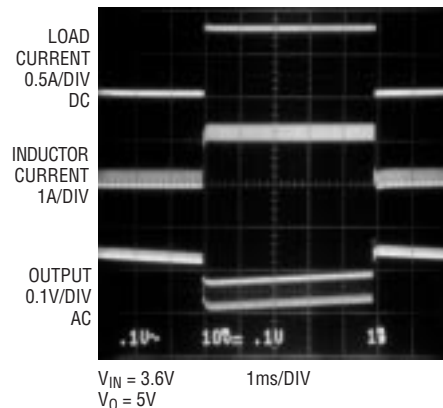
**Start-Up to Shutdown Transient Response\***



**Continuous-Conduction Mode Switching Waveforms in Stepdown Mode**



**Transient Response of the Converter in Figure 1 with a 50mA to 800mA Load Step**



\* Notice that the Input Start-Up Current is well Controlled and the Output Voltage Falls to Zero in Shutdown.

## PIN FUNCTIONS

**V<sub>C</sub> (Pin 1):** Compensation Pin for Error Amplifier. V<sub>C</sub> is the output of the transconductance error amplifier. Loop frequency compensation is done by connecting an RC network from the V<sub>C</sub> pin to ground.

**FB (Pin 2):** Inverting Input of the Error Amplifier. Connect the resistor divider tap here. Set output voltage according to  $V_{OUT} = 1.24V (1 + R_1/R_2)$ .

**V<sub>OUT</sub> (Pin 3):** Output of the Switching Regulator and Emitter of the Synchronous Rectifier. Connect appropriate output capacitor from here to ground. V<sub>OUT</sub> must be kept below 5.5V.

**GND (Pin 4):** Ground. Connect to local ground plane.

**SW (Pin 5):** Switch Pin. The collectors of the grounded power switch and the synchronous rectifier. Keep the SW trace as short as possible to minimize EMI.

**CAP (Pin 6):** Power Supply to the Synchronous Rectifier Driver. The bootstrap capacitor and the blocking diode are tied to this pin. The CAP voltage switches between a low level of  $V_{IN} - V_D$  to a high level determined by the V<sub>SW</sub> high level.

**V<sub>IN</sub> (Pin 7):** Supply or Battery Input Pin. Must be closely bypassed to ground plane.

**S/S (Pin 8):** Shutdown and Synchronization Pin. Shutdown is active low with a typical threshold of 0.9V. For normal operation, the S/S pin is tied to V<sub>IN</sub>. To externally synchronize the switching regulator, drive the S/S pin with a pulse train.

## BLOCK DIAGRAM

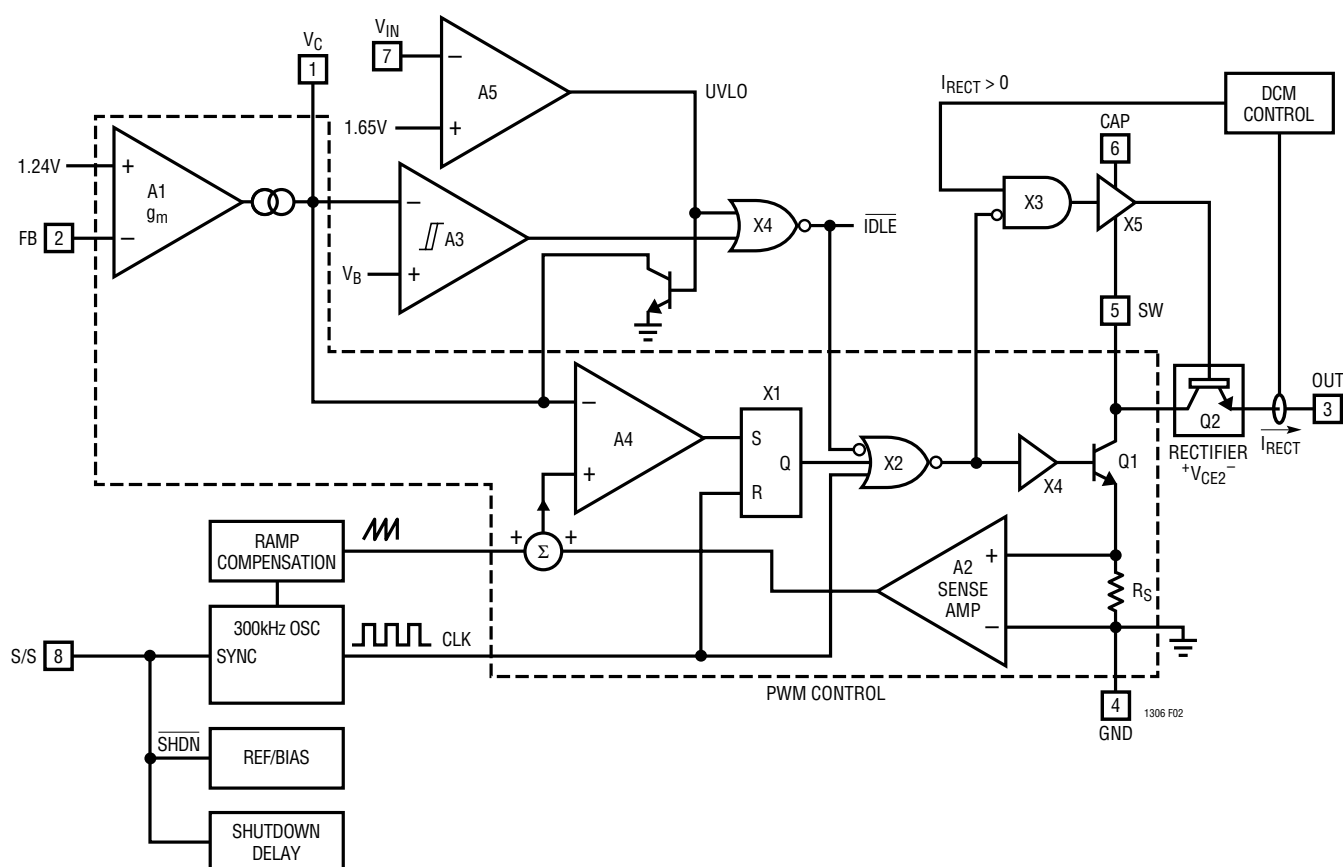


Figure 2. LT1306 Block Diagram

## OPERATION

The LT1306 is a fixed frequency current mode PWM regulator with integrated power transistor Q1 and synchronous rectifier Q2.

In the Block Diagram, Figure 2, the PWM control circuit is enclosed within the dashed line. It consists of the current sense amplifier (A2), the oscillator, the compensating ramp generator, the PWM comparator (A4), the logic (X1 and X2), the power transistor driver (X4) and the main power switch (Q1). Notice that the clock (CLK) “blanks” Q1 conduction. The internal oscillator frequency is 300kHz.

The pulse width of the clock determines the maximum on duty ratio of Q1. In the LT1306 this is set to 88%. Q1 turns on at the trailing edge of the clock pulse. To prevent subharmonic oscillation above 50% duty ratio, a compensating ramp (generated from the oscillator sawtooth) is added to the sensed Q1 current. Q1 is turned off when this sum exceeds the error amplifier A1 output,  $V_C$ . Q1's absolute current limit is reached when  $V_C$ 's upward excursion is clamped internally at 1.28V.

The error amplifier output,  $V_C$ , determines the peak switch current required to regulate the output voltage.  $V_C$  is a measure of the output power. At heavy loads, the average and the peak inductor currents are both high.  $V_C$  moves to the upper end of its operating range and the LT1306 operates in continuous conduction mode (CCM).

As load decreases, the average inductor current decreases. In CCM, the peak-to-peak inductor current ripple to the first order depends only on the inductance, the input and the output voltages. When the average inductor current falls below 1/2 of the peak-to-peak inductor current ripple, the converter enters discontinuous conduction mode (DCM). The switching frequency remains constant except that the inductor current always returns to zero within each switching cycle.

In both CCM and DCM, the output voltage is regulated with negative feedback. A1 amplifies the error voltage between the internally generated 1.24V reference and the attenuated output voltage. The RC network from the  $V_C$  pin to ground provides the loop compensation.

Further reduction in the load moves  $V_C$  towards the lower end of its operating range. Both the peak inductor current

and switch Q1's on-time decrease. Hysteretic comparator A3 determines if  $V_C$  is too low for the LT1306 to operate efficiently. As  $V_C$  falls below the trip voltage  $V_B$ , the output of A3 goes high. All circuits except the error amplifier, comparators A3 and A5, and the rectifier driver control X5, are turned off. After the remaining energy stored in the inductor is delivered to the output through the synchronous rectifier Q2, the LT1306 stops switching. In this idle state, the LT1306 draws only 160 $\mu$ A from the input. With switching stopped and the load being powered by the output filter capacitor, the output voltage decreases.  $V_C$  then starts to increase. Q1 does not start to switch until  $V_C$  rises above the upper trip point of A3. The LT1306 again delivers power to the output as a current mode PWM converter except that the switch current limit is only about 250mA due to the low value of  $V_C$ . If the load is still light, the output voltage will rise and  $V_C$  will fall, causing the converter to idle again. Power delivery therefore occurs in bursts. The on-off cycle frequency, or burst frequency, depends on the operating conditions, the inductance and the output filter capacitance. The output voltage ripple in Burst Mode operation is usually higher than either CCM or DCM operation. Burst Mode operation increases light load efficiency because it delivers more energy to the output during each clock cycle than is possible with DCM operation's extremely low peak switch current. This allows fewer switching cycles per unit time to maintain a given output. Chip supply current therefore becomes a small fraction of the total input current.

The synchronous rectifier is represented as NPN transistor, Q2, in the Block Diagram (Figure 2). A rectifier drive circuit, X5, supplies variable base drive to Q2 and controls the voltage across the rectifier. The supply voltage,  $V_{CAP}$ , for the driver is generated locally with the bootstrap circuit, D1 and C1 (Figure 1). When Q1 is on, the bootstrap capacitor C1 is charged from the input to the voltage  $V_{IN} - V_{D1(ON)} - V_{CESAT1}$ . The charging current flows from the input through D1, C1 and Q1 to ground. After Q1 is switched off, the node SW goes above  $V_O$  by the rectifier drop  $V_{CESAT2}$ . D1 becomes back-biased and the CAP voltage is pushed up to  $V_O + V_{CESAT2} + V_{IN} - V_{D1(ON)} - V_{CESAT1}$ . C1 supplies the base drive to Q2. The consumed charge is replenished during the Q1 on interval.

## OPERATION

In boost operation, X5 drives the rectifier Q2 into saturation. The voltage across the rectifier is  $V_{CESAT}$ . As the inductor current decreases, Q2's base drive also decreases. X5 ceases supplying base current to Q2 when the inductor current falls to zero.

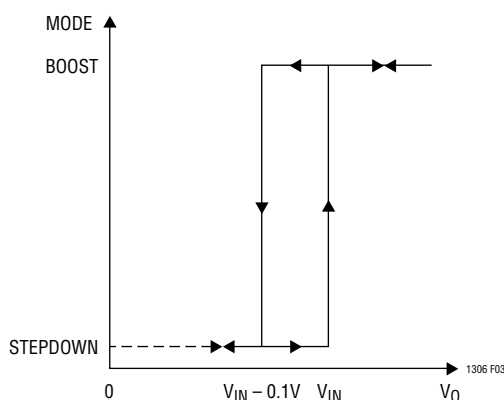
If  $V_{IN} > V_O$ , Q2 will no longer be driven into saturation. Instead the voltage across Q2 is allowed to increase so that the inductor voltage reverses polarity as Q1 switches. Since the inductor voltage is bipolar, volt-second balance can be maintained regardless of the input voltage. The LT1306 is therefore capable of operating as a step-down regulator with the basic boost topology. Input start-up current is also well controlled since the inductor current cannot increase during Q1's off-time with negative inductor voltage.

The rectifier voltage drop depends on both the input and the output voltages. Efficiency in the step-down mode is less than that of a linear regulator. For sustained step-down operation, the maximum output current will be limited by the package thermal characteristics.

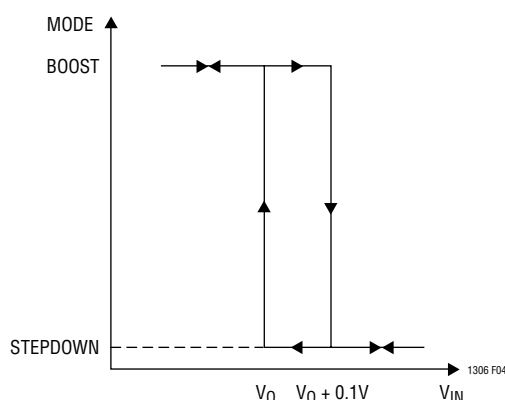
A hysteretic comparator in driver X5 controls the mode of operation. DC transfer characteristics of the comparator are shown in Figure 3 and Figure 4.

A logic low at the S/S pin (Pin 8) initiates shutdown. First, all circuit blocks in the LT1306 are switched off. The synchronous rectifier Q2 and its driver are kept on to allow stored inductive energy to flow to the output. As  $V_O$  drops below  $V_{IN}$ , the voltage across the rectifier Q2 increases so that the inductor voltage reverses. Inductor current continues to fall to zero. Driver X5 then turns off and the rectifier, Q2, becomes an open circuit. The LT1306 dissipates only 9 $\mu$ A in shutdown.

The LT1306 is guaranteed to start with a minimum  $V_{IN}$  of 1.8V. Comparator A5 senses the input voltage and generates an undervoltage lockout (UVLO) signal if  $V_{IN}$  falls below this minimum. In UVLO,  $V_C$  is pulled low and Q1 stops switching. The LT1306 draws 160 $\mu$ A from the input.



**Figure 3. DC Transfer Characteristics of the Mode Control Comparator Plotted with  $V_O$  as an Independent Variable.  $V_{IN}$  is Considered Fixed.**



**Figure 4. DC Transfer Characteristics of the Mode Control Comparator Plotted with  $V_{IN}$  as an Independent Variable.  $V_O$  is Considered Fixed.**



## APPLICATIONS INFORMATION

### Output Voltage Setting

The output voltage of the LT1306 is set with a resistive divider, R1 and R2 (Figure 1 and Figure 5), from the output to ground. The divider tap is tied to the FB pin. Current through R2 should be significantly higher than the FB pin input bias current ( $\leq 25\text{nA}$ ). With  $R2 = 249\text{k}$ , the input bias current of the error amplifier is 0.5% of the current in R1.

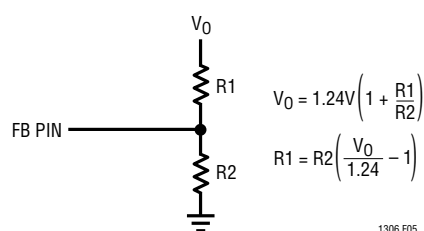


Figure 5. Feedback Resistive Divider

### Synchronization and Shutdown

The S/S pin (Pin 8) can be used to synchronize the oscillator or disconnect the load from the input. The S/S pin is tied to the input ( $V_{IN} > 1.8\text{V}$ ) for normal operation. The oscillator in the LT1306 can be externally synchronized by driving the S/S pin with a pulse train (See the graph “Maximum Allowable Rise Time of Synchronizing Pulse” in the Typical Performance Characteristics). The synchronization is positive edge triggered. The recommended frequency of the external clock ranges from 425kHz to 500kHz. If synchronization results in switching jitter, reducing the rising edge  $dv/dt$  of the external clock pulse usually cures the problem.

Shutdown will be activated if the S/S pin voltage stays below the shutdown threshold (0.45V) for more than 50 $\mu\text{s}$ . This shutdown delay is reset whenever the S/S pin goes above the shutdown threshold.

### Inductor

The value of the energy storage inductor L1 (Figure 1) is usually selected so that the peak-to-peak ripple current is less than 40% of the average inductor current. For 1- or 2-cell alkaline or single Li-Ion to 5V applications, 10 $\mu\text{H}$  to 20 $\mu\text{H}$  is recommended for the LT1306 running at 300kHz. A 5 $\mu\text{H}$  to 10 $\mu\text{H}$  inductor can be used if the LT1306 is externally synchronized at 500kHz.

The inductor should be able to handle the full load peak inductor current without saturation. The peak inductor current can be as high as 2A. This places a lower limit on the core size of the inductor. Powder iron cores have unacceptable core losses and are not suitable for high efficiency applications. Most ferrite core materials have manageable core losses and are recommended. Inductor DC winding resistance (DCR) also needs to be considered for efficiency. Usually there are trade-offs between core loss, DCR, saturation current, cost and size.

For EMI sensitive applications, one may want to use magnetically shielded or toroidal inductors to contain field radiation. Table 1 lists a number of inductors suitable for LT1306 applications.

Table 1. Inductors Suitable for Use with the LT1306

VENDOR	PART NO.	VALUE ( $\mu\text{H}$ )	MAX DCR ( $\Omega$ )	CORE TYPE	HEIGHT (mm)
BH Electronics	511-0033	5.0	0.023	Toroid	4.8
Coilcraft	DO3308-103	10	0.09	Open	3.0
	DO3316-472	4.7	0.018	Open	5.2
	DO3316-103	10	0.029	Open	5.2
	DO3316-153	15	0.046	Open	5.2
Coiltronics	CTX5-2	5	0.021	Toroid	6.0
	CTX10-2	10	0.032	Toroid	6.0
Murata	LQN6C4R7	4.7	0.034	Open	5.0
Sumida	CDRH73-100	10	0.072	Magnetic Shielding	3.4
	CD43-4R7	4.7	0.109	Open	3.2

### Capacitors

The output filter capacitor is usually chosen based on its equivalent series resistance (ESR) and the acceptable change in output voltage as a result of load transients. The output voltage ripple at the switching frequency can be estimated by considering the peak inductor current and the capacitor ESR.

$$I_{\text{PEAK}} \approx I_{\text{IN}} \approx \frac{(I_0)(V_0)}{V_{\text{IN}}}$$

$$\text{output ripple} \approx (\text{ESR})(I_{\text{PEAK}}) = \frac{(\text{ESR})(I_0)(V_0)}{V_{\text{IN}}}$$



## APPLICATIONS INFORMATION

Since a boost converter produces high output current ripple, one also needs to consider the maximum ripple current rating of the output capacitor. Capacitor reliability will be affected if the ripple current exceeds the maximum allowable ratings. This maximum rating is usually specified as the RMS ripple current. In the LT1306 the RMS output capacitor ripple current is:

$$I_O \sqrt{\frac{V_O - V_{IN}}{V_{IN}}}$$

For 2-cell to 5V applications, 220 $\mu$ F low ESR solid tantalum capacitors (AVX TPS series or Sprague 593D series) work well. To reduce output voltage ripple due to heavy load transients or Burst Mode operation, higher capacitance may be used. For through-hole applications, Sanyo OS-CON capacitors are also good choices.

In a boost regulator, the input capacitor ripple current is much lower. Maximum ripple current rating and input voltage ripples are not usually of concern. A 22 $\mu$ F tantalum capacitor soldered near the input pin is generally an adequate bypass.

### Bootstrap Supply

Diode D1 and capacitor C1 generate a pulsating supply voltage,  $V_{CAP}$ , which is higher than the output. The rectifier drive circuit runs off this supply. During rectifier on-time, the rectifier base current drains C1. Q2 base current and the maximum allowable  $V_{CAP}$  ripple voltage determine the size of C1. A 1 $\mu$ F capacitor is sufficient to keep  $V_{CAP}$  ripple below 0.3V. For a 2-cell input ( $V_{IN} > 1.8V$ ) over an extended temperature range, a BAT54 Schottky diode may be used for D1. The use of a Schottky diode increases the bootstrap voltage and the operating headroom for the rectifier driver, X5. Diodes like a 1N4148 or 1N914 work well for 2-cell inputs over the 0°C to 70°C commercial temperature range.

The charge drawn from C1 during the rectifier on-time has to be replenished during the switch on-interval. As duty cycle decreases, the amplitude of the C1 charging current can increase dramatically especially when delivering high power to the load. This charging current flows through the

switch and can cause the current limit comparator to trip erratically. For boost applications where  $V_{IN}$  is a few tenths of a volt below  $V_O$ , a 1 $\mu$ F or 2.2 $\mu$ F tantalum capacitor (such as AVX TAJ series) can be used for C1. The ESR of the tantalum capacitor limits the charging current. A low value resistor (2 $\Omega$  to 5 $\Omega$ ) can also be added in series with C1 for further limiting the charging current although this tends to lower the converter efficiency slightly.

### Frequency Compensation

Current mode switching regulators have two feedback loops. The inner current feedback loop controls the inductor current in response to the outer loop. The outer or overall feedback loop tightly regulates the output voltage. The high frequency gain asymptote of the inner current loop rolls off at -20dB/decade and crosses the unity gain axis at a frequency  $\omega_c$  between 1/6 to 2/3 of the switching frequency. The current loop is stable and is wideband compared to the overall voltage feedback loop. The low frequency current loop gain is not high (usually between unity and 10) but it increases the low frequency impedance of the inductor as seen by the output filter capacitor. (In a boost regulator, the inductor is connected to the output during the switch off-time.) Current mode control introduces an effective series resistance ( $\gg DCR$ ) to the inductor that damps the LC tank response. The complex high-Q poles of the LC filter are now separated, resulting in a dominant pole determined by the filter capacitance and the load resistance and a second high frequency pole.

For a boost regulator the control to output transfer function can be shown to have a dominant pole at the load corner frequency

$$\omega_P = \frac{1}{\left(\frac{R_L}{2}\right)(C_O)}$$

and a moving right-half plane (RHP) zero with a minimum value of

$$\omega_Z = \frac{R_L(1-D_{MAX})^2}{L}$$

## APPLICATIONS INFORMATION

where

$$R_L = \text{Maximum Load} = \frac{\text{Output Voltage}}{\text{Maximum DC Load Current}}$$

$$D_{MAX} = \text{Maximum Converter Duty Cycle}$$

$$= \frac{V_O - V_{IN(MIN)} + 0.5}{V_O + 0.1}$$

There is also a second pole at the current loop crossover frequency  $\omega_C$  (Figure 6).  $\omega_Z$  is much lower in frequency than  $\omega_C$ . The loop is compensated by adjusting the midband gain with resistor R3 (Figure 7) so that the overall loop gain crosses 0dB before the minimum frequency RHP zero (i.e., corresponding to the highest duty ratio). The value of R3 can be estimated with the formula:

$$R3 = \frac{390V_O(1 - D_{MAX})C_O R_L}{L}$$

Due to the low transconductance of the error amplifier, the gain setting resistor R3 is AC-coupled with capacitor  $C_Z$ . This prevents R3 from inducing an offset to the input of the error amplifier. It also creates a pole at DC and a low frequency zero.

The amplitude response of the error amplifier with the compensation network shown is:

$$\frac{\hat{V}_C}{\hat{V}_O} = g_m \left( \frac{R2}{R1 + R2} \right) \frac{1 + (S \cdot R3 \cdot C_Z)}{S \cdot C_Z [1 + (S \cdot R3 \cdot C_P)]}$$

$$C_Z \gg C_P$$

The low frequency zero  $1/R3C_Z$  of the compensation network is placed at  $\omega_P/2$ .

$$C_Z = \frac{2}{R3\omega_P}$$

The capacitor  $C_P$  ensures adequate gain margin beyond the RHP zero. The high frequency pole  $1/R3C_P$  of the amplifier frequency response is placed beyond  $\omega_Z$ .

$$C_P = \frac{1}{3\omega_Z R3}$$

Higher output filter capacitance rolls off the gain response from a lower corner frequency so higher midband gain is required in the compensation network to make the overall loop gain cross 0dB just below  $\omega_Z$ .

### Layout Consideration

To minimize EMI and high frequency resonances, it is essential to keep the SW and the CAP trace leads as short as possible. The input and the output bypass capacitors  $C_{IN}$  and  $C_{OUT}$  should be placed close to the IC package and soldered to the ground plane. A ground plane under the switching regulator is highly recommended. Figure 8 shows a suggested component placement and PC board layout.

## APPLICATIONS INFORMATION

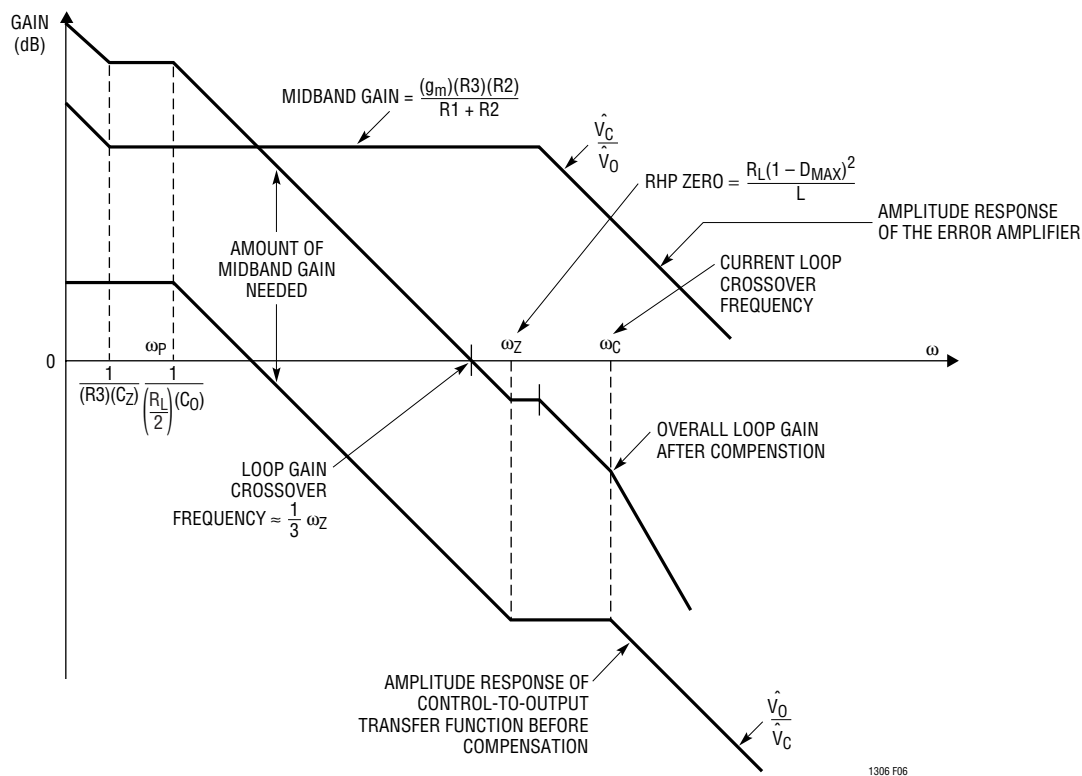


Figure 6. Gain Asymptotes of the Control-to-Output  $\left(\frac{\hat{V}_O}{\hat{V}_C}\right)$  and Error Amplifier  $\left(\frac{\hat{V}_C}{\hat{V}_O}\right)$  Transfer Function

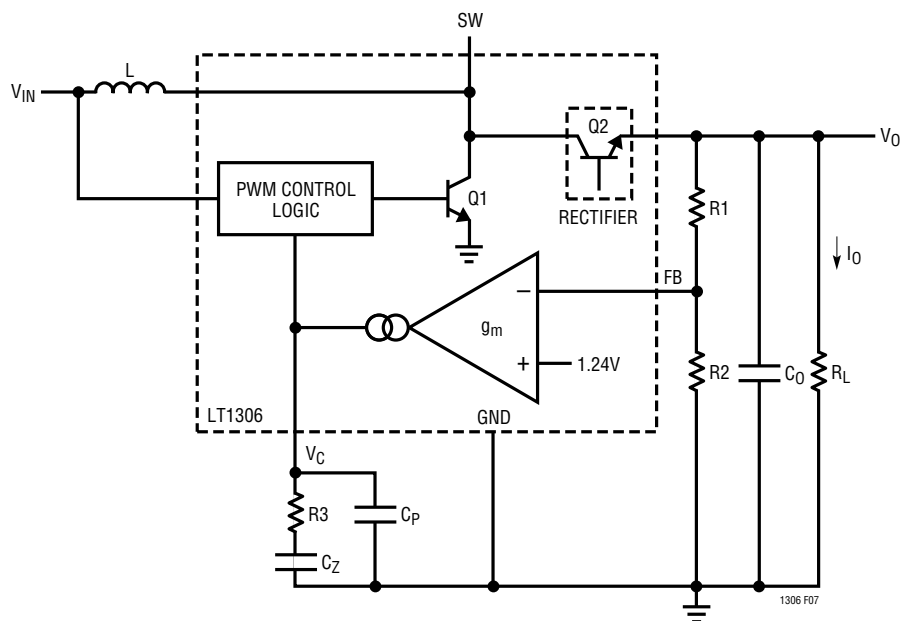
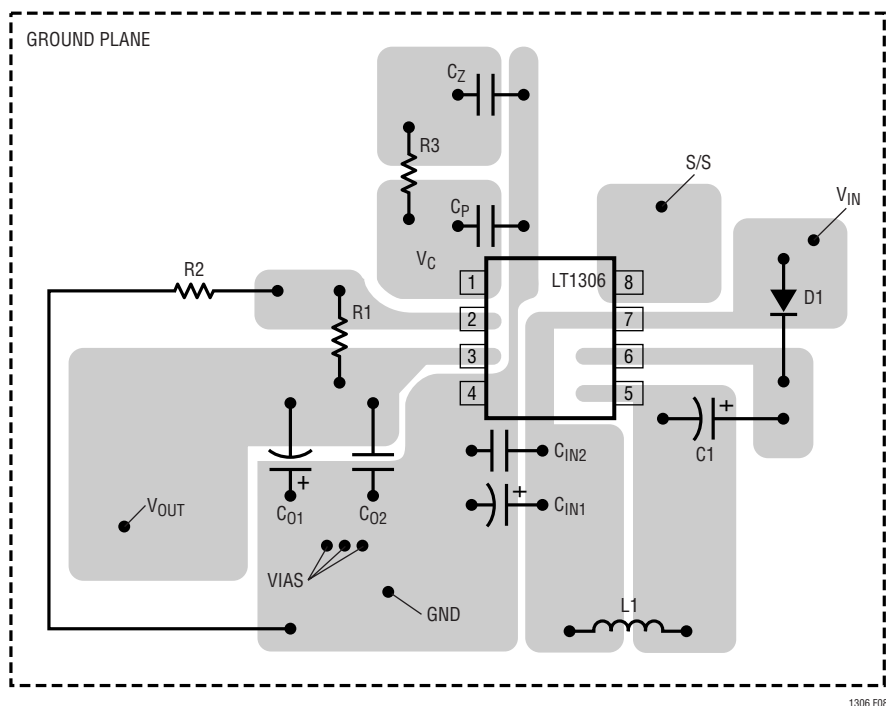


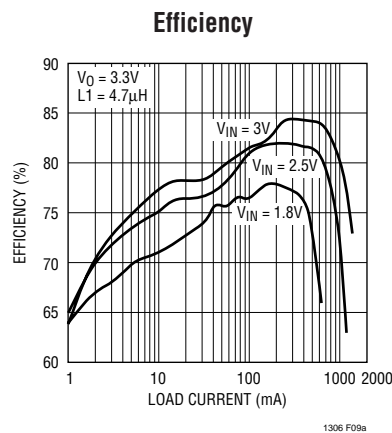
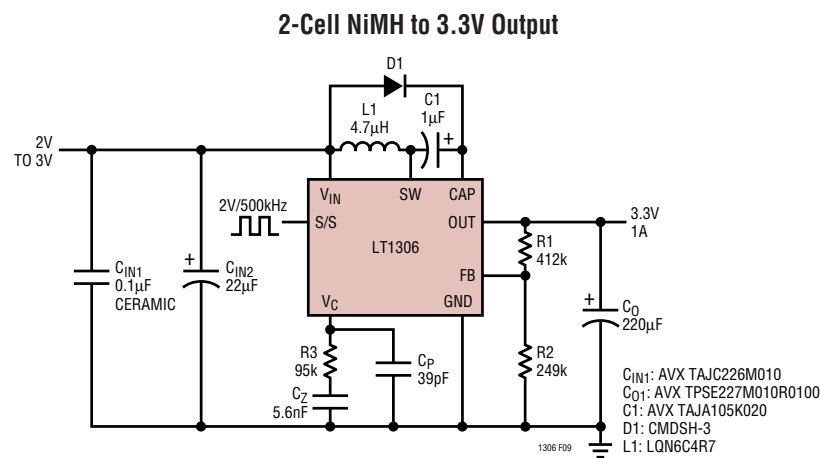
Figure 7. Current Mode Boost Converter Overall-Loop Compensation

## APPLICATIONS INFORMATION



**Figure 8. Recommended Component Placement for LT1306.**  
 Notice That the Input and the Output Capacitors Are Grounded at the Same Point. A Ground Plane Under the DC/DC Converter Is Highly Recommended. Use Multiple Vias to Tie Pin 4 Copper to the Ground Plane

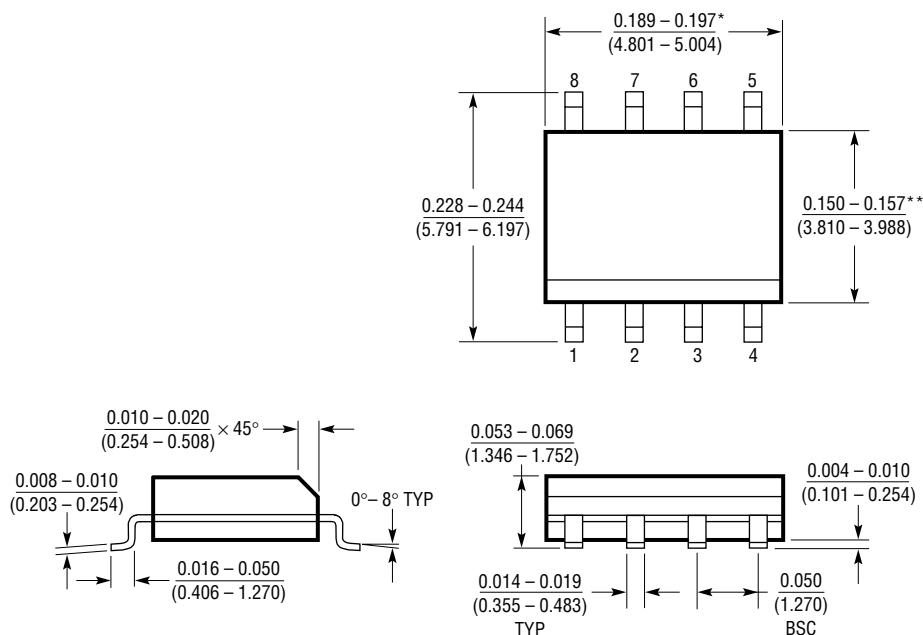
TYPICAL APPLICATIONS



# PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

## S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

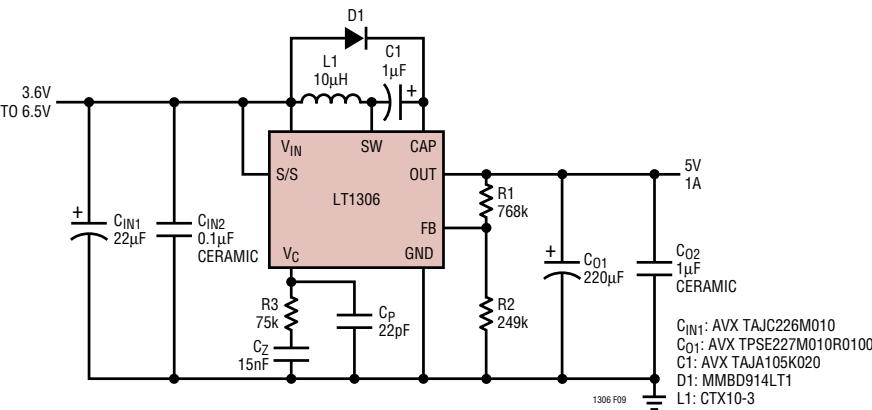
\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298

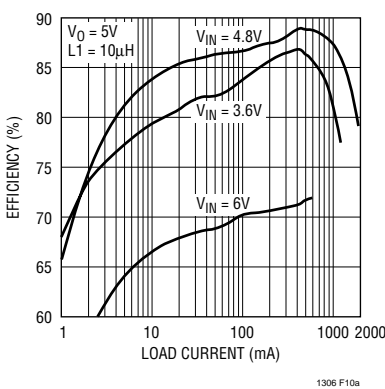


TYPICAL APPLICATIONS

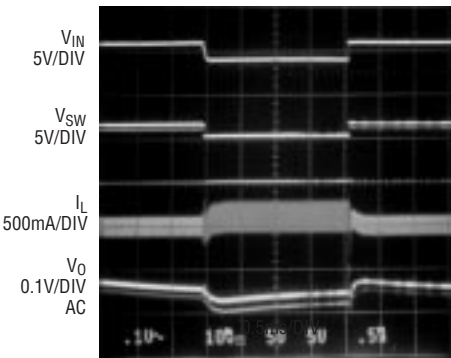
4-Cell NiMH to 5V Output



Efficiency



Transient Response with Step Input (4V to 6V)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1302	High Output Current Micropower DC/DC Converter	5V/600mA from 2V, 2A Internal Switch, 200µA I <sub>Q</sub>
LT1304	2-Cell Micropower DC/DC Converter	5V/200mA, Low-Battery Detector Active in Shutdown
LT1307/LT1307B	Single Cell, Micropower, 600kHz PWM DC/DC Converters	3.3V at 75mA from One Cell, MSOP Package
LT1308A/LT1308B	High Output Current Micropower DC/DC Converter	5V at 1A from Single Li-Ion Cell
LT1316	Burst Mode Operation DC/DC with Programmable Current Limit	1.5V Minimum, Precise Control of Peak Current Limit
LT1317/LT1317B	Micropower, 600kHz PWM DC/DC Converters	100µA I <sub>Q</sub> , Operate with V <sub>IN</sub> as Low as 1.5V
LT1610	Single-Cell Micropower DC/DC Converter	3V at 30mA from 1V, 1.7MHz Fixed Frequency
LT1613	1.4MHz Switching Regulator in 5-Lead SOT-23	5V at 200mA from 4.4V Input, Tiny SOT-23 package
LT1615	Micropower Step-Up DC/DC in 5-Lead SOT-23	20µA I <sub>Q</sub> , 36V/350mA Internal Switch, V <sub>IN</sub> as Low as 1.2V
LTC1624	High Efficiency N-channel Switching Regulator Controller	V <sub>OUT</sub> = 1.19V to 30V in Stepdown; V <sub>IN</sub> = 3.5V to 36V SO-8 Package
LT1949	600kHz, 1A Switch PWM DC/DC Converter	1.1A, 0.5Ω/30V Internal Switch, V <sub>IN</sub> as Low as 1.5V