ISSI

PIN CONFIGURATION
32-Pin SOJ

A0	1		32	A16	
A1	2		31	A15	
A2	3		30	A14	
A3	4		29	A13	
$\overline{CE}$	5		28	$\overline{OE}$	
I/O0	6		27	I/O7	
I/O1	7		26	I/O6	
VDD	8		25	GND	
GND	9		24	VDD	
I/O2	10		23	I/O5	
I/O3	11		22	I/O4	
$\overline{WE}$	12		21	A12	
A4	13		20	A11	
A5	14		19	A10	
A6	15		18	A9	
A7	16		17	A8	

PIN CONFIGURATION
32-Pin TSOP (Type II) (T)
32-Pin sTSOP (Type I) (H)

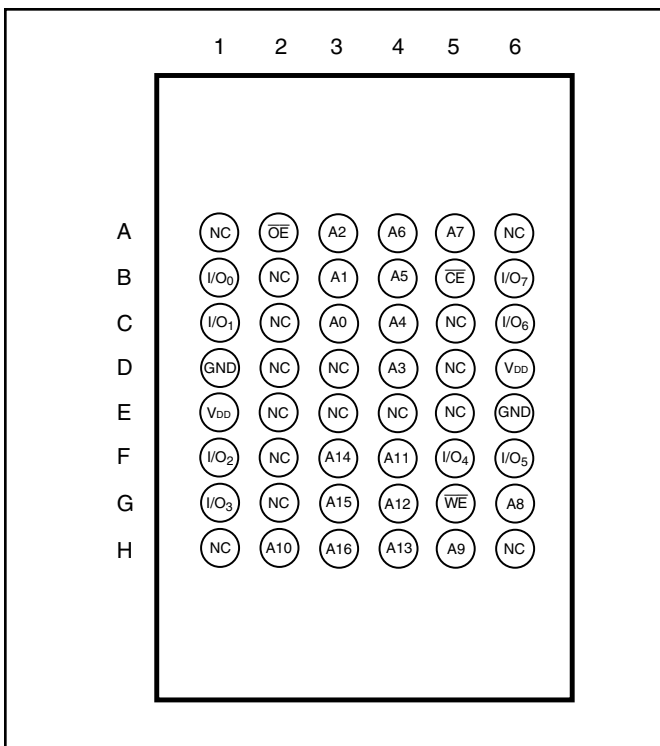|				
A0	1	32	A16	
A1	2	31	A15	
A2	3	30	A14	
A3	4	29	A13	
$\overline{CE}$	5	28	$\overline{OE}$	
I/O0	6	27	I/O7	
I/O1	7	26	I/O6	
VDD	8	25	GND	
GND	9	24	VDD	
I/O2	10	23	I/O5	
I/O3	11	22	I/O4	
$\overline{WE}$	12	21	A12	
A4	13	20	A11	
A5	14	19	A10	
A6	15	18	A9	
A7	16	17	A8	
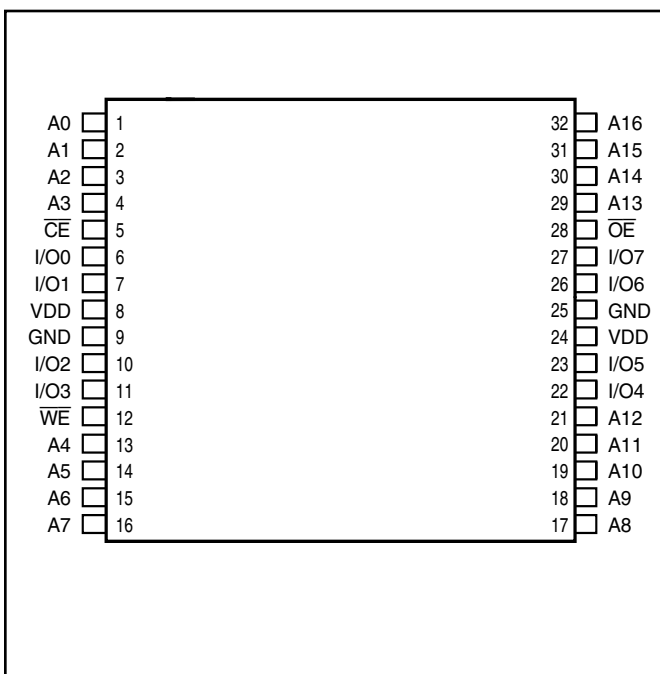
PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground

PIN CONFIGURATION
48-mini BGA (B) (6 mm x 8 mm)

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A2	A6	A7	NC
B	I/O0	NC	A1	A5	$\overline{CE}$	I/O7
C	I/O1	NC	A0	A4	NC	I/O6
D	GND	NC	NC	A3	NC	VDD
E	VDD	NC	NC	NC	NC	GND
F	I/O2	NC	A14	A11	I/O4	I/O5
G	I/O3	NC	A15	A12	$\overline{WE}$	A8
H	NC	A10	A16	A13	A9	NC

Integrated Silicon Solution, Inc. — www.issi.com
Rev. B1
03/23/2018

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{DD}+0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.5	W
V_{DD}	V_{DD} Related to GND	-0.2 to +3.9	V

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V_{DD} - 0.3V	0.4V to V_{DD} - 0.3V	0.4V to V_{DD} - 0.3V
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD}/2$	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 (Ω)	1909	317	13500
R2 (Ω)	1105	351	10800
V_{TM} (V)	3.0V	3.3V	1.8V

AC TEST LOADS
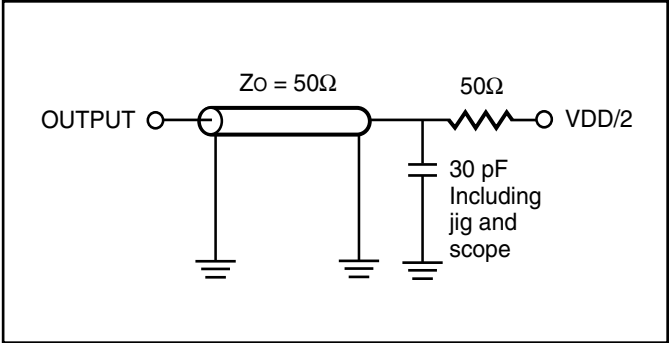
Figure 1.
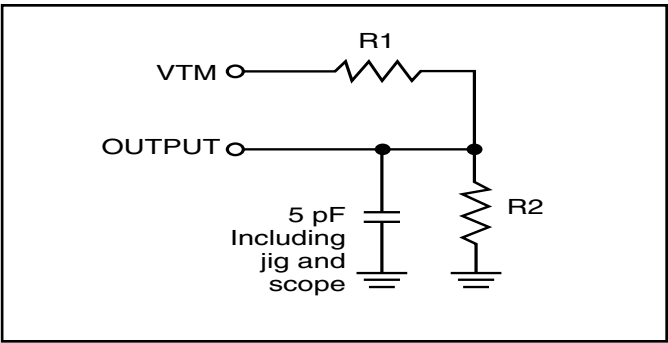
Figure 2.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

HIGH SPEED (IS63WV1288DALL/DBLL)

OPERATING RANGE (V_{DD}) (IS63WV1288DALL)

Range	Ambient Temperature	V_{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	−40°C to +85°C	1.65V-2.2V	20ns
Automotive	−40°C to +125°C	1.65V-2.2V	20ns

OPERATING RANGE (V_{DD}) (IS63WV1288DBLL)[1]

Range	Ambient Temperature	V_{DD} (8 ns)[1]	V_{DD} (10 ns)[1]
Commercial	0°C to +70°C	3.3V $\pm$ 5%	2.4V-3.6V
Industrial	−40°C to +85°C	3.3V $\pm$ 5%	2.4V-3.6V

Note:
1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V $\pm$ 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV1288DBLL)[2]

Range	Ambient Temperature	V_{DD} (8 ns)[2]	V_{DD} (10 ns)[2]
Automotive	−40°C to +125°C	3.3V $\pm$ 5%	2.4V-3.6V

Note:
2. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V $\pm$ 5%, the device meets 8ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-20 Min.	-20 Max.	Unit
I_{CC}	V_{DD} Dynamic Operating	V_{DD} = Max.,	Com.	—	65	—	50	—	45	—	40	mA
	Supply Current	I_{OUT} = 0 mA, f = f_{MAX}	Ind.	—	70	—	55	—	50	—	45	
		$\overline{CE}$ = V_{IL}	Auto.[3]	—	—	—	65	—	55	—	50	
		$V_{IN} \geq V_{DD} - 0.3V$, or	typ.[2]		45			45				
		$V_{IN} \leq 0.4V$										
I_{SB2}	CMOS Standby	V_{DD} = Max.,	Com.	—	40	—	40	—	40	—	40	µA
	Current (CMOS Inputs)	$\overline{CE} \geq V_{DD} - 0.2V$,	Ind.	—	55	—	55	—	55	—	55	
		$V_{IN} \geq V_{DD} - 0.2V$, or	Auto.	—	—	—	90	—	90	—	90	
		$V_{IN} \leq 0.2V$, f = 0	typ.[2]		4			4				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

3. For Automotive grade at 15ns, typ. Icc = 38mA, not 100% tested.

LOW POWER (IS63WV1288DALS/DBLS)

OPERATING RANGE (V_{DD}) (IS63WV1288DALS)

Range	Ambient Temperature	V_{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	−40°C to +85°C	1.65V-2.2V	45ns
Automotive	−40°C to +125°C	1.65V-2.2V	55ns

OPERATING RANGE (V_{DD}) (IS63WV1288DBLS)

Range	Ambient Temperature	V_{DD} (35 ns)
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	−40°C to +85°C	2.4V-3.6V

OPERATING RANGE (V_{DD}) (IS64WV1288DBLS)

Range	Ambient Temperature	V_{DD} (35 ns)
Automotive	−40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 Min.	-25 Max.	-35 Min.	-35 Max.	-45 Min.	-45 Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} $\overline{CE}$ = V_{IL} $V_{IN} \geq V_{DD}$ − 0.3V, or $V_{IN} \leq$ 0.4V	Com.	—	15	—	15	—	12	mA
			Ind.	—	20	—	20	—	18	
			Auto.	—	30	—	30	—	25	
			typ.[2]	18						
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD}$ − 0.2V, $V_{IN} \geq V_{DD}$ − 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	40	—	40	—	40	μA
			Ind.	—	50	—	50	—	50	
			Auto.	—	75	—	75	—	75	
			typ.[2]	4						

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	—	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	4	0	5	0	6	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	4	0	5	0	6	ns
t_{PU}	$\overline{CE}$ to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	$\overline{CE}$ to Power Down Time	—	8	—	10	—	12	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V loading specified in Figure 1.
2. Tested with the loading specified in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

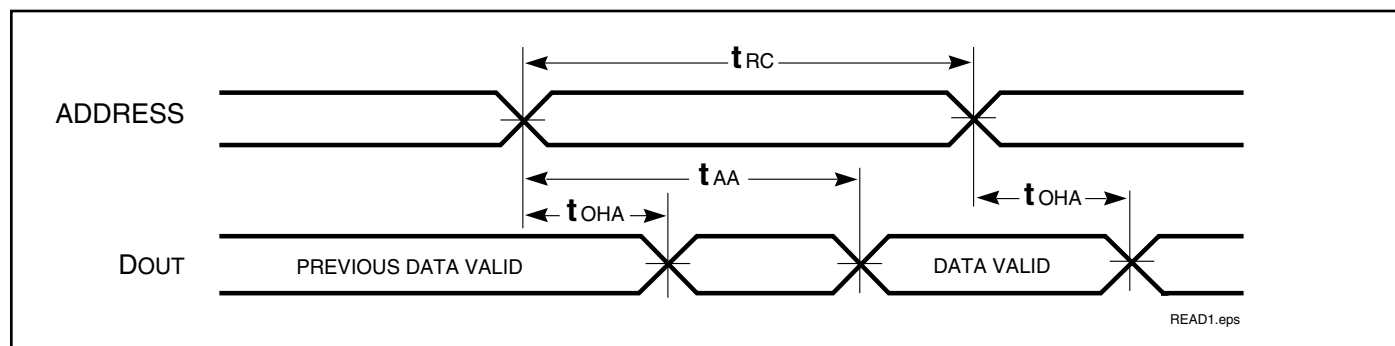## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

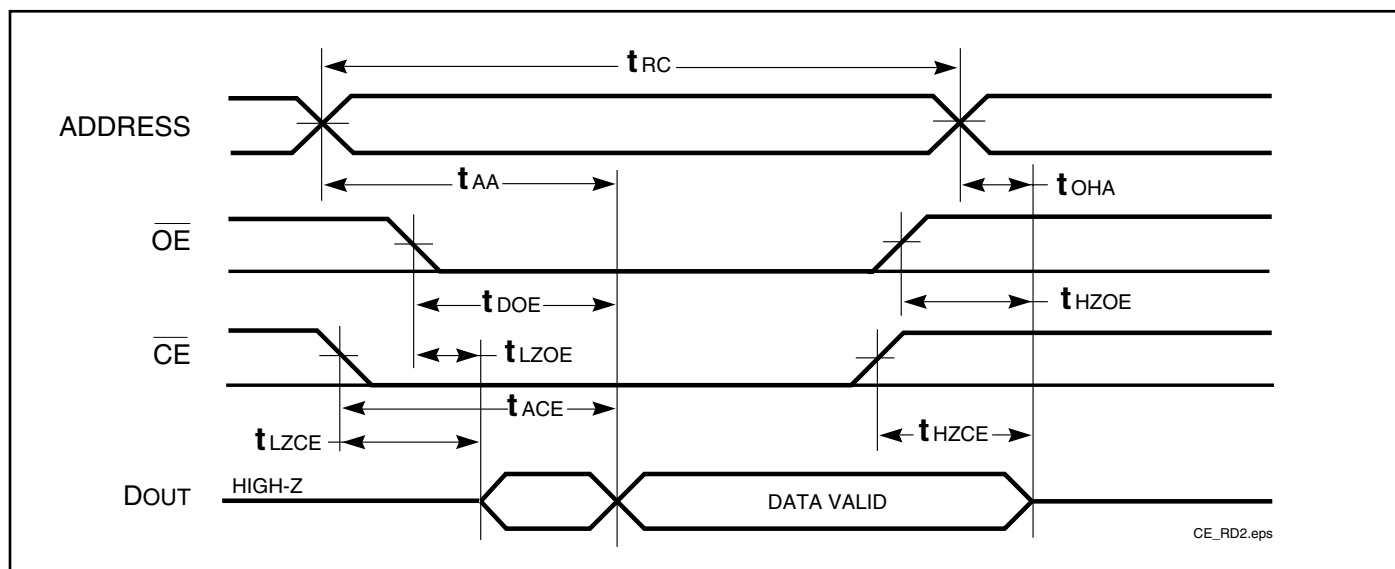| Symbol	Parameter	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	-35 ns Min.	-35 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{OHA}	Output Hold Time	2.5	—	6	—	8	—	10	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	—	25	—	35	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	—	12	—	15	—	20	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	8	0	8	0	10	0	15	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	8	0	8	0	10	0	15	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	10	—	10	—	10	—	ns

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[(1,2)]

ADDRESS

t_{RC}

t_{AA}

t_{OHA}

t_{OHA}

DOUT — PREVIOUS DATA VALID — DATA VALID

READ1.eps

READ CYCLE NO. 2[(1,3)]

ADDRESS

t_{RC}

t_{AA}

t_{OHA}

$\overline{OE}$

t_{DOE}

t_{HZOE}

$\overline{CE}$

t_{LZOE}

t_{ACE}

t_{HZCE}

t_{LZCE}

DOUT — HIGH-Z — DATA VALID

CE_RD2.eps

Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	7	—	8	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE_1}[1]	$\overline{WE}$ Pulse Width ($\overline{OE}$ High)	7	—	7	—	8	—	ns
t_{PWE_2}[2]	$\overline{WE}$ Pulse Width ($\overline{OE}$ Low)	8	—	10	—	12	—	ns
t_{SD}	Data Setup to Write End	5	—	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	4	—	5	—	6	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

## WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	-35 ns Min.	-35 ns Max.	-45ns Min.	-45ns Max.	Unit
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{SCE}	$\overline{CE}$ to Write End	12	—	18	—	25	—	35	—	ns
t_{AW}	Address Setup Time to Write End	12	—	15	—	25	—	35	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	12	—	18	—	30	—	35	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	17	—	20	—	30	—	35	—	ns
t_{SD}	Data Setup to Write End	9	—	12	—	15	—	20	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	9	—	12	—	20	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	3	—	5	—	5	—	5	—	ns

Notes:
1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
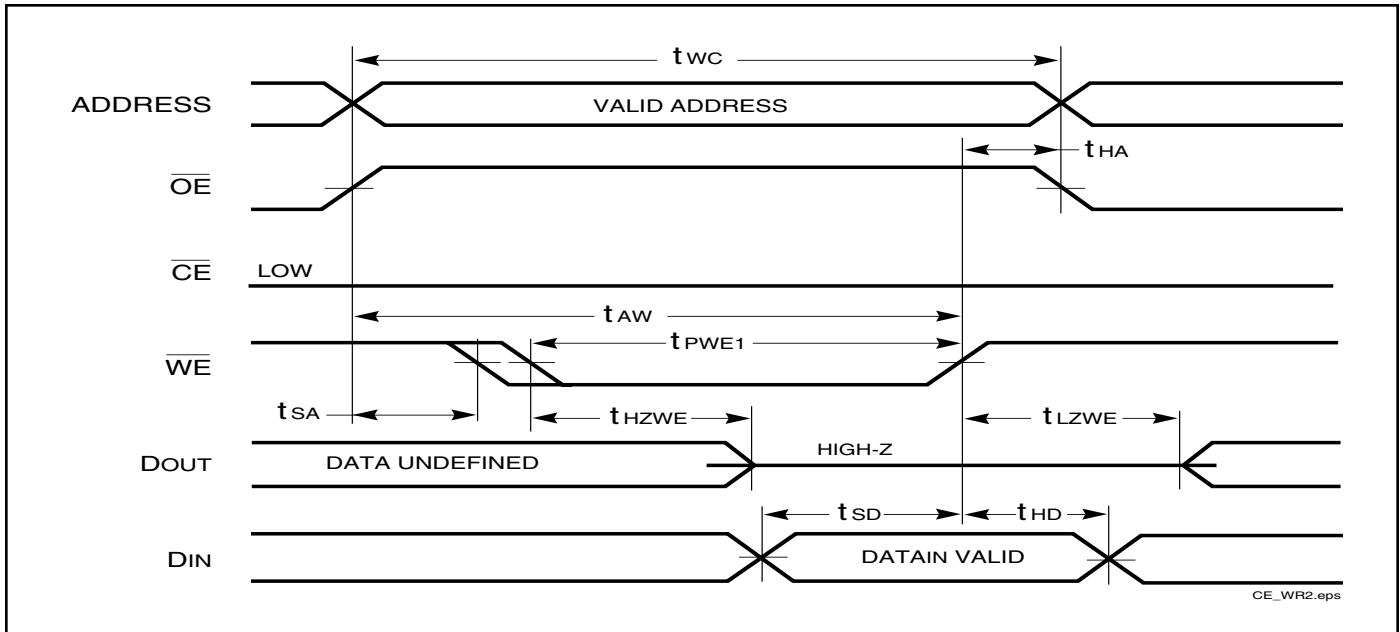
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)
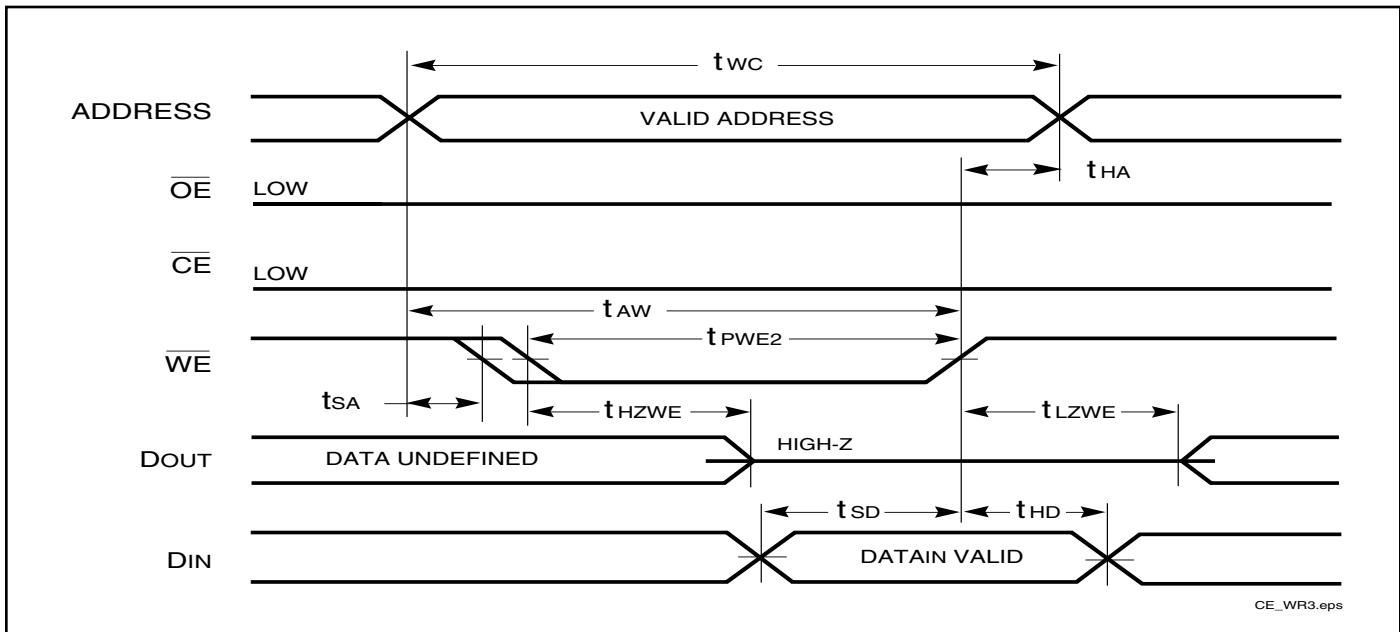

CE_WR1.eps
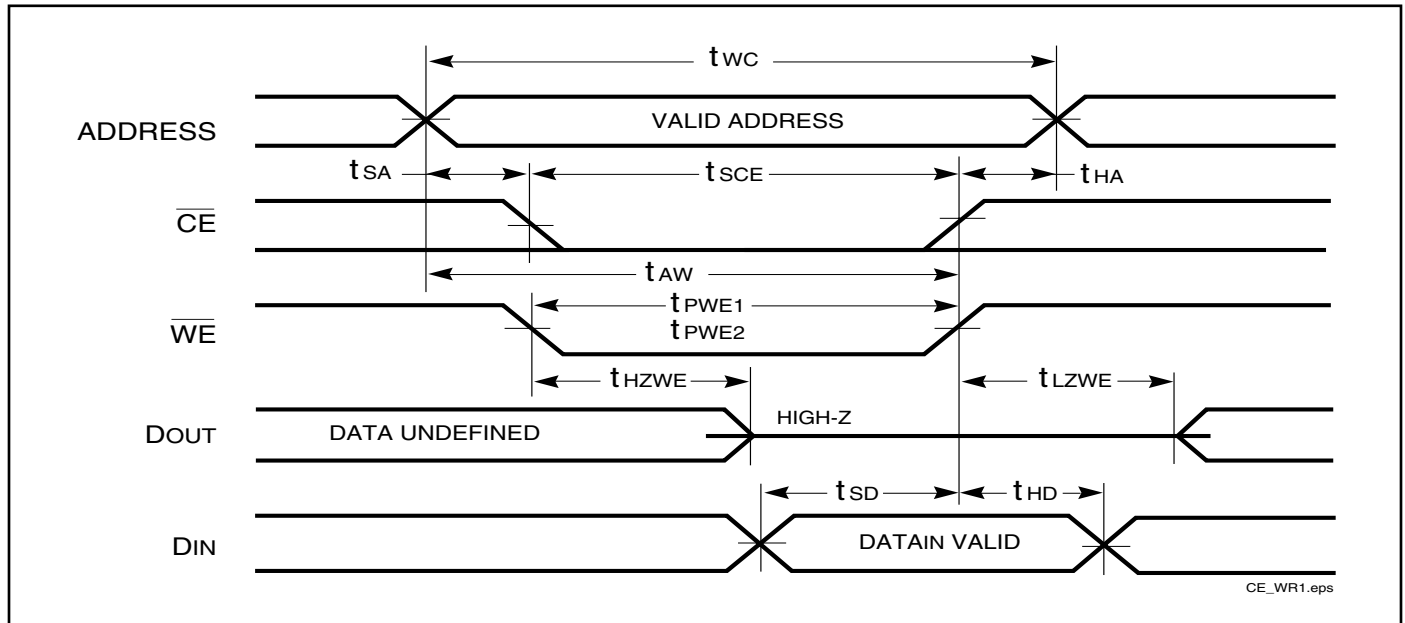
AC WAVEFORMS

WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)

ADDRESS — VALID ADDRESS
t_{WC}
t_{HA}

$\overline{OE}$

$\overline{CE}$ — LOW

$\overline{WE}$
t_{AW}
t_{PWE1}

t_{SA}
t_{HZWE}
t_{LZWE}

Dout — DATA UNDEFINED — HIGH-Z

t_{SD} t_{HD}

Din — DATAIN VALID

CE_WR2.eps

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

ADDRESS — VALID ADDRESS
t_{WC}
t_{HA}

$\overline{OE}$ — LOW

$\overline{CE}$ — LOW

$\overline{WE}$
t_{AW}
t_{PWE2}

t_{SA}
t_{HZWE}
t_{LZWE}

Dout — DATA UNDEFINED — HIGH-Z

t_{SD} t_{HD}

Din — DATAIN VALID

CE_WR3.eps

Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

HIGH SPEED (IS63/4WV1288DALL/DBLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

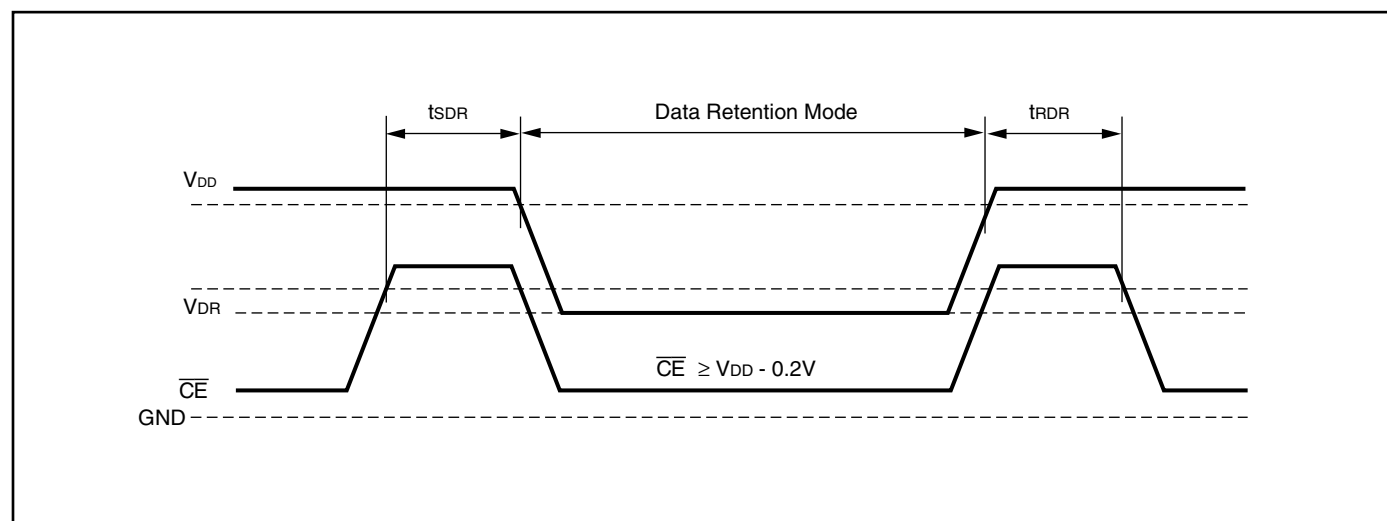| Symbol	Parameter	Test Condition	Options	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V$, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	55	
			Auto.			90	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25°C$ and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V$, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	55	
			Auto.	—	—	90	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 1.8V$, $T_A = 25°C$ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

LOW POWER (IS63/4WV1288DALS/DBLS)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V$, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	50	
			Auto.			75	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25°C$ and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V$, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	50	
			Auto.	—	—	75	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 1.8V$, $T_A = 25°C$ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

ORDERING INFORMATION
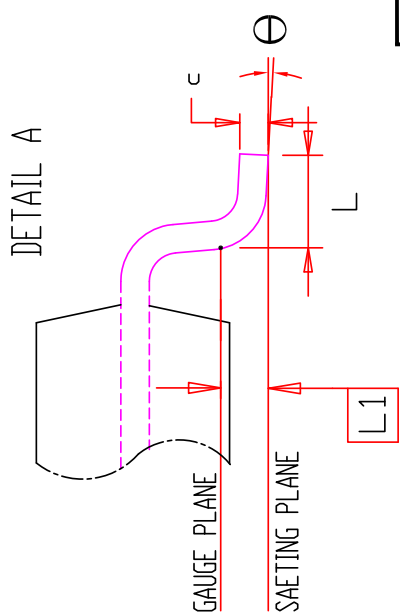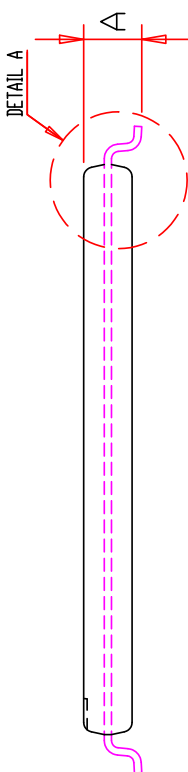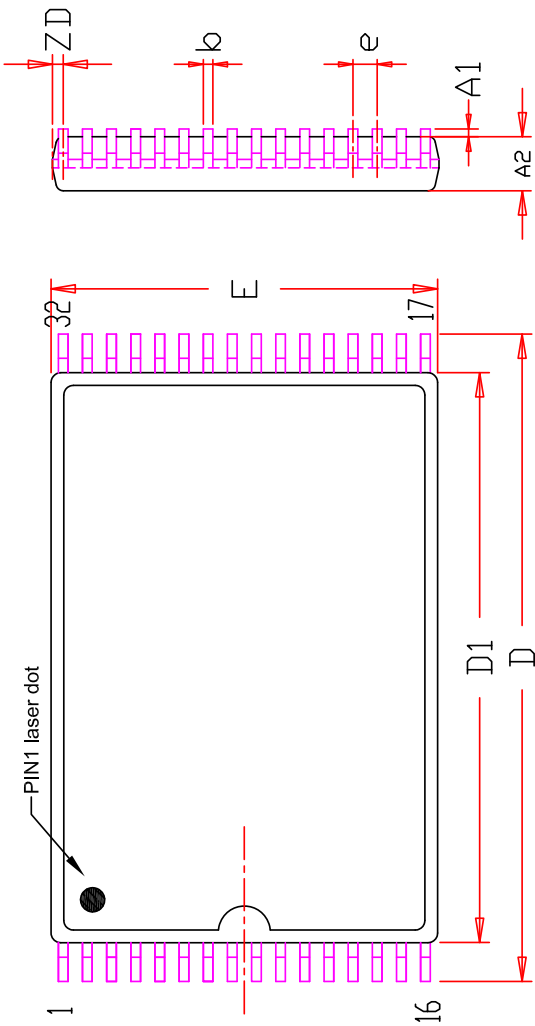
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS63WV1288DBLL-8TLI	32-pin TSOP (Type II), Lead-free
	IS63WV1288DBLL-8HLI	sTSOP (Type I) (8mm x13.4mm), Lead-free
	IS63WV1288DBLL-8JLI	32-pin SOJ (300-mil), Lead-free
10	IS63WV1288DBLL-10TLI	32-pin TSOP (Type II), Lead-free
	IS63WV1288DBLL-10HLI	sTSOP (Type I) (8mm x13.4mm), Lead-free
	IS63WV1288DBLL-10JLI	32-pin SOJ (300-mil), Lead-free
	IS63WV1288DBLL-10KLI	32-pin SOJ (400-mil), Lead-free

Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
10(8*)	IS64WV1288DBLL-10CTLA3	32-pin TSOP (Type II), Copper Lead frame, Lead-free
	IS64WV1288DBLL-10HLA3	sTSOP (Type I) (8mm x13.4mm), Lead-free

Note:
1. Speed = 8ns for V_{DD} = 3.3V + 5%. Speed = 10ns for V_{DD} = 2.4V-3.6V.

SYMBOL	DIMENSION IN MM MIN	NOM	MAX	DIMENSION IN INCH MIN	NOM	MAX
A	0.95	---	1.25	0.037	---	0.049
A1	0.05	---	0.15	0.002	---	0.008
A2	0.90	---	1.05	0.035	---	0.041
b	0.16	---	0.27	0.006	---	0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
θ	0	3°	5°	0	3°	5°
c	0.10		0.21	0.004		0.008

NOTE :

1. Controlling Dimension : mm
2. Dimension D1 and E do not include mold protrusion.
3. Dimension b does not include dambar protrusion/intrusion.
4. Reference Document : JEDEC MO-183
5. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

CASE 1

PIN1 laser dot

DETAIL A

GAUGE PLANE

SAETING PLANE

| TITLE | 32L 8x13.4mm TSOP-1 Package Outline | REV. F | DATE 06/21/2017 |

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	—	3.76	0.128	—	0.148
A1	2.08	—	—	0.082	—	—
A3	0.635	—	—	0.025	—	—
b	0.38	—	0.51	0.015	—	0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BSC			0.370 BSC		
e	1.27 BSC			0.050 BSC		
ZD	0.95 REF			0.037 REF		
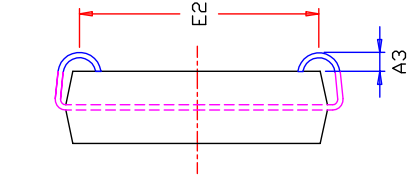
NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
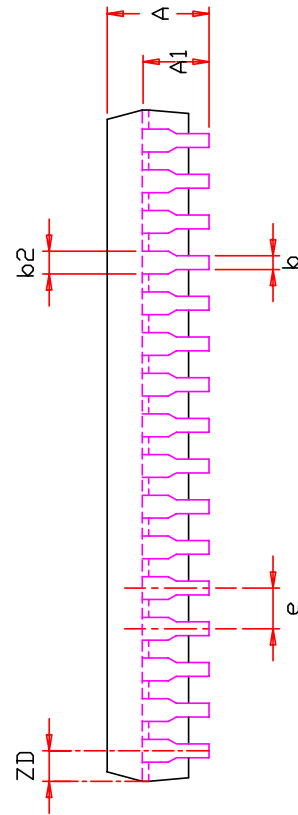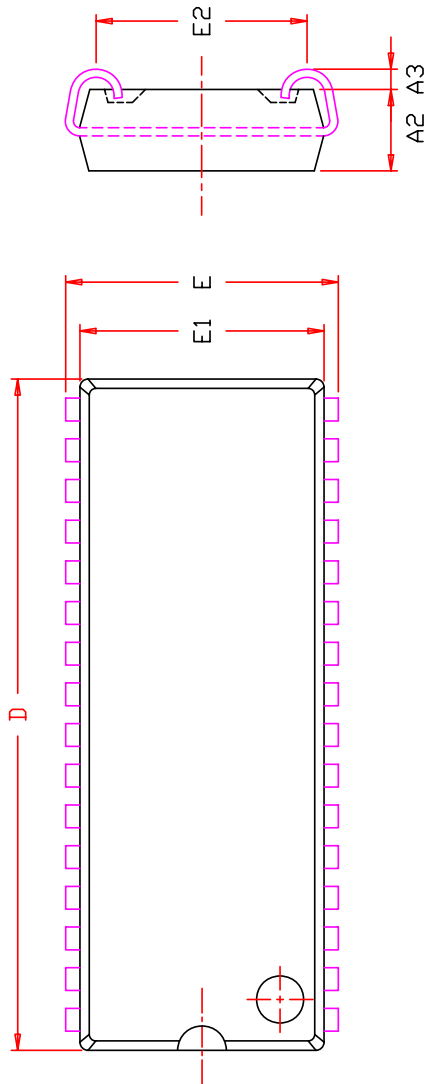5. Reference document : JEDEC SPEC MS-027.

SEATING PLANE
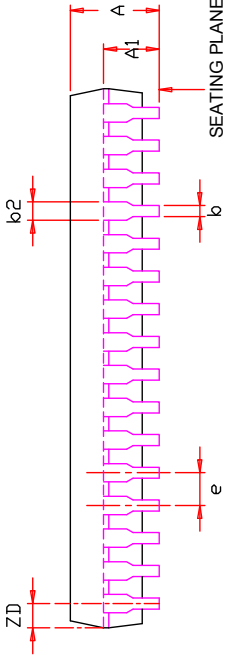
TITLE	32L 400mil SOJ Package Outline	REV.	E	DATE	12/19/2007

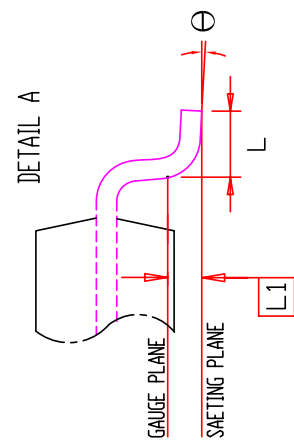| SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.05		3.76	0.120		0.148
A1	2.08		2.41	0.082		0.095
A2	2.41	2.54	2.67	0.095	0.100	0.105
A3	0.64		1.09	0.025		0.043
b	0.41		0.51	0.016		0.020
b2	0.66		0.81	0.026		0.032
D	20.82		21.09	0.820		0.830
E	8.38	8.51	8.64	0.330	0.335	0.340
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.48		6.99	0.255		0.275
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	**32L 300mil SOJ** Package Outline	REV.	**C**	DATE	08/14/2009

Integrated Silicon Solution, Inc. — www.issi.com
Rev. B1
03/23/2018

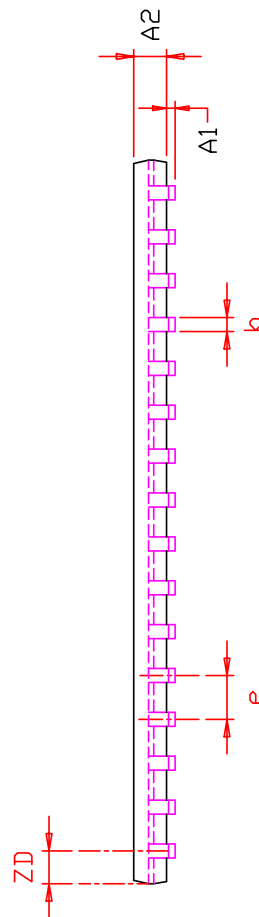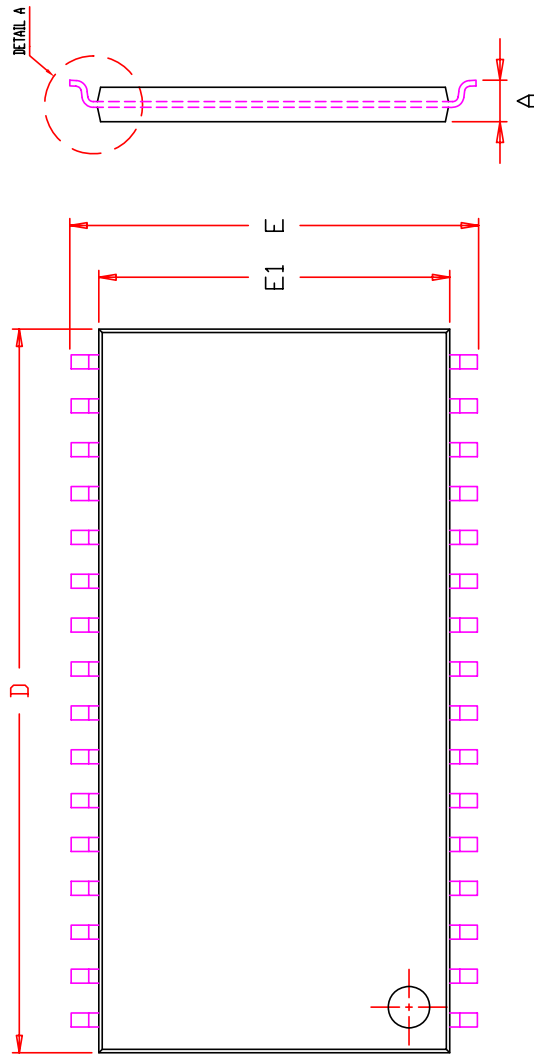| SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.52	0.012		0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	1.27 BSC.			0.050 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.95 REF.			0.037 REF.		
Θ	0		8°	0		8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	32L 400mil TSOP-2 Package Outline	REV. E	DATE 06/23/2009

DETAIL A

A

A2

A1

b

e

E

E1

D

ZD

DETAIL A

GAUGE PLANE

SAETING PLANE

L

L1

Θ

SYMBOL	DIMENSION IN MM MIN.	NOM.	MAX.	DIMENSION IN INCH MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
Øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC.			0.030 BSC.		
ZD	1.375 REF.			0.054 REF.		
ZE	1.125 REF.			0.044 REF.		

NOTE :
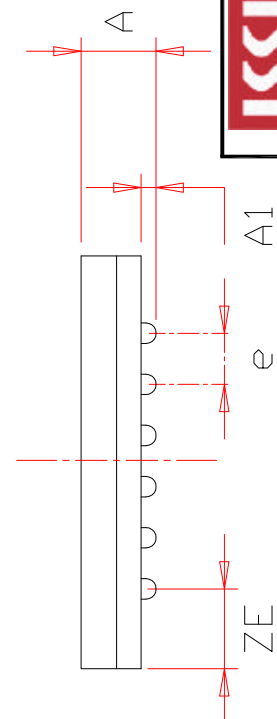
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

48L 6x8mm TF-BGA Package Outline

TITLE	REV.	DATE
	C	08/12/2008

TOP VIEW

Integrated Silicon Solution, Inc. — www.issi.com
Rev. B1
03/23/2018