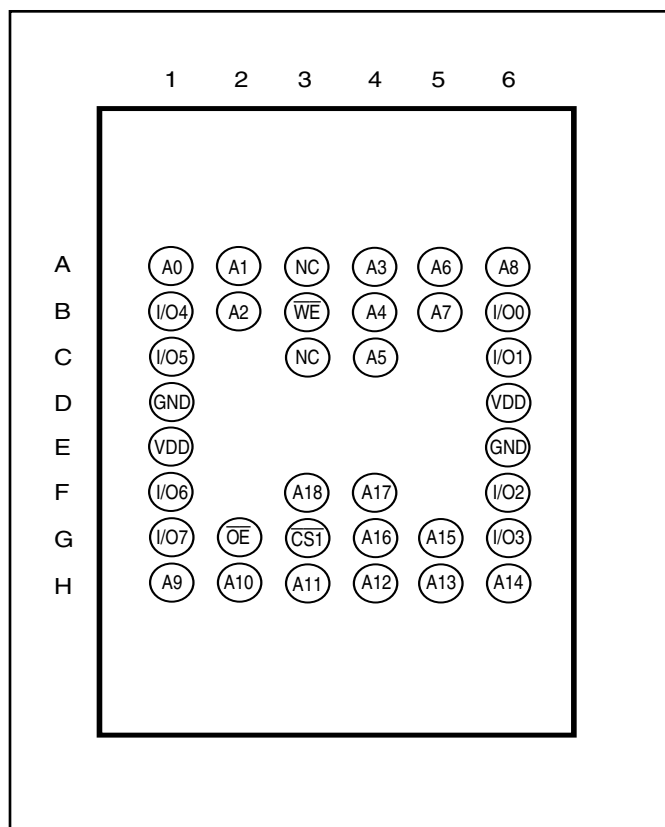


## PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{\text{CS1}}$	Chip Enable 1 Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
V <sub>DD</sub>	Power
GND	Ground

## 36-pin mini BGA (B) (6mm x 8mm) (Package Code B)

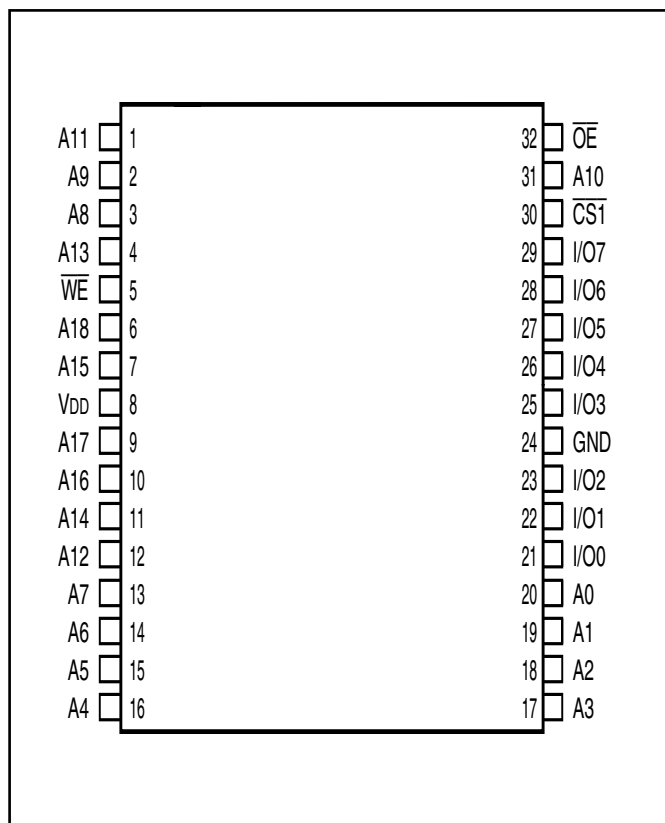


## PIN DESCRIPTIONS

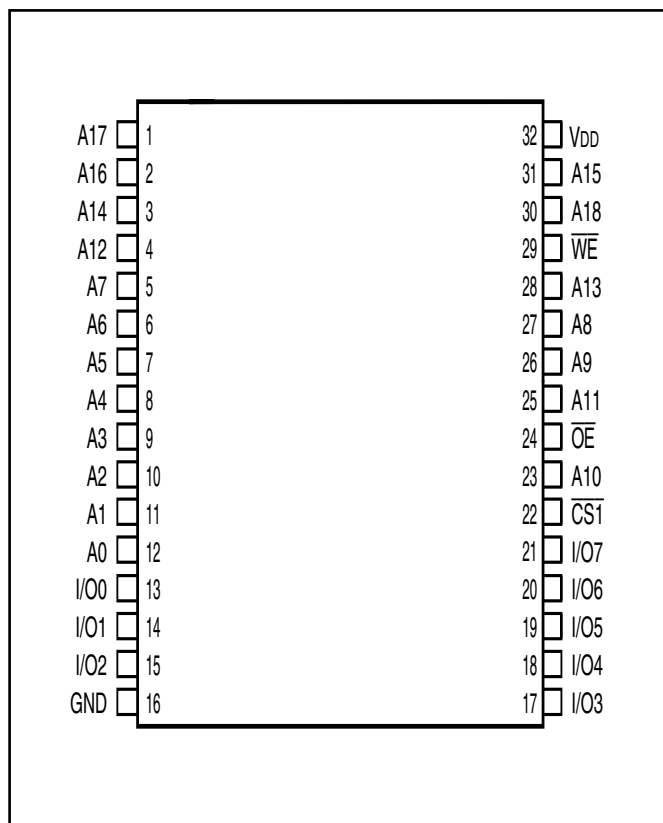
A0-A18	Address Inputs
CS1	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

## PIN CONFIGURATION

**32-pin TSOP (TYPE I), (Package Code T)**  
**32-pin sTSOP (TYPE I) (Package Code H)**



**32-pin SOP (Package Code Q)**  
**32-pin TSOP (TYPE II) (Package Code T2)**



## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	$\overline{OE}$	I/O Operation	V <sub>DD</sub> Current
Not Selected (Power-down)	X	H	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	High-Z	I <sub>CC</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC</sub>

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	−0.5 to V <sub>DD</sub> + 0.5	V
V <sub>DD</sub>	V <sub>DD</sub> Relates to GND	−0.3 to 4.0	V
T <sub>STG</sub>	Storage Temperature	−65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

## AC TEST CONDITIONS

Parameter	Unit (2.3V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level ( $V_{Ref}$ )	$V_{DD} / 2$	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 ( $\Omega$ )	1005	1213	13500
R2 ( $\Omega$ )	820	1378	10800
$V_{TM}$ (V)	3.0V	3.3V	1.8V

## AC TEST LOADS

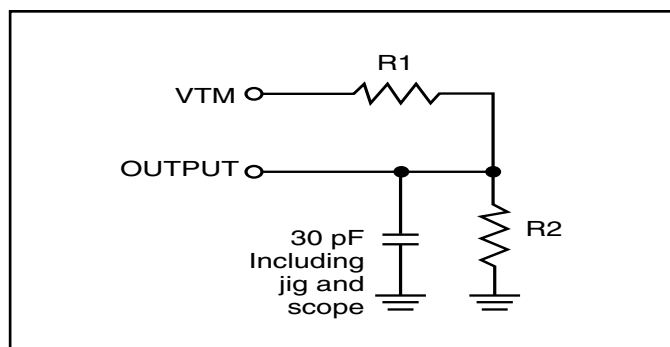


Figure 1.

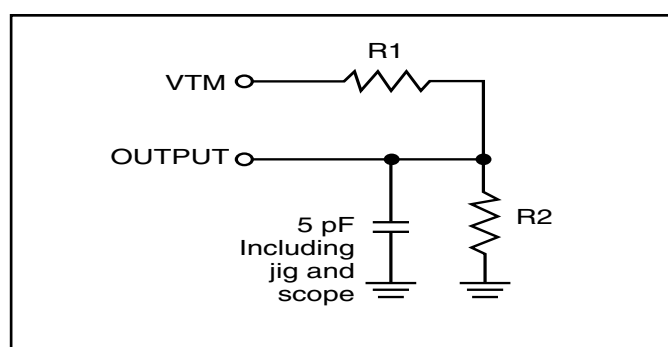


Figure 2.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 3.3V \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1 \text{ mA}$	2.4	—	V
$V_{OL}$	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH Voltage		2	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled	-1	1	$\mu\text{A}$

**Note:**

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}$ ;  $V_{IL} (\text{min.}) = -2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.  
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}$ ;  $V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 2.3V-3.6V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	1.8	—	V
$V_{OL}$	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled	-1	1	$\mu\text{A}$

**Note:**

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}$ ;  $V_{IL} (\text{min.}) = -2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.  
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}$ ;  $V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 1.65V-2.2V$

Symbol	Parameter	Test Conditions	$V_{DD}$	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$	1.65-2.2V	1.4	—	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$	1.65-2.2V	—	0.2	V
$V_{IH}$	Input HIGH Voltage		1.65-2.2V	1.4	$V_{DD} + 0.2$	V
$V_{IL}^{(1)}$	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$		-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled		-1	1	$\mu\text{A}$

**Note:**

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}$ ;  $V_{IL} (\text{min.}) = -2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.  
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}$ ;  $V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.

### OPERATING RANGE (V<sub>DD</sub>)

Range	Ambient Temperature	V <sub>DD</sub>	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	-40°C to +85°C	1.65V-2.2V	55ns
Automotive	-40°C to +125°C	1.65V-2.2V	55ns

### OPERATING RANGE (V<sub>DD</sub>)

Range	Ambient Temperature	V <sub>DD</sub> (45 ns)	V <sub>DD</sub> (35 ns)
Commercial	0°C to +70°C	2.3V-3.6V	3.3V±5%
Industrial	-40°C to +85°C	2.3V-3.6V	3.3V±5%

### OPERATING RANGE (V<sub>DD</sub>)

Range	Ambient Temperature	V <sub>DD</sub> (45 ns)
Automotive	-40°C to +125°C	2.3V-3.6V

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-35		-45		-55		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	—	20	—	15	—	15	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	—	25	—	20	—	20	
		$\overline{CE}$ = V <sub>IL</sub>	Auto.	—	30	—	25	—	25	
		V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.3V, or V <sub>IN</sub> ≤ 0.4V	typ. <sup>(2)</sup>	10						
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	—	3	—	3	—	3	mA
		I <sub>OUT</sub> = 0 mA, f = 0	Ind.	—	3	—	3	—	3	
		$\overline{CE}$ = V <sub>IL</sub>	Auto.	—	3	—	3	—	3	
		V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.3V, or V <sub>IN</sub> ≤ 0.4V								
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	—	5	—	5	—	5	μA
		$\overline{CE} \geq V_{DD} - 0.2V$ ,	Ind.	—	10	—	10	—	10	
		V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.2V, or	Auto.	—	30	—	30	—	30	
		V <sub>IN</sub> ≤ 0.2V, f = 0	typ. <sup>(2)</sup>	2						

#### Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

## READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

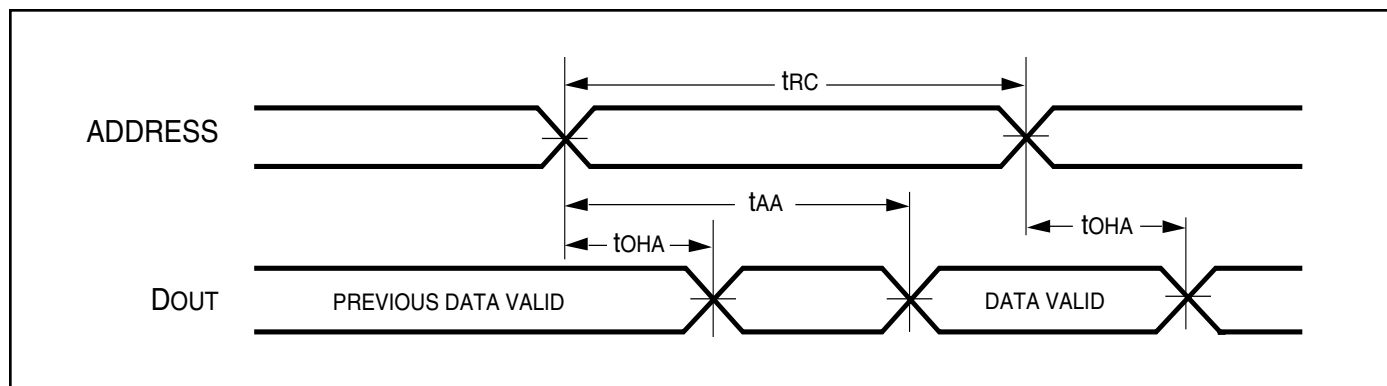
Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	35	—	45	—	55	—	ns
$t_{AA}$	Address Access Time	—	35	—	45	—	55	ns
$t_{OHA}$	Output Hold Time	10	—	10	—	10	—	ns
$t_{ACS1}$	$\overline{CS1}$ Access Time	—	35	—	45	—	55	ns
$t_{DOE}$	$\overline{OE}$ Access Time	—	10	—	20	—	25	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	—	10	—	15	—	20	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	3	—	5	—	5	—	ns
$t_{HZCS1}$	$\overline{CS1}$ to High-Z Output	0	10	0	15	0	20	ns
$t_{LZCS1}$	$\overline{CS1}$ to Low-Z Output	5	—	10	—	10	—	ns

### Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to  $V_{DD}-0.2V/V_{DD}-0.3V$  and output loading specified in Figure 1.
- Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

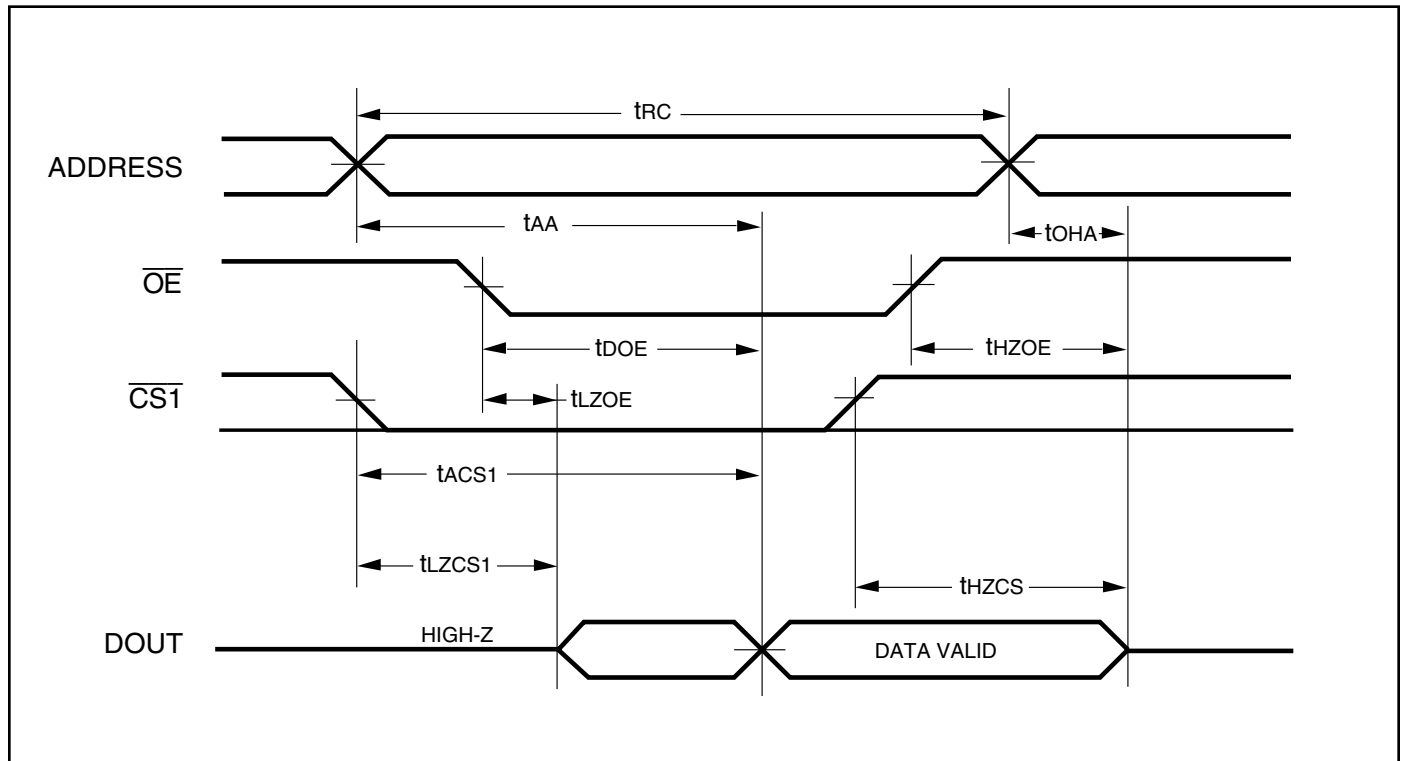
## AC WAVEFORMS

### READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ )



## AC WAVEFORMS

### READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CS1}$ , $\overline{OE}$ Controlled)



#### Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1} = V_{IL}$ .  $\overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

## WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)

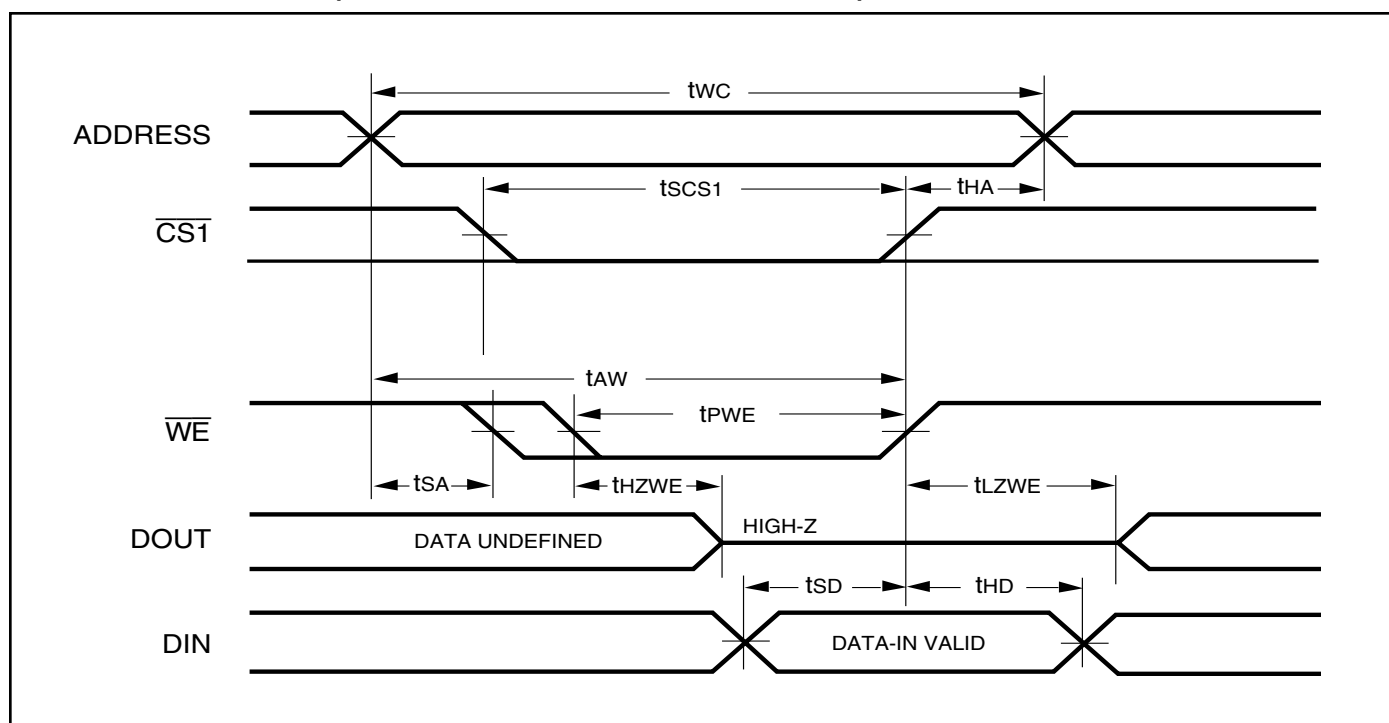
Symbol	Parameter	35ns		45ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	35	—	45	—	55	—	ns
t <sub>SCS1</sub>	$\overline{\text{CS1}}$ to Write End	25	—	35	—	45	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	25	—	35	—	45	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	25	—	35	—	40	—	ns
t <sub>SD</sub>	Data Setup to Write End	20	—	20	—	25	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	$\overline{\text{WE}}$ LOW to High-Z Output	—	10	—	20	—	20	ns
t <sub>LZWE</sub> <sup>(3)</sup>	$\overline{\text{WE}}$ HIGH to Low-Z Output	3	—	5	—	5	—	ns

### Notes:

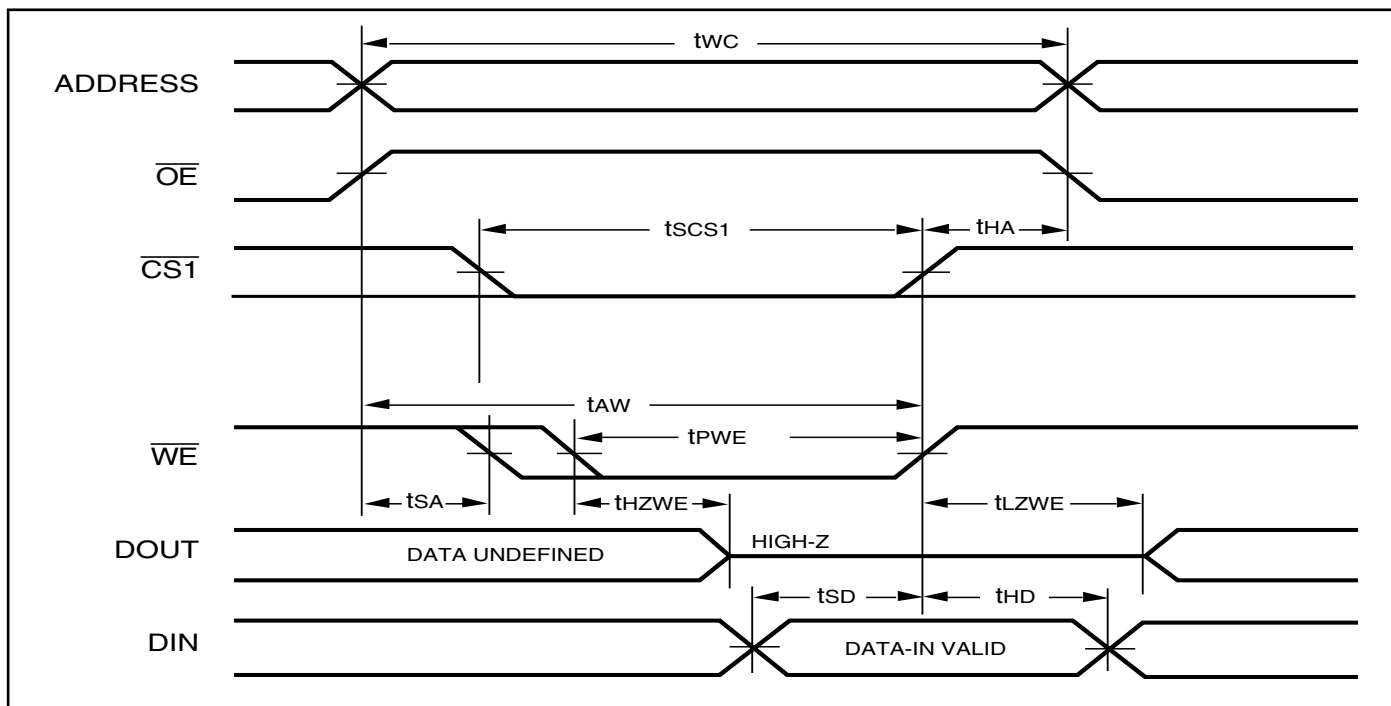
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{\text{CS1}}$  LOW and  $\overline{\text{WE}}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

## AC WAVEFORMS

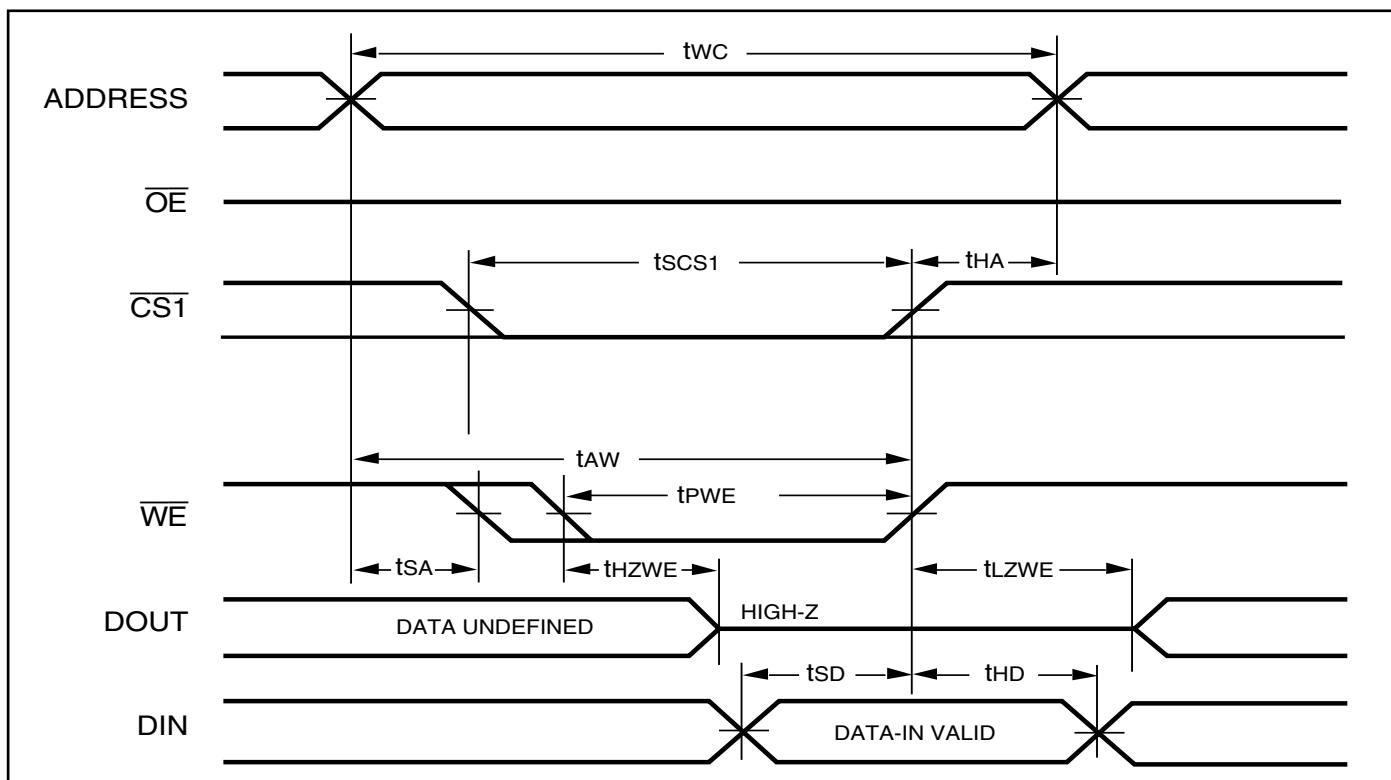
### WRITE CYCLE NO. 1 ( $\overline{\text{CS1}}$ Controlled, $\overline{\text{OE}}$ = HIGH or LOW)



**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)

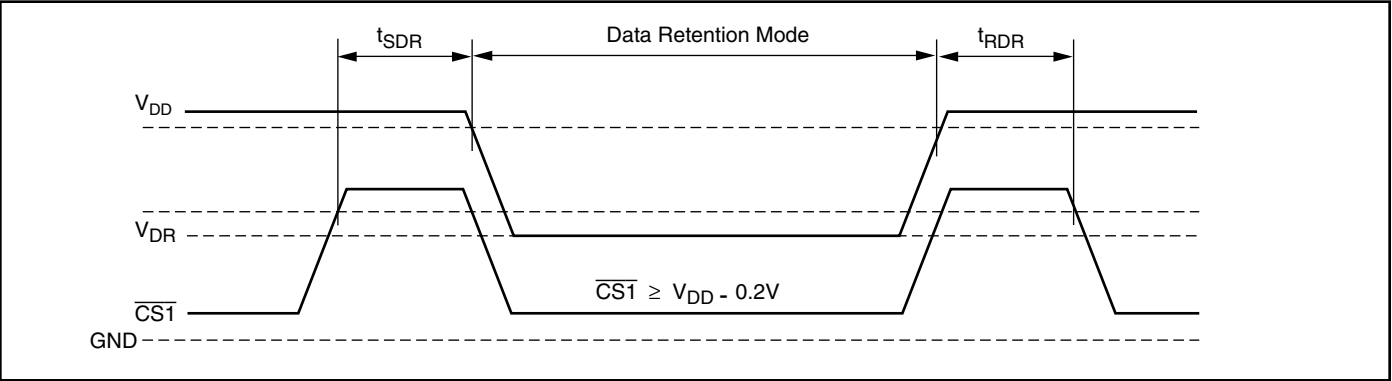


DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.2	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, $\overline{\text{CS1}} \geq V_{\text{DD}} - 0.2\text{V}$	Com. Ind. Auto. typ. <sup>(1)</sup>	3 7 20	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

Note: 1. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ( $\overline{\text{CS1}}$  Controlled)



## ORDERING INFORMATION

### IS62WV5128DALL (1.65V-2.2V)

Industrial Range: -40°C to +85°C

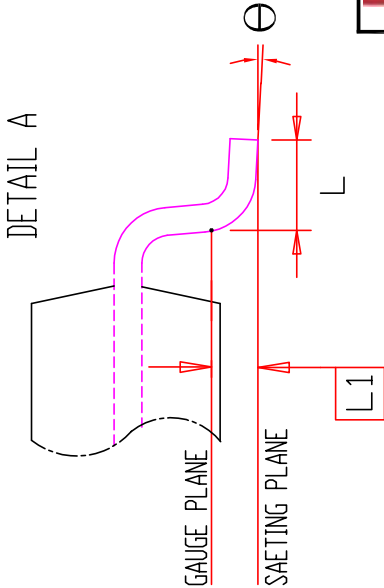
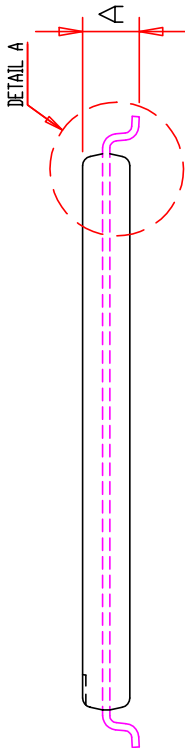
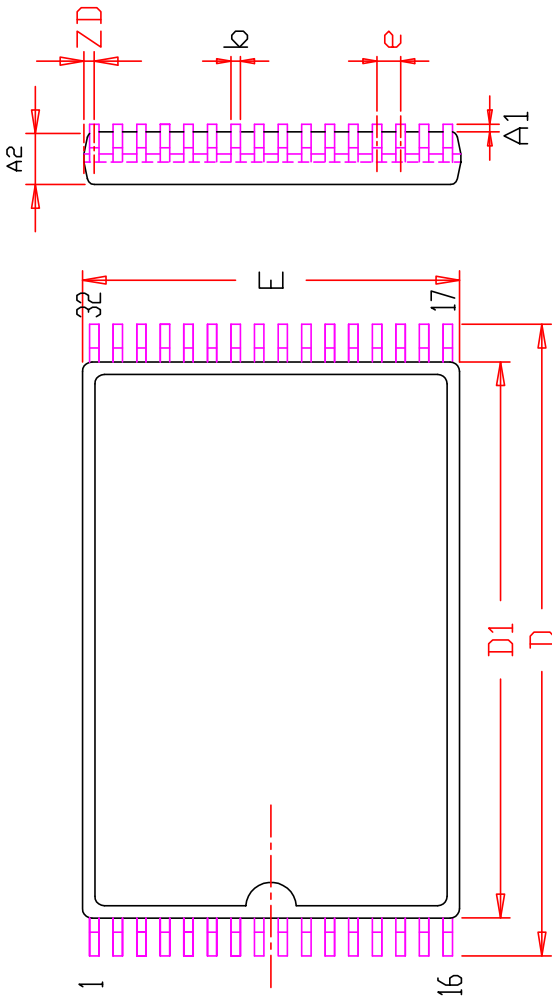
Speed (ns)	Order Part No.	Package
55	IS62WV5128DALL-55TLI	TSOP, TYPE I, Lead-free (8 x 20 mm)
55	IS62WV5128DALL-55T2LI	TSOP, TYPE II, Lead-free
55	IS62WV5128DALL-55HLI	sTSOP, TYPE I, Lead-free (8 x 13.4 mm)
55	IS62WV5128DALL-55BI	mini BGA (6mmx8mm)
	IS62WV5128DALL-55BLI	mini BGA (6mmx8mm), Lead-free

## ORDERING INFORMATION

### IS62WV5128BLL (2.3V - 3.6V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62WV5128DBLL-45TLI	TSOP, TYPE I, Lead-free (8 x 20 mm)
45	IS62WV5128DBLL-45QLI	SOP, Lead-free
45	IS62WV5128DBLL-45T2LI	TSOP, TYPE II, Lead-free
45	IS62WV5128DBLL-45HLI	sTSOP, TYPE I, Lead-free (8 x 13.4 mm)
45	IS62WV5128DBLL-45BI	mini BGA (6mmx8mm)
45	IS62WV5128DBLL-45BLI	mini BGA (6mmx8mm), Lead-free

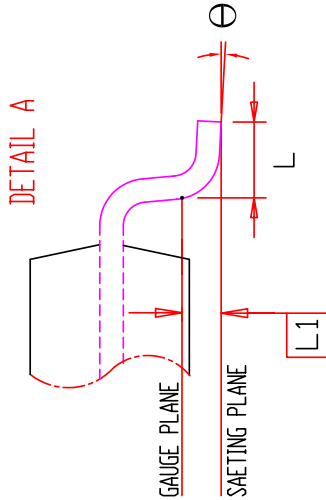
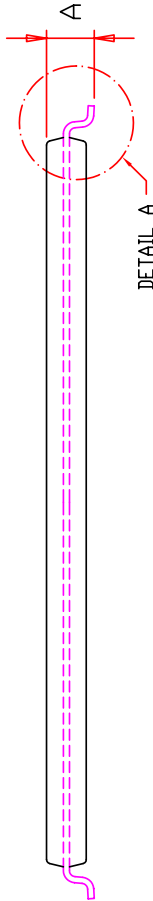
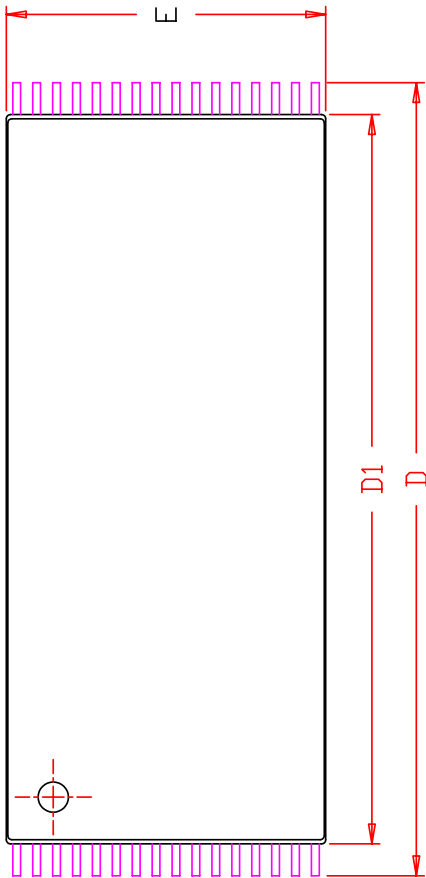
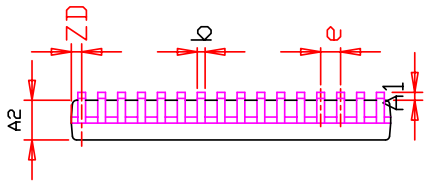


**NOTE :**

- 1. CONTROLLING DIMENSION : MM
- 2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
- 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
- 4. Reference Document : JEDEC MO-183

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NDM	MAX	MIN	NDM	MAX
A	0.95		1.20	0.037		0.047
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

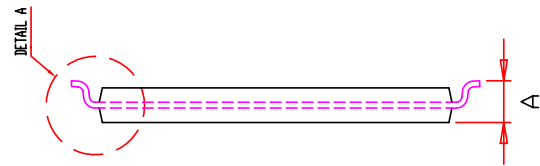
ISSI	TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	E	DATE	04/24/2008
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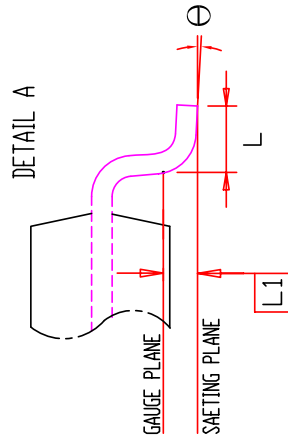
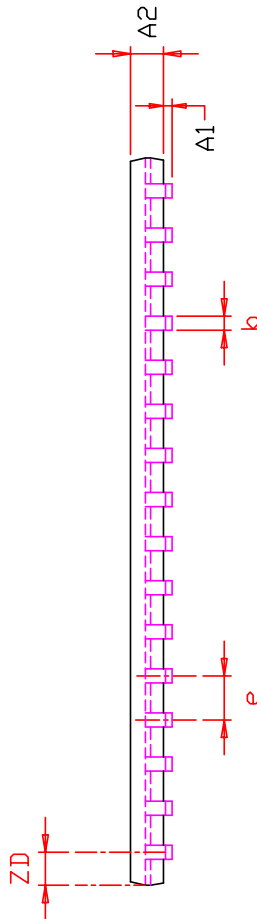
NOTE :

- 1. Controlling dimension : mm
- 2. Dimension D1 adn E do not include mold protrusion .
- 3. Dimension b does not include dambar protrusion/intrusion.
- 4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00		1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e		0.50 BSC.	
L	0.40		0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
Θ	0	5°	8°



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.52	0.012		0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	1.27 BSC.			0.050 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.95 REF.			0.037 REF.		
θ	0		8°	0		8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	32L 400mil TSOP-2 Package Outline	REV.	E	DATE	06/23/2009

