

**Electrical Characteristics @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.1	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
G <sub>fs</sub>	Forward Transconductance	6.2	—	—	S	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-25	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V <sub>GS</sub> = 20V
Q <sub>G</sub>	Total Gate Charge	—	—	60	nC	I <sub>D</sub> = -15.8A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	13		V <sub>DS</sub> = -50V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	35.2		V <sub>GS</sub> = -10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	35	ns	V <sub>DD</sub> = -50V
t <sub>r</sub>	Rise Time	—	—	85		I <sub>D</sub> = -15.8A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	85		R <sub>G</sub> = 7.5Ω
t <sub>f</sub>	Fall Time	—	—	65		V <sub>GS</sub> = -10V
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C <sub>iss</sub>	Input Capacitance	—	1400	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	600	—		V <sub>DS</sub> = -25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	200	—		f = 1.0MHz

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-15.8	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-60		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-5.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -15.8A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	280	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -15.8A, V <sub>DD</sub> ≤ -50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	3.6	μC	di/dt = -100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>θJC</sub>	Junction-to-Case	—	—	1.25	°C/W	
R <sub>θCS</sub>	Case-to-sink	—	0.21	—		
R <sub>θJA</sub>	Junction-to-Ambient	—	—	80		Typical socket mount

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.  
 ② V<sub>DD</sub> = -50V, starting T<sub>J</sub> = 25°C, L = 5.1mH, Peak I<sub>L</sub> = -15.8A, V<sub>GS</sub> = -10V  
 ③ I<sub>SD</sub> ≤ -15.8A, di/dt ≤ -200A/μs, V<sub>DD</sub> ≤ -100V, T<sub>J</sub> ≤ 150°C  
 ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

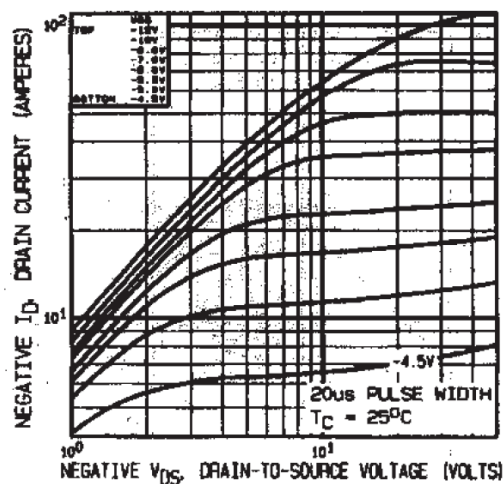


Fig 1. Typical Output Characteristics

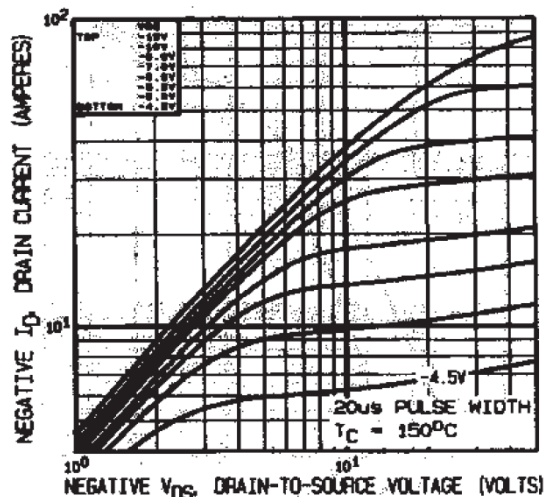


Fig 2. Typical Output Characteristics

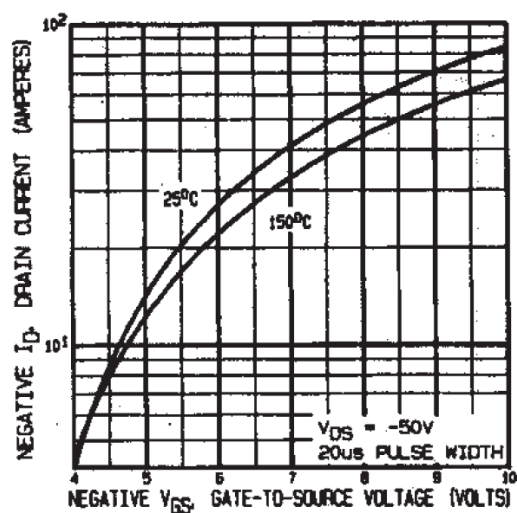


Fig 3. Typical Transfer Characteristics

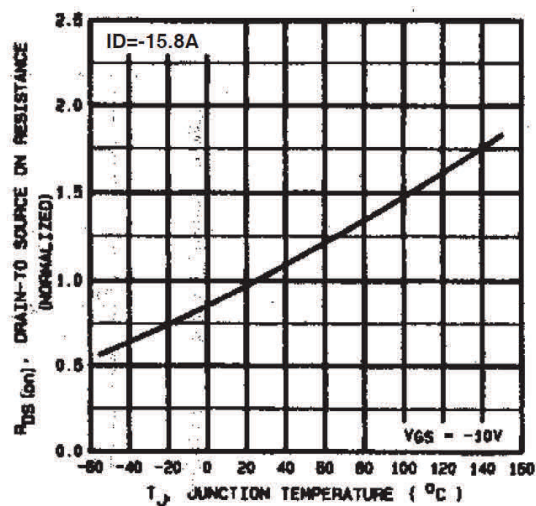


Fig 4. Normalized On-Resistance Vs. Temperature

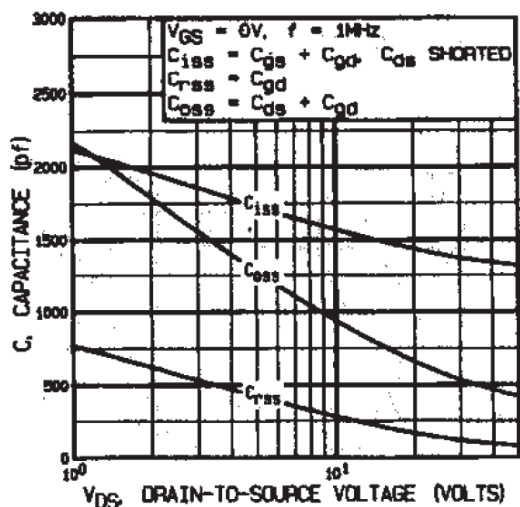


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

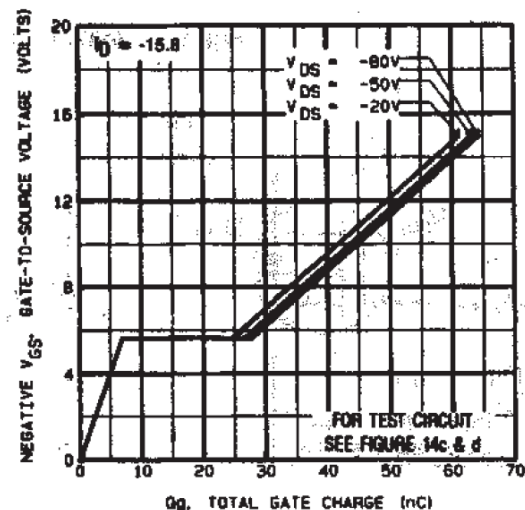
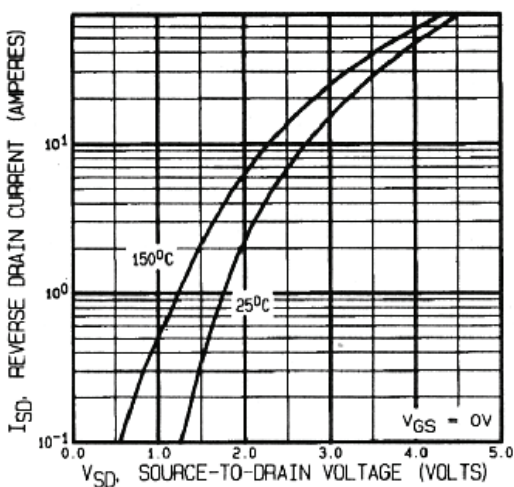
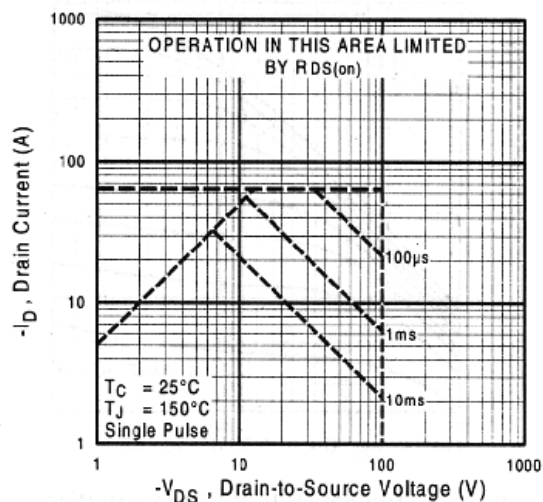


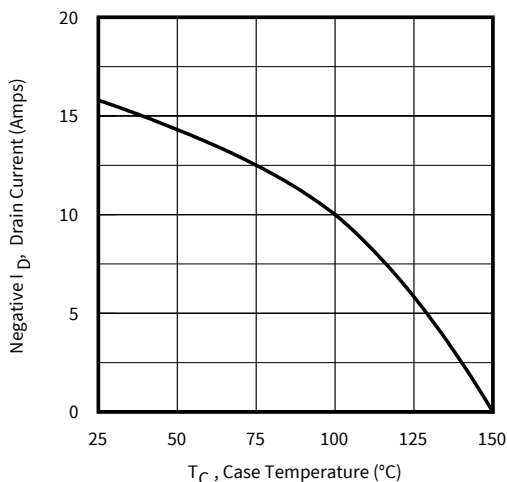
Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



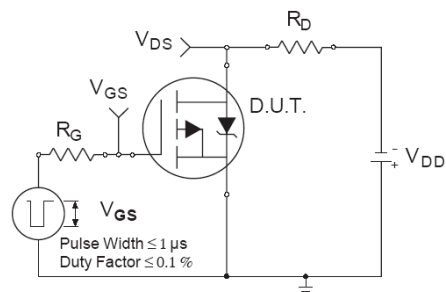
**Fig 7.** Typical Source-Drain Diode Forward Voltage



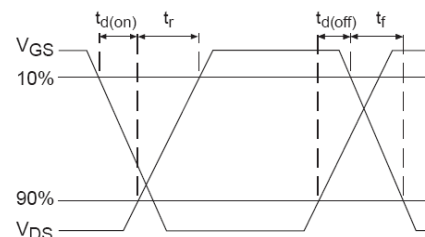
**Fig 8.** Maximum Safe Operating Area



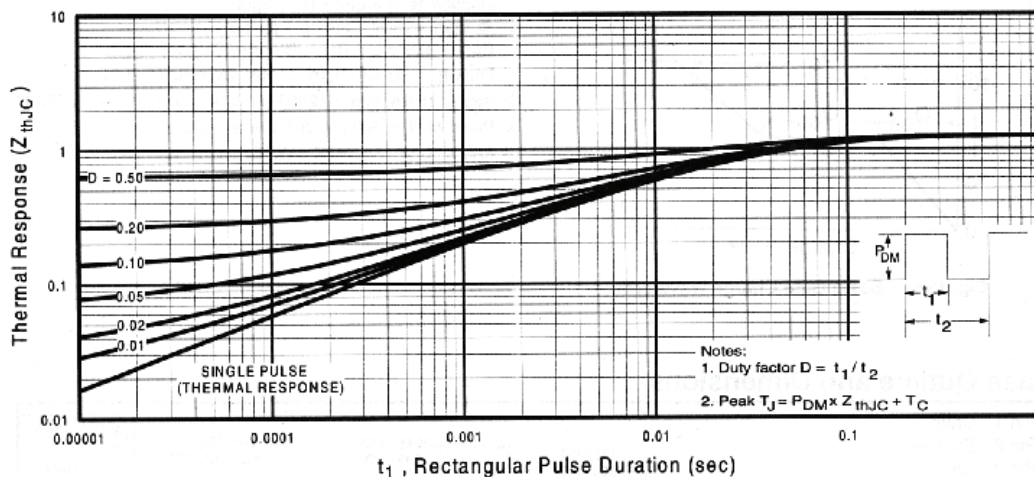
**Fig 9.** Maximum Drain Current Vs. Case Temperature



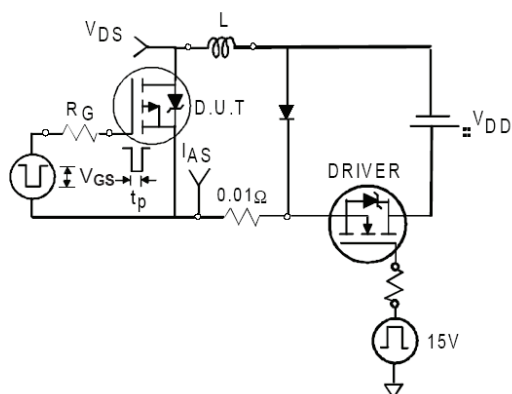
**Fig 10a.** Switching Time Test Circuit



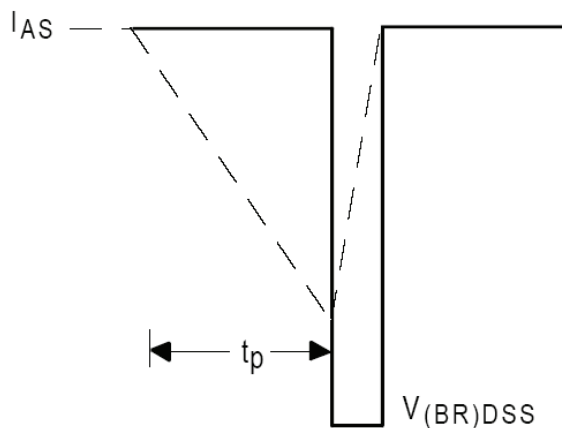
**Fig 10b.** Switching Time Waveforms



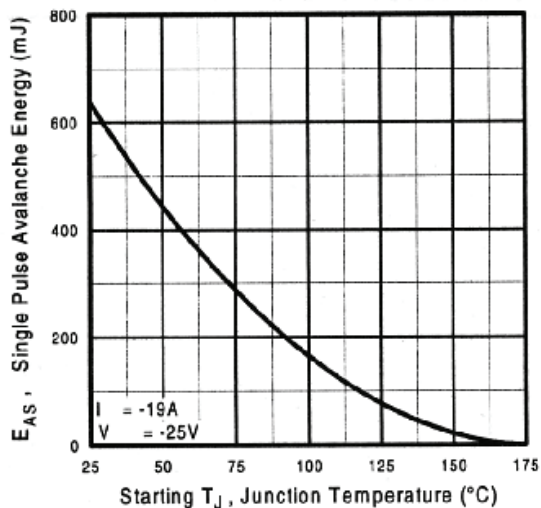
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



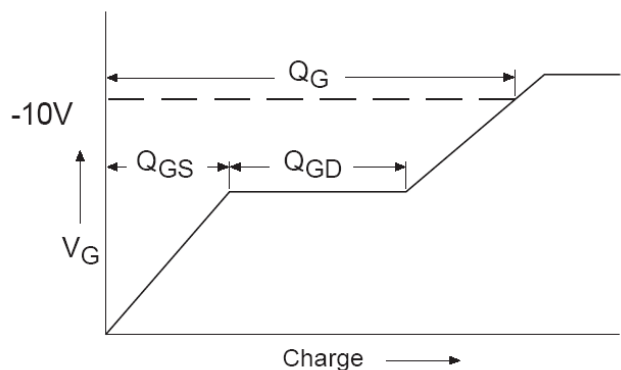
**Fig 12a.** Unclamped Inductive Test Circuit



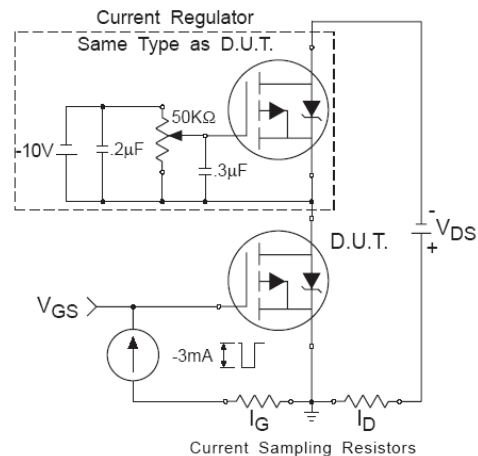
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

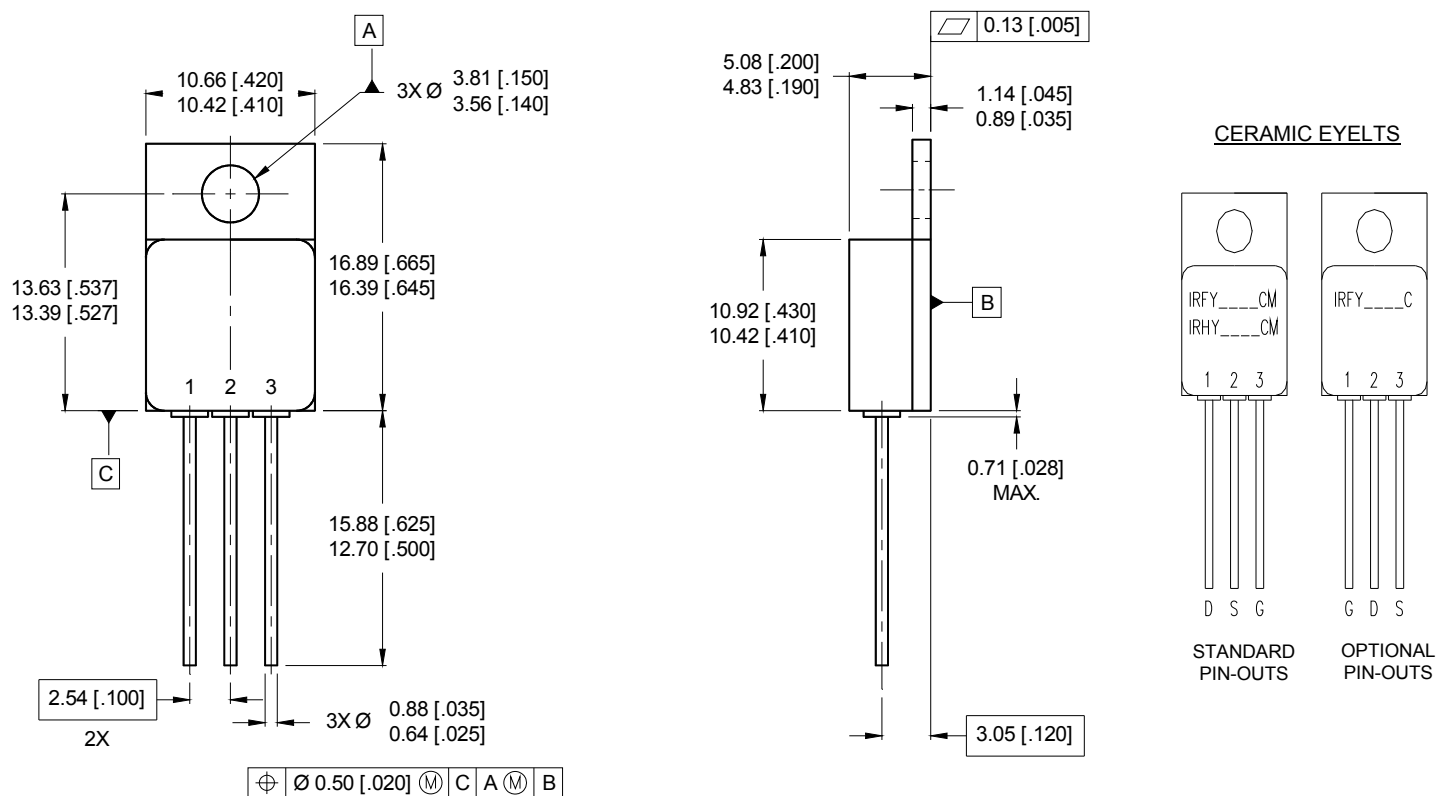


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Case Outline and Dimensions — TO-257AA



### NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

### LEAD ASSIGNMENT

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

### **IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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