READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 13 address inputs (A_0 -A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later-occurring signal and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225AB and DS1225AD execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1225AD provides full-functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become “don’t care,” and all outputs become high-impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1225AB and 4.5 volts for the DS1225AD.

FRESHNESS SEAL

Each DS1225 is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP} , the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	+260°C for 10 seconds
Caution: Do Not Reflow	(Wave or Hand Solder Only)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(T_A: See Note 10)
(V_{CC} =5V ± 5% for DS1225AB)
(V_{CC} =5V ± 10% for DS1225AD)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} > V_{IH} < V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ =2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ =V_{CC} -0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current (Commercial)	I_{CC01}			75	mA	
Operating Current (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1225AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1225AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(T_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

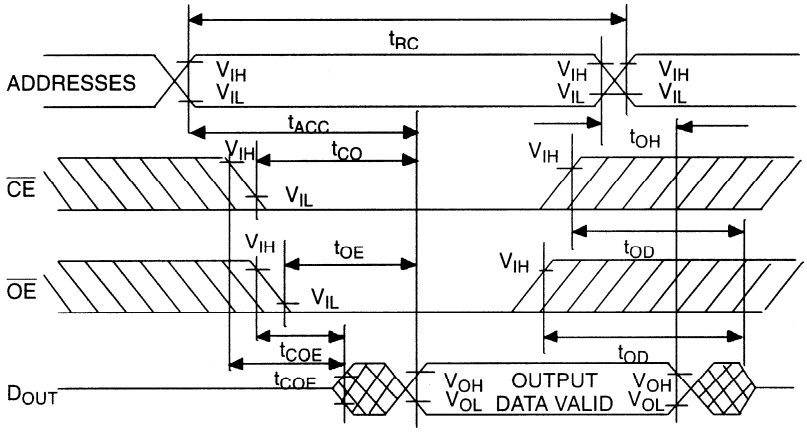
(T_A: See Note 10)
(V_{CC} =5V ± 5% for DS1225AB)
(V_{CC} =5V ± 10% for DS1225AD)

PARAMETER	SYMBOL	DS1225AB-70 DS1225AD-70		DS1225AB-85 DS1225AD-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

AC ELECTRICAL CHARACTERISTICS (cont'd)

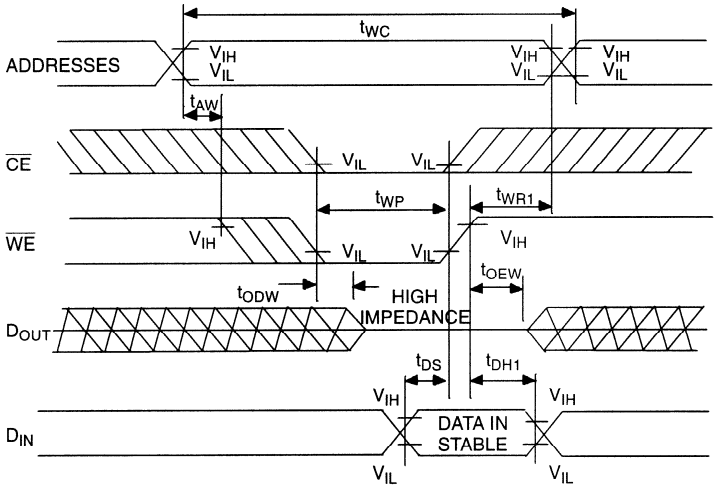
PARAMETER	SYMBOL	DS1225AB- 150 DS1225AD- 150		DS1225AB-200 DS1225AD-200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		100		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

READ CYCLE



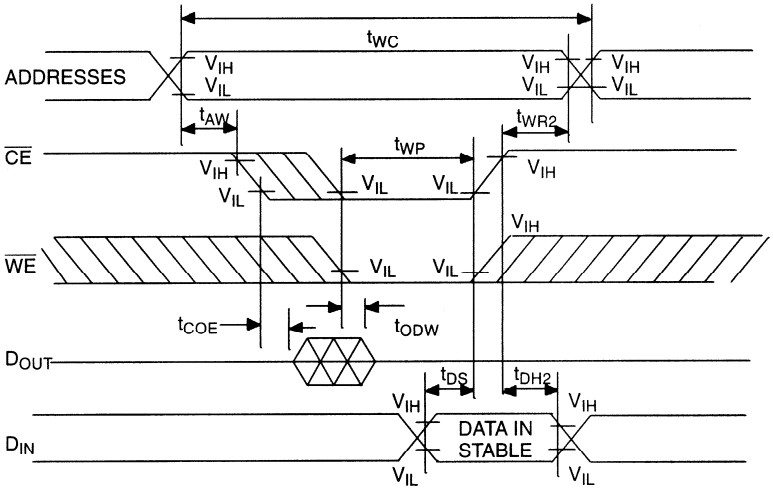
SEE NOTE 1

WRITE CYCLE 1



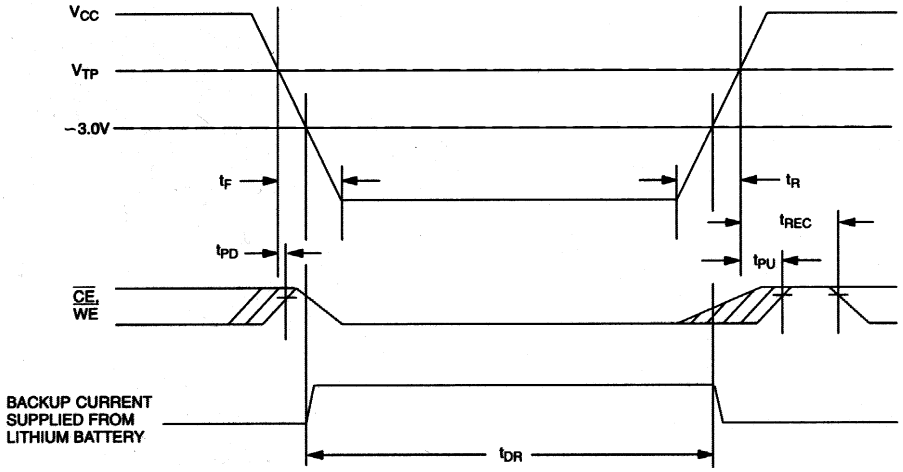
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(T_A : See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	11
V_{CC} slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} slew from 0V to V_{TP}	t_R	300			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high-impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1225AB and each DS1225AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user. This parameter is guaranteed by design and is not 100% tested.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC} .
12. t_{WR1} , t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} , t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1225 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

DC TEST CONDITIONS

Outputs Open
Cycle = 200ns for Operating Current
All Voltages Are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	SUPPLY TOLERANCE	PIN/PACKAGE	SPEED GRADE
DS1225AB-70	0°C to +70°C	5V ± 5%	28 / 720 EMOD	70ns
DS1225AB-70+	0°C to +70°C	5V ± 5%	28 / 720 EMOD	70ns
DS1225AB-70IND	-40°C to +85°C	5V ± 5%	28 / 720 EMOD	70ns
DS1225AB-70IND+	-40°C to +85°C	5V ± 5%	28 / 720 EMOD	70ns
DS1225AB-85	0°C to +70°C	5V ± 5%	28 / 720 EMOD	85ns
DS1225AB-85+	0°C to +70°C	5V ± 5%	28 / 720 EMOD	85ns
DS1225AB-150	0°C to +70°C	5V ± 5%	28 / 720 EMOD	150ns
DS1225AB-150+	0°C to +70°C	5V ± 5%	28 / 720 EMOD	150ns
DS1225AB-150IND	-40°C to +85°C	5V ± 5%	28 / 720 EMOD	150ns
DS1225AB-150IND+	-40°C to +85°C	5V ± 5%	28 / 720 EMOD	150ns
DS1225AB-200	0°C to +70°C	5V ± 5%	28 / 720 EMOD	200ns
DS1225AB-200+	0°C to +70°C	5V ± 5%	28 / 720 EMOD	200ns
DS1225AB-200IND	-40°C to +85°C	5V ± 5%	28 / 720 EMOD	200ns
DS1225AB-200IND+	-40°C to +85°C	5V ± 5%	28 / 720 EMOD	200ns
DS1225AD-70	0°C to +70°C	5V ± 10%	28 / 720 EMOD	70ns
DS1225AD-70+	0°C to +70°C	5V ± 10%	28 / 720 EMOD	70ns
DS1225AD-70IND	-40°C to +85°C	5V ± 10%	28 / 720 EMOD	70ns
DS1225AD-70IND+	-40°C to +85°C	5V ± 10%	28 / 720 EMOD	70ns
DS1225AD-85	0°C to +70°C	5V ± 10%	28 / 720 EMOD	85ns
DS1225AD-85+	0°C to +70°C	5V ± 10%	28 / 720 EMOD	85ns
DS1225AD-150	0°C to +70°C	5V ± 10%	28 / 720 EMOD	150ns
DS1225AD-150+	0°C to +70°C	5V ± 10%	28 / 720 EMOD	150ns
DS1225AD-150IND	-40°C to +85°C	5V ± 10%	28 / 720 EMOD	150ns
DS1225AD-150IND+	-40°C to +85°C	5V ± 10%	28 / 720 EMOD	150ns
DS1225AD-200	0°C to +70°C	5V ± 10%	28 / 720 EMOD	200ns
DS1225AD-200+	0°C to +70°C	5V ± 10%	28 / 720 EMOD	200ns
DS1225AD-200IND	-40°C to +85°C	5V ± 10%	28 / 720 EMOD	200ns
DS1225AD-200IND+	-40°C to +85°C	5V ± 10%	28 / 720 EMOD	200ns

+ Denotes lead(Pb)-free/RoHS-compliant product.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to http://www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 EDIP	MDT28+2	**21-0245**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
121907	Added package information table. Removed the DIP module package drawing and dimension table.	9