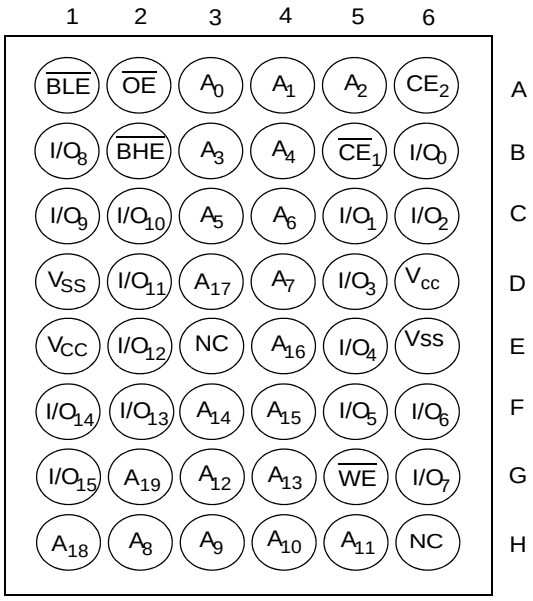
Contents

Pin Configurations

Figure 1. 48-Ball VFBGA pinout (Top View) [1, 2]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[3]	Max		Typ[3]	Max	Typ[3]	Max	Typ[3]	Max
CY62167EV18LL	1.65	1.8	2.25	55	2.2	4.0	25	30	1.5	12
CY62167EV30LL[4]										

Notes
1. NC pins are not connected on the die.
2. Ball H6 for the VFBGA package can be used to upgrade to a 32 M density.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
4. This part can be operated in the V_{CC} range of 1.65 V–2.25 V at 55ns speed. It can also be operated in the V_{CC} range of 2.2 V–3.6 V at 45ns speed.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.2 V to 2.45 V ($V_{CC(max)}$ + 0.2 V)

DC voltage applied to outputs in High Z state [5, 6] ..... –0.2 V to 2.45 V ($V_{CC(max)}$ + 0.2 V)

DC input voltage[5, 6] ..... –0.2 V to 2.45 V ($V_{CC(max)}$ + 0.2 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch up current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[7]
CY62167EV18LL	Industrial	–40 °C to +85 °C	1.65 V to 2.25 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	1.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	–	–	0.2	V
V_{IH}	Input HIGH voltage	V_{CC} = 1.65 V to 2.25 V	1.4	–	V_{CC} + 0.2 V	V
V_{IL}	Input LOW voltage	V_{CC} = 1.65 V to 2.25 V	–0.2	–	0.4	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}; V_{CC} = V_{CC}(max); I_{OUT} = 0 mA; CMOS levels	–	25	30	mA
		f = 1 MHz; I_{OUT} = 0 mA; CMOS levels	–	2.2	4.0	mA
I_{SB1}[9]	Automatic power down current – CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2 V), f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = $V_{CC(max)}$	–	1.5	12	µA
I_{SB2}[9]	Automatic power down current – CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$	–	1.5	12	µA

Notes
5. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns.
6. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full Device AC operation is based on a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Chip enables ($\overline{CE_1}$ and CE_2), and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be tied to CMOS levels to meet the I_{SB1} /I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

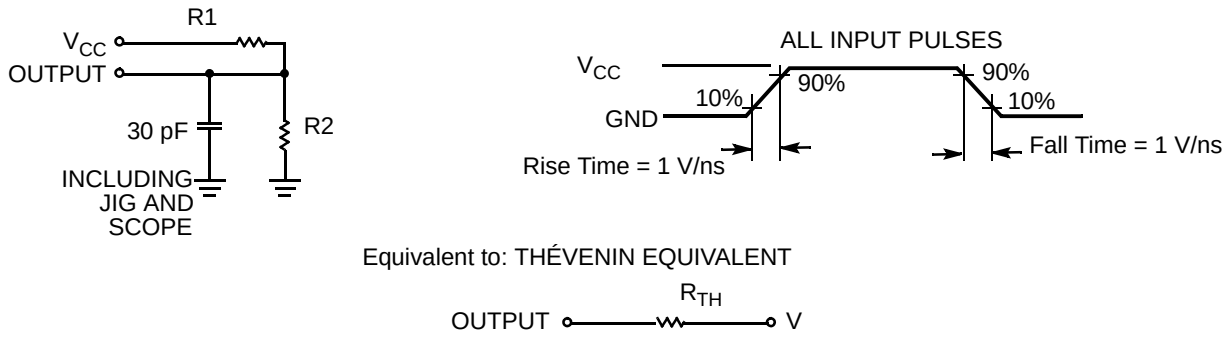
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal resistance (junction to case)		16	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	1.8 V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Note
10. Tested initially and after any design or process changes that may affect these parameters.

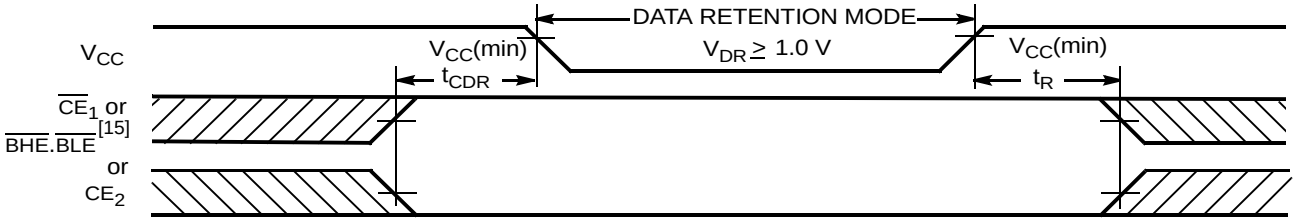
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR}[12]	Data retention current	V_{CC} = 1.0 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	10	µA
t_{CDR}[13]	Chip deselect to data retention time		0	–	–	ns
t_R[14]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
12. Chip enables ($\overline{CE_1}$ and CE_2), and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be tied to CMOS levels to meet the I_{SB1} /I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 µs or stable at V_{CC}(min) ≥ 100 µs.
15. $\overline{BHE}$. $\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter [16, 17]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[18]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[18, 19]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[18]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[18, 19]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-down	–	55	ns
t_{DBE}	BLE/$\overline{BHE}$ LOW to data valid	–	55	ns
t_{LZBE}	BLE/$\overline{BHE}$ LOW to Low Z[18]	10	–	ns
t_{HZBE}	BLE/$\overline{BHE}$ HIGH to High Z[18, 19]	–	18	ns
Write Cycle[20, 21]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse Width	40	–	ns
t_{BW}	BLE/$\overline{BHE}$ LOW to write end	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[18, 19]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[18]	10	–	ns

Notes

16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. Test conditions for all parameters other than tri-state parameters are based on signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
18. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
19. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the output enters a high impedance state.
20. The internal memory write time is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled).[22, 23]

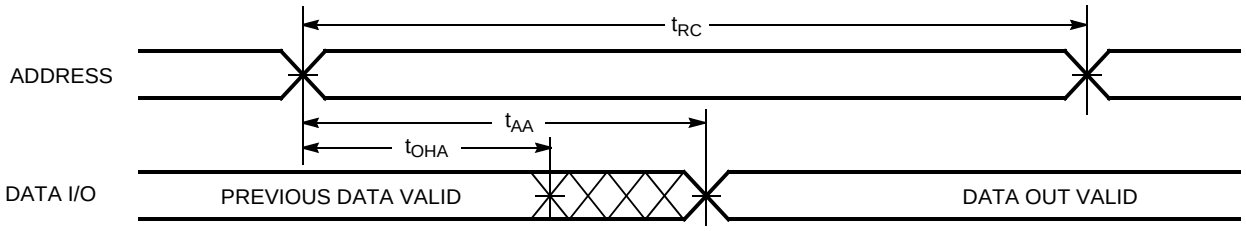
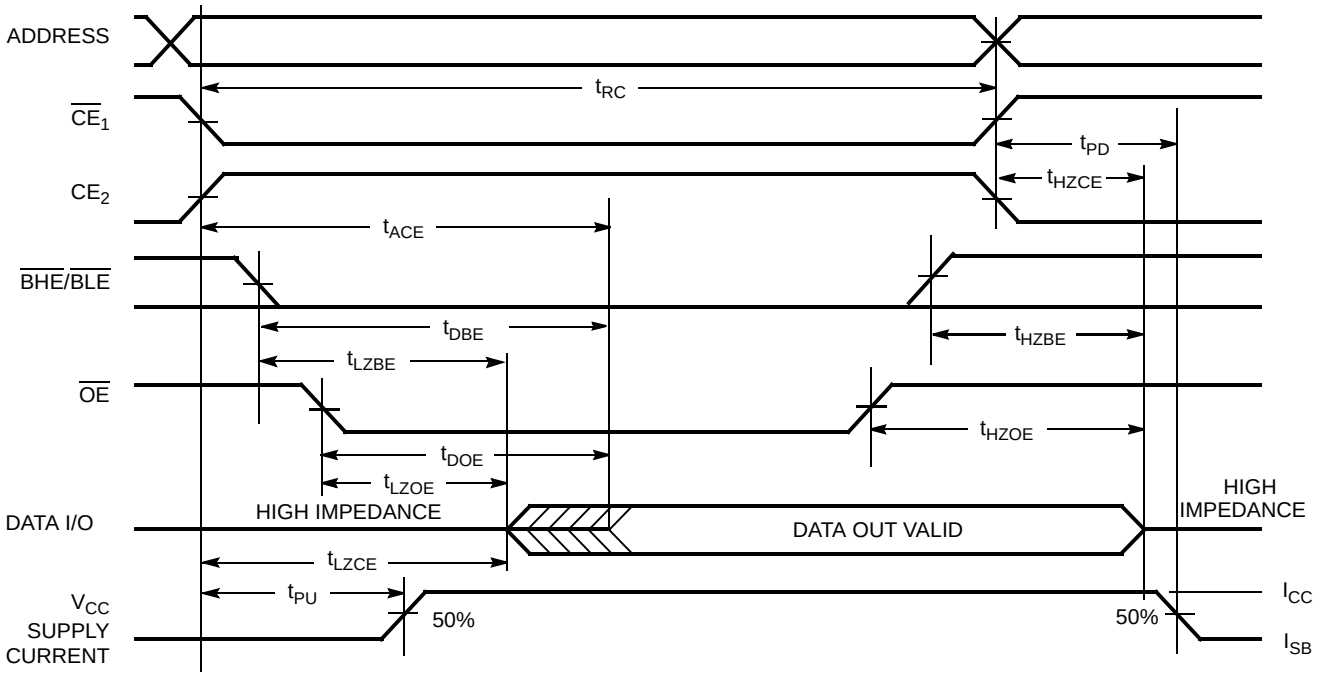


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [23, 24]



Notes
22. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}.
23. $\overline{WE}$ is HIGH for read cycle.
24. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [25, 26, 27]

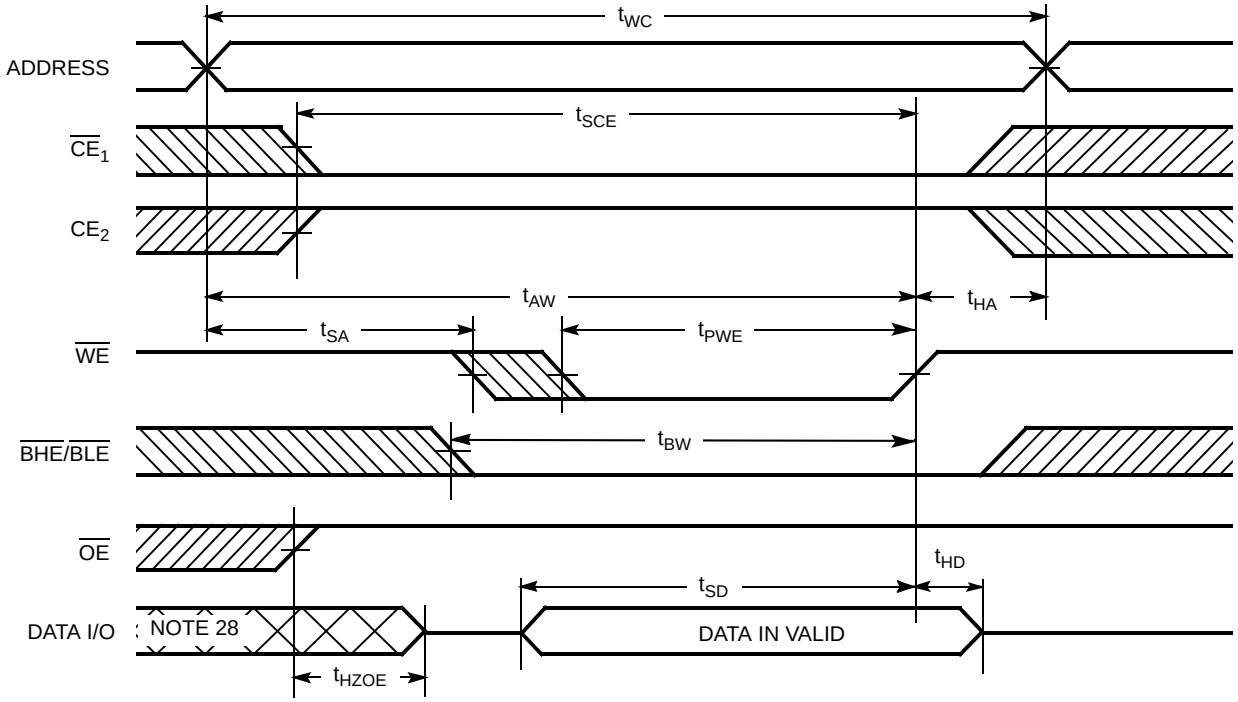
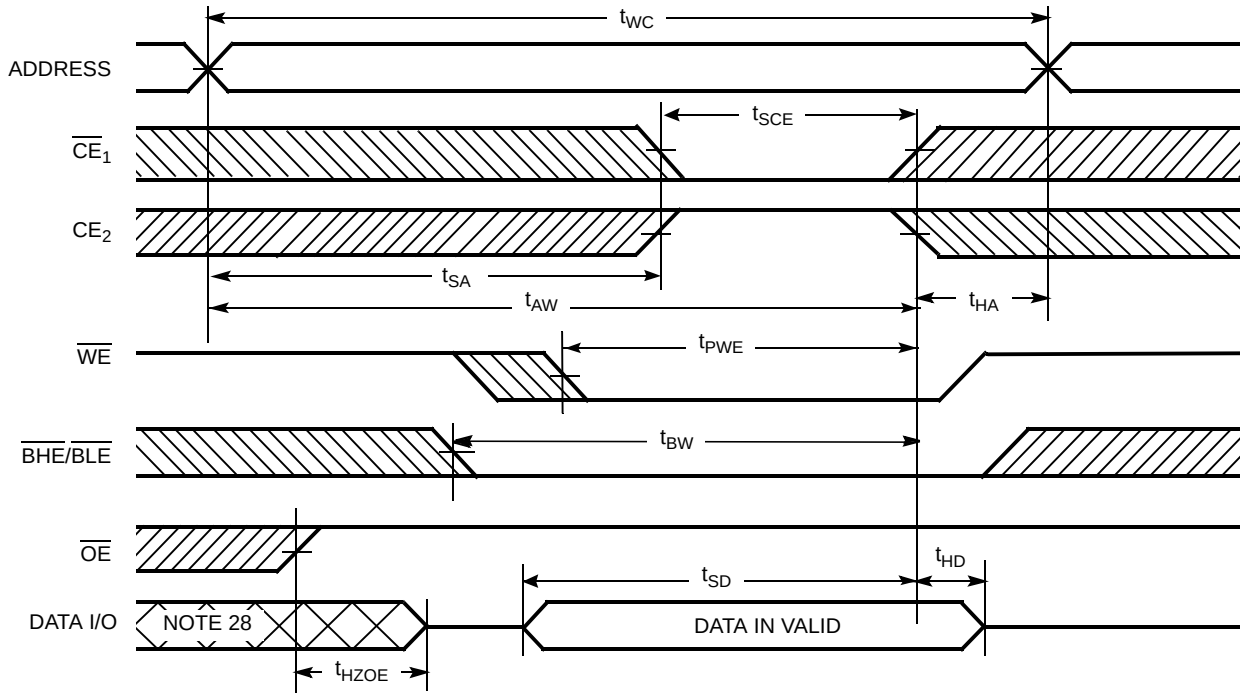


Figure 7. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [25, 26, 27]



Notes

25. The internal memory write time is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (WE controlled, OE LOW) [29, 31]

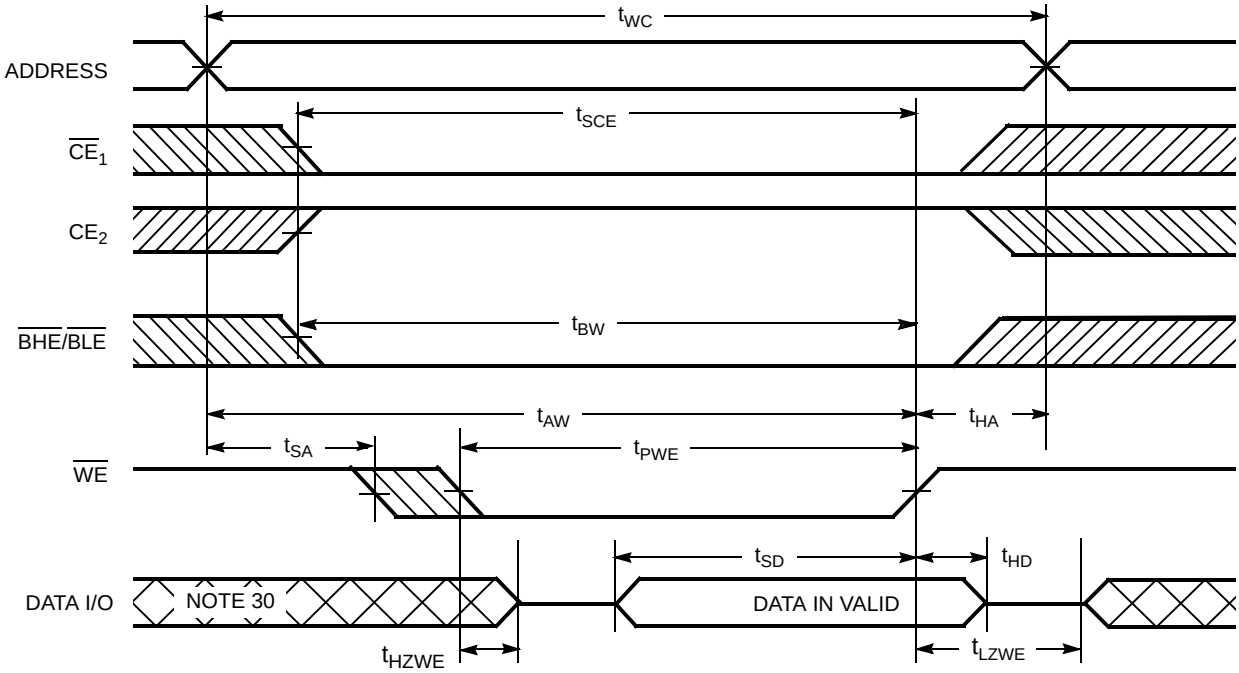
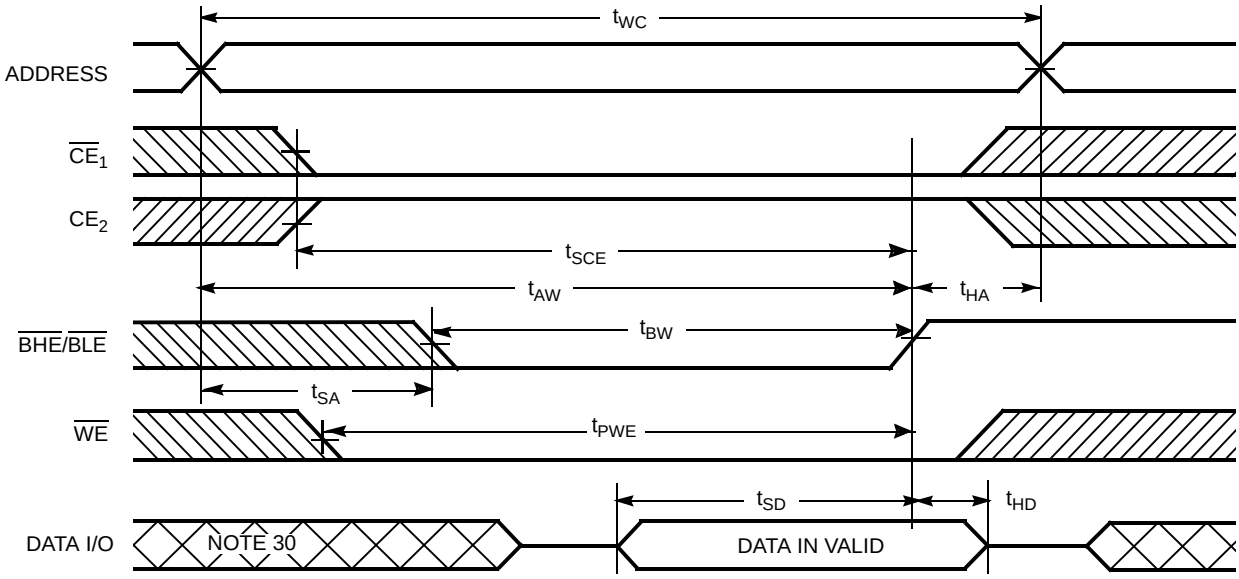


Figure 9. Write Cycle No. 4 (BHE/BLE Controlled) [29]



Notes
29. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
30. During this period the I/Os are in output state. Do not apply input signals.
31. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

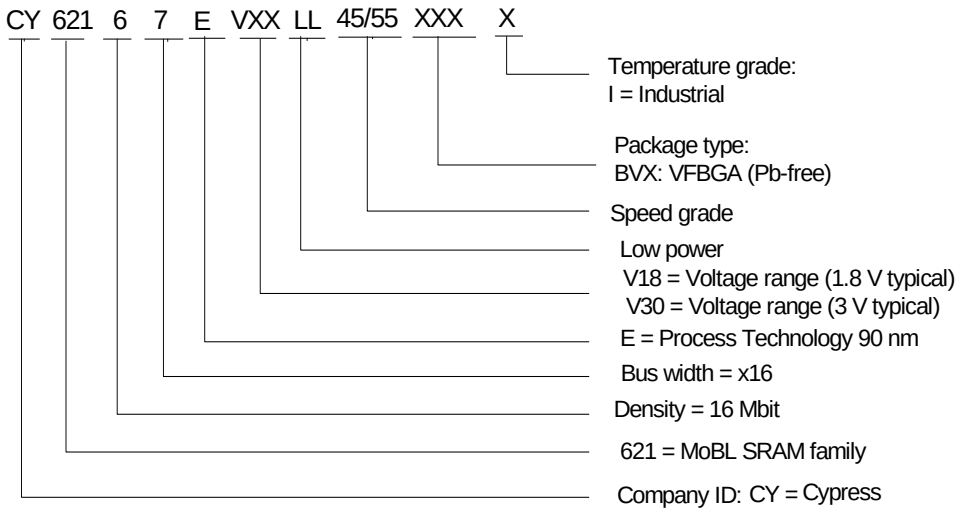
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[32]	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X[32]	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X[32]	X[32]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note
32. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167EV18LL-55BVI	51-85150	48-ball VFBGA (6 × 8 × 1 mm)	Industrial
	CY62167EV18LL-55BVXI		48-ball VFBGA (6 × 8 × 1 mm) (Pb-free)	
	CY62167EV30LL-45BVI [33]		48-ball VFBGA (6 × 8 × 1 mm)	

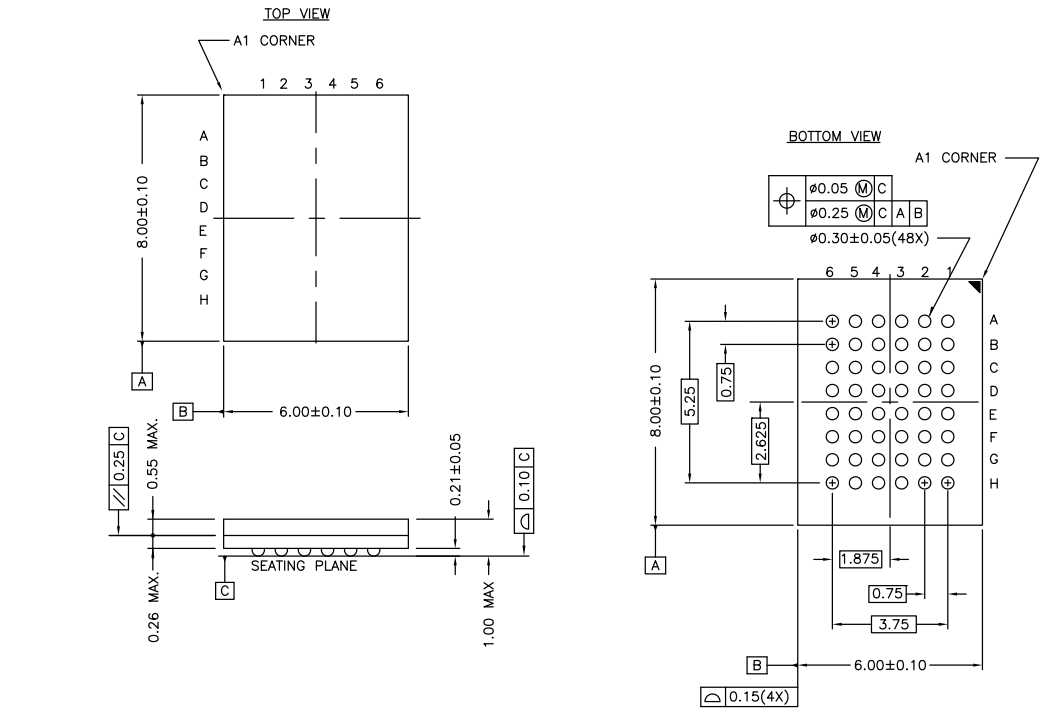
Ordering Code Definitions



Note
33. This part can be operated in the V_{CC} range of 1.65 V to 2.25 V at 55 ns speed. It can also be operated in the V_{CC} range of 2.2 V–3.6 V at 45ns speed.

Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62167EV18 MoBL®, 16-Mbit (1 M × 16) Static RAM Document Number: 38-05447				
Rev.	**ECN No.**	**Orig. of Change**	**Submission date**	**Description of Change**
**	202600	AJU	01/23/2004	New data sheet.
*A	463674	NXR	See ECN	Converted from Advance Information to Preliminary Changed $V_{CC(max)}$ from 2.20 V to 2.25 V Removed 'L' bin and 35 ns speed bin from product offering Changed ball E3 from DNU to NC Removed redundant foot note on DNU Changed the $I_{SB2(typ)}$ value from 1.3 µA to 1.5 µA Changed the $I_{CC(max)}$ value from 40 mA to 25 mA Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics (t_R) from 100 µs to t_{RC} ns Changed the I_{CCDR} Value from 8 µA to 5 µA Changed t_{OHA}, t_{LZCE}, t_{LZBE}, and t_{LZWE} from 6 ns to 10 ns Changed t_{LZOE} from 3 ns to 5 ns Changed t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE}, t_{AW}, and t_{BW} from 40 ns to 35 ns Changed t_{PE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Updated 48 ball FBGA Package Information Updated the Ordering Information table
*B	469182	NSI	See ECN	Minor Change: Moved to external web
*C	619122	NXR	See ECN	Replaced 45 ns speed bin with 55 ns speed bin
*D	1130323	VKN	See ECN	Converted from preliminary to final Added footnote# 8 related I_{SB2} and I_{CCDR} Changed I_{SB1} and I_{SB2} spec from 10 µA to 12 µA Changed I_{CCDR} spec from 8 µA to 10 µA Added footnote# 13 related AC timing parameters Changed t_{WC} spec from 45 ns to 55 ns Changed t_{SCE}, t_{AW}, t_{PWE}, t_{BW} spec from 35 ns to 40 ns Changed t_{HZWE} spec from 18 ns to 20 ns
*E	1388287	VKN	See ECN	Added 48-Ball VFBGA (6 x 7 x 1mm) package Added footnote# 1 related to FBGA package Updated Ordering Information table
*F	1664843	VKN / AESA	See ECN	Added CY62167EV30LL-45BVI part in the Ordering Information table Added footnote# 5 related to CY62167EV30LL-45BVI part
*G	2675375	VKN / PYRS	03/17/2009	Added CY62167EV18LL-55BVI part in the Ordering Information table
*H	2904565	AJU	04/05/2010	Removed inactive part from the ordering information table.Updated package diagrams.
*I	2934396	VKN	06/03/10	Added footnote #24 related to chip enable Updated template
*J	3006301	RAME	08/12/2010	Included $\overline{BHE}$ and $\overline{BLE}$ in I_{SB1}, I_{SB2}, and I_{CCDR} test conditions to reflect Byte power down feature. Removed 48-Ball VFBGA (6 x 7 x 1 mm) package related information. Added Acronyms and Ordering code definition. Format updates to match template.
*K	3113908	PRAS	12/17/2010	Updated Figure 1 and Package Diagram.

Document History Page (continued)

Document Title: CY62167EV18 MoBL®, 16-Mbit (1 M × 16) Static RAM Document Number: 38-05447				
Rev.	**ECN No.**	**Orig. of Change**	**Submission date**	**Description of Change**
*L	3295175	RAME	06/29/2011	Updated Package Diagrams. Added Document Conventions. Removed reference to AN1064 SRAM system guidelines. Added I_{SB1} to footnotes 9 and 13. Modified Ordering Code Definitions. Updated Table of Contents.
*M	3421697	TAVA	10/25/2011	Removed Figure caption for AC Test Loads and Waveforms Updated Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, and Figure 9 Updated Package Diagrams
*N	4100342	VINI	08/21/2013	Updated Switching Characteristics: Added Note 16 and referred the same note in “Parameter” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. Removed spec 51-85183 (48-pin TSOP I Package). Updated in new template. Completing Sunset Review.
*O	4576406	VINI	01/16/2015	Added related documentation hyperlink in page 1. Added Note 21 in Switching Characteristics. Added note reference 21 in the Switching Characteristics table. Added Note 31 in Switching Waveforms. Added note reference 31 in Figure 8. Updated the Write Cycle number to 4 in Figure 9 title.

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