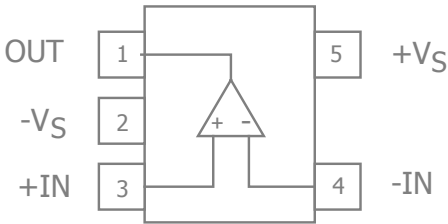




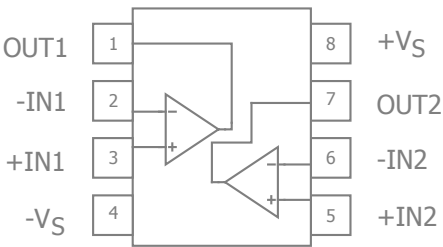
CLC1009 Pin Configuration



CLC1009 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	-VS	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	+VS	Positive supply

CLC2009 Pin Configuration



CLC2009 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	-VS	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	+VS	Positive supply



## Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	6	V
Input Voltage Range	$-V_S - 0.5V$	$+V_S + 0.5V$	V
Continuous Output Current	-30	30	mA

## Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			175	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead TSOT23		215		°C/W
8-Lead SOIC		100		°C/W

Notes:

Package thermal resistance ( $\theta_{JA}$ ), JEDEC standard, multi-layer test boards, still air.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.5		5.5	V



## Electrical Characteristics at +2.7V

$T_A = 25^\circ\text{C}$ ,  $V_S = +2.7\text{V}$ ,  $R_f = R_g = 2.5\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	$G = +1$ , $V_{OUT} = 0.05V_{pp}$ , $R_f = 0$		28		MHz
$BW_{SS}$	-3dB Bandwidth	$G = +2$ , $V_{OUT} < 0.2V_{pp}$		15		MHz
$BW_{LS}$	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		7		MHz
GBWP	Gain Bandwidth Product	$G = +11$ , $V_{OUT} = 0.2V_{pp}$		16		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time	$V_{OUT} = 0.2\text{V}$ step; (10% to 90%)		16		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 1\text{V}$ step		140		ns
OS	Overshoot	$V_{OUT} = 1\text{V}$ step		1		%
SR	Slew Rate	$2\text{V}$ step, $G = -1$		20		V/ $\mu\text{s}$
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 100kHz		-85		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 100kHz		-63		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 100kHz		62		dB
$e_n$	Input Voltage Noise	$> 10\text{kHz}$		23		nV/ $\sqrt{\text{Hz}}$
$X_{TALK}$	Crosstalk	$V_{OUT} = 0.2V_{pp}$ , 100kHz		98		dB
DC Performance						
$V_{IO}$	Input Offset Voltage			0.8		mV
$dV_{IO}$	Average Drift			11		$\mu\text{V}/^\circ\text{C}$
$I_b$	Input Bias Current			0.37		$\mu\text{A}$
$dI_b$	Average Drift			1		nA/ $^\circ\text{C}$
$I_{OS}$	Input Offset Current			8		nA
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	DC	56	60		dB
$A_{OL}$	Open-Loop Gain	$V_{OUT} = V_S / 2$		65		dB
$I_S$	Supply Current	per channel		185		$\mu\text{A}$
Input Characteristics						
$R_{IN}$	Input Resistance	Non-inverting		$> 10$		M $\Omega$
$C_{IN}$	Input Capacitance			1.4		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, $V_{CM} = 0\text{V}$ to $V_S - 1.5$		92		dB
Output Characteristics						
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$ to $V_S / 2$		0.08 to 2.6		V
		$R_L = 10\text{k}\Omega$ to $V_S / 2$		0.06 to 2.62		V
$I_{OUT}$	Output Current			$\pm 8$		mA
$I_{SC}$	Short Circuit Output Current			$\pm 12.5$		mA

### Notes:

1. 100% tested at  $25^\circ\text{C}$



## Electrical Characteristics at +5V

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = R_g = 2.5\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	$G = +1$ , $V_{OUT} = 0.05V_{pp}$ , $R_f = 0$		35		MHz
$BW_{SS}$	-3dB Bandwidth	$G = +2$ , $V_{OUT} < 0.2V_{pp}$		18		MHz
$BW_{LS}$	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		8		MHz
GBWP	Gain Bandwidth Product	$G = +11$ , $V_{OUT} = 0.2V_{pp}$		20		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time	$V_{OUT} = 0.2\text{V}$ step; (10% to 90%)		13		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 1\text{V}$ step		140		ns
OS	Overshoot	$V_{OUT} = 1\text{V}$ step		1		%
SR	Slew Rate	$2\text{V}$ step, $G = -1$		27		V/ $\mu\text{s}$
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 100kHz		-78		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 100kHz		-66		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 100kHz		65		dB
$e_n$	Input Voltage Noise	> 10kHz		21		nV/ $\sqrt{\text{Hz}}$
$X_{TALK}$	Crosstalk	$V_{OUT} = 0.2V_{pp}$ , 100kHz		98		dB
DC Performance						
$V_{IO}$	Input Offset Voltage <sup>(1)</sup>		-5	-1.5	5	mV
$dV_{IO}$	Average Drift			20		$\mu\text{V}/^\circ\text{C}$
$I_b$	Input Bias Current <sup>(1)</sup>		-1.3	0.37	1.3	$\mu\text{A}$
$dI_b$	Average Drift			1		nA/ $^\circ\text{C}$
$I_{OS}$	Input Offset Current <sup>(1)</sup>			7	130	nA
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	DC	56	60		dB
$A_{OL}$	Open-Loop Gain	$V_{OUT} = V_S / 2$	56	62		dB
$I_S$	Supply Current <sup>(1)</sup>	per channel		208	260	$\mu\text{A}$
Input Characteristics						
$R_{IN}$	Input Resistance	Non-inverting		>10		M $\Omega$
$C_{IN}$	Input Capacitance			1.2		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio <sup>(1)</sup>	DC, $V_{CM} = 0\text{V}$ to $V_S - 1.5$	65	95		dB
Output Characteristics						
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$ to $V_S / 2$ <sup>(1)</sup>	0.2 to 4.7	0.1 to 4.8		V
		$R_L = 10\text{k}\Omega$ to $V_S / 2$		0.08 to 4.88		V
$I_{OUT}$	Output Current			$\pm 8.5$		mA
$I_{SC}$	Short Circuit Output Current			$\pm 13$		mA

### Notes:

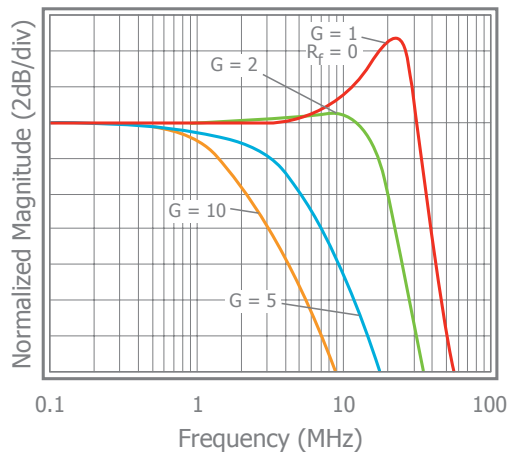
1. 100% tested at  $25^\circ\text{C}$



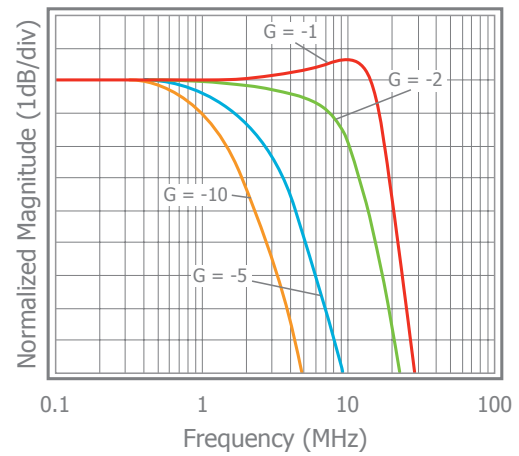
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = R_g = 2.5\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

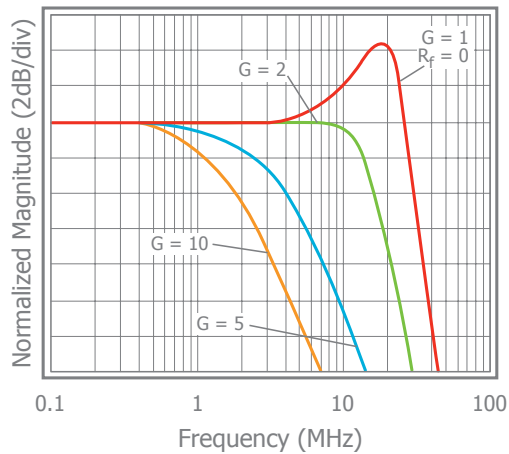
### Non-Inverting Frequency Response



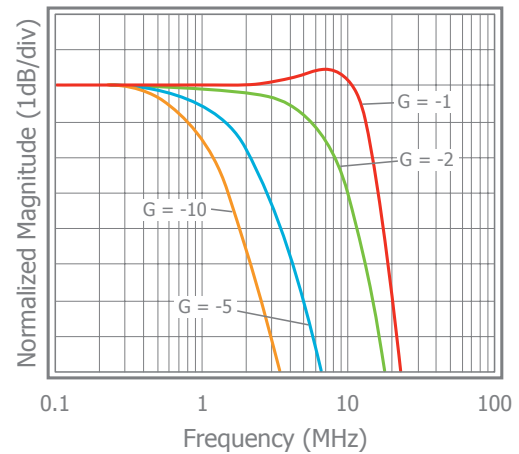
### Inverting Frequency Response



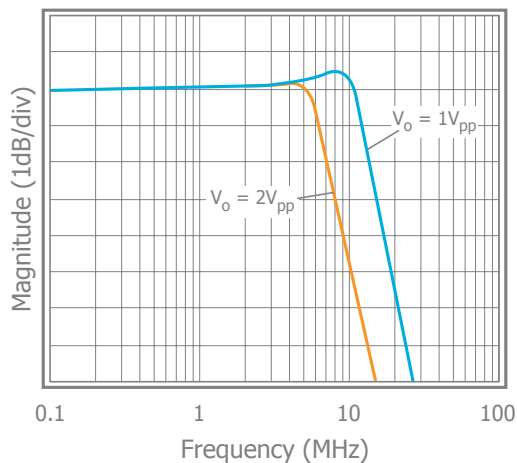
### Non-Inverting Frequency Response at $V_S = 2.7\text{V}$



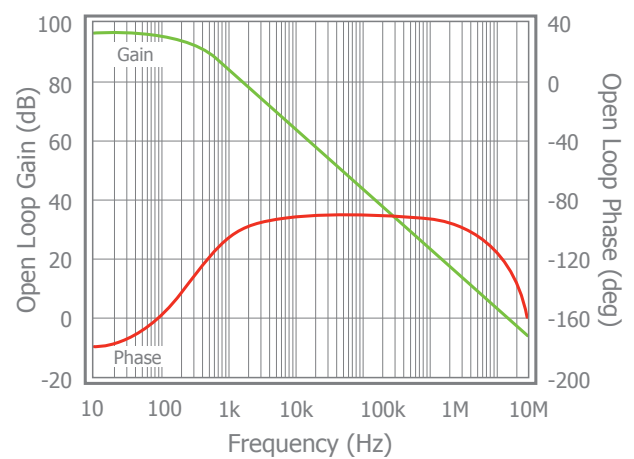
### Inverting Frequency Response at $V_S = 2.7\text{V}$



### Frequency Response vs. $V_{OUT}$



### Open Loop Gain & Phase vs. Frequency

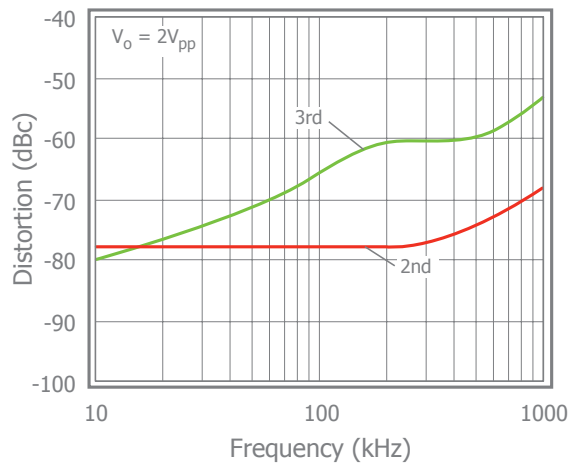




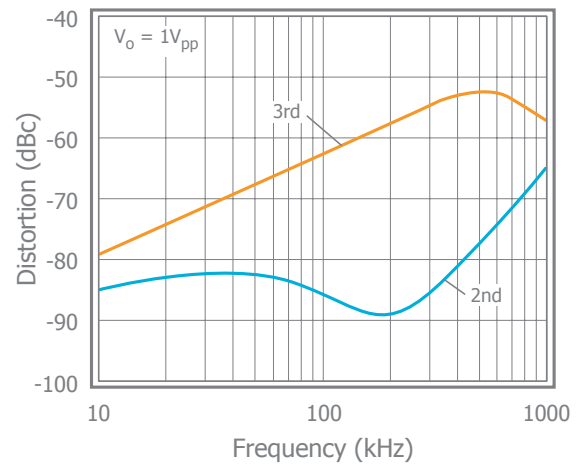
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = R_g = 2.5\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

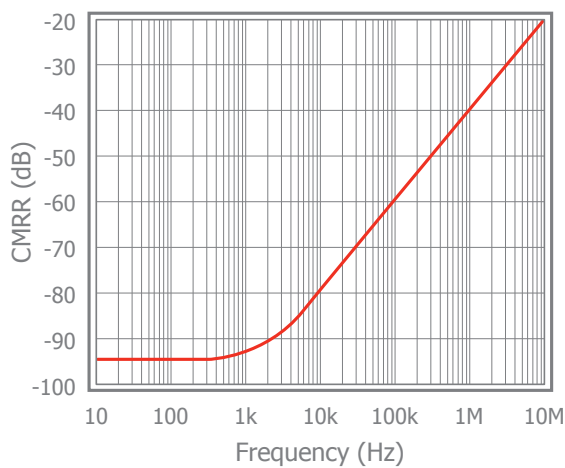
### 2nd & 3rd Harmonic Distortion



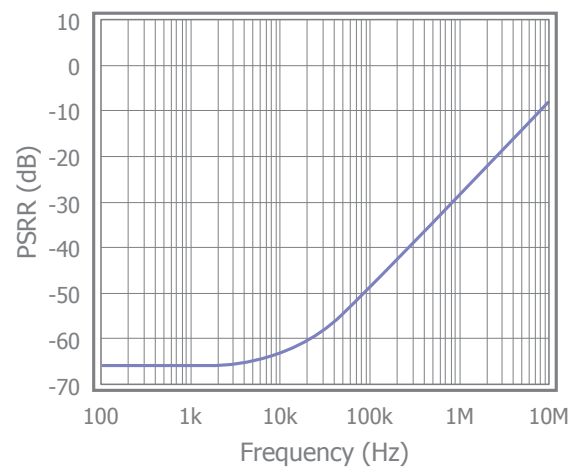
### 2nd & 3rd Harmonic Distortion at $V_S = 2.7\text{V}$



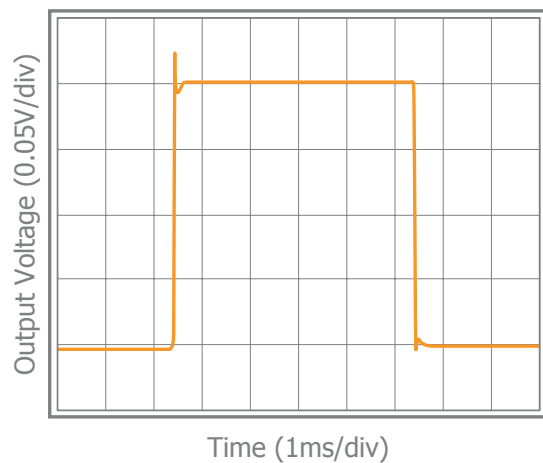
### CMRR



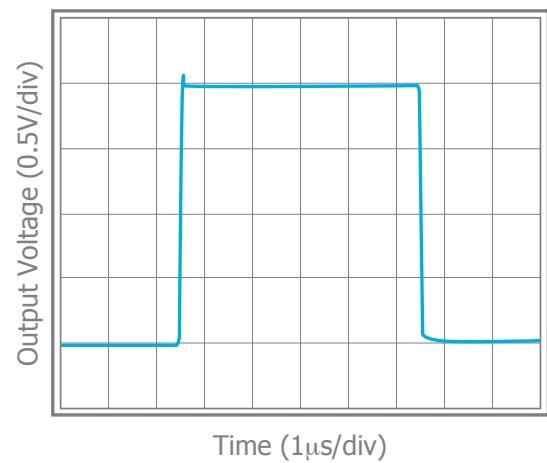
### PSRR



### Small Signal Pulse Response



### Large Signal Pulse Response

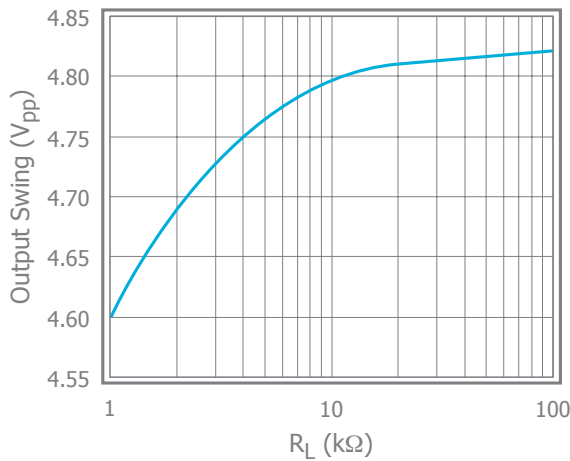




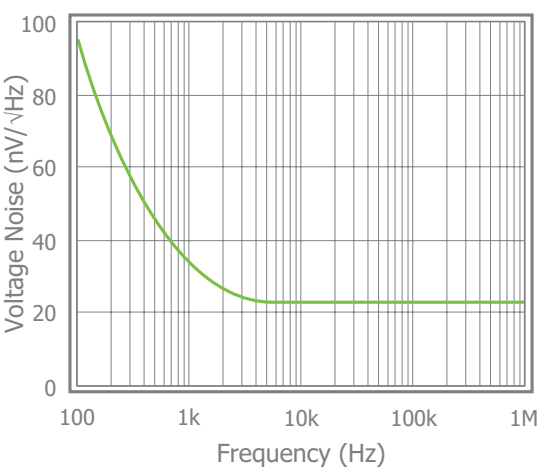
### Typical Performance Characteristics - Continued

$T_A = 25^{\circ}\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = R_g = 2.5\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

Output Swing vs.  $R_L$



Input Voltage Noise



Input Voltage Noise



## Application Information

### General Description

The CLC1009 family are a single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process. The CLC1009 offers 35MHz unity gain bandwidth, 27V/ $\mu$ s slew rate, and only 208 $\mu$ A supply current. It features a rail-to-rail output stage and is unity gain stable.

The design utilizes a patent pending topology that provides increased slew rate performance. The common mode input range extends to 300mV below ground and to 1.2V below  $V_s$ . Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

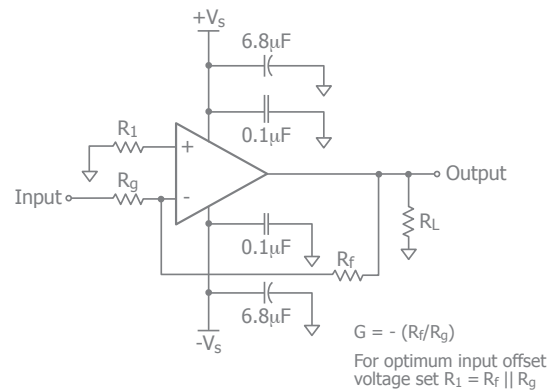


Figure 2. Typical Inverting Gain Circuit

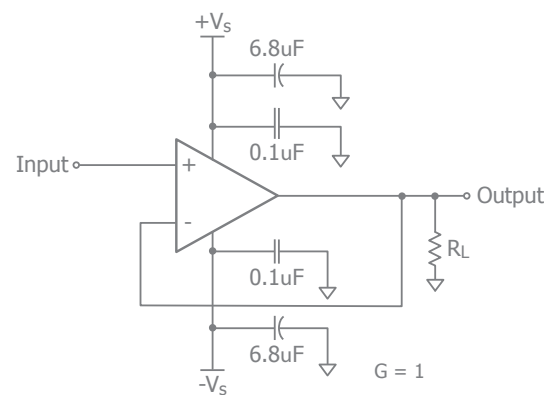


Figure 3. Unity Gain Circuit

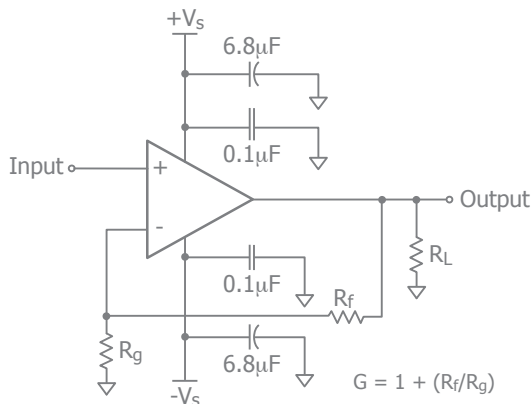


Figure 1. Typical Non-Inverting Gain Circuit

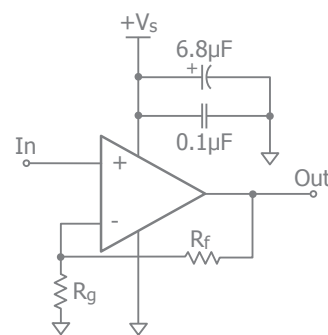


Figure 4. Single Supply Non-Inverting Gain Circuit





## Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value  $\Theta_{JA}$  ( $\Theta_{JA}$ ) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\Theta_{JA} \times P_D)$$

Where  $T_{\text{Ambient}}$  is the temperature of the working environment.

In order to determine  $P_D$ , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMS supply}}$$

$$V_{\text{supply}} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{LOAD}})_{\text{RMS}}^2) / R_{\text{load eff}}$$

The effective load resistor ( $R_{\text{load eff}}$ ) will need to include the effect of the feedback network. For instance,

$R_{\text{load eff}}$  in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here,  $P_D$  can be found from

$$P_D = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified  $I_S$  values along with known supply voltage,  $V_{\text{Supply}}$ . Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{LOAD}})_{\text{RMS}} = V_{\text{PEAK}} / \sqrt{2}$$

$$(I_{\text{LOAD}})_{\text{RMS}} = (V_{\text{LOAD}})_{\text{RMS}} / R_{\text{load eff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{DYNAMIC}} = (V_{S+} - V_{\text{LOAD}})_{\text{RMS}} \times (I_{\text{LOAD}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or  $V_{\text{supply}}/2$ .

The CLC1009 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

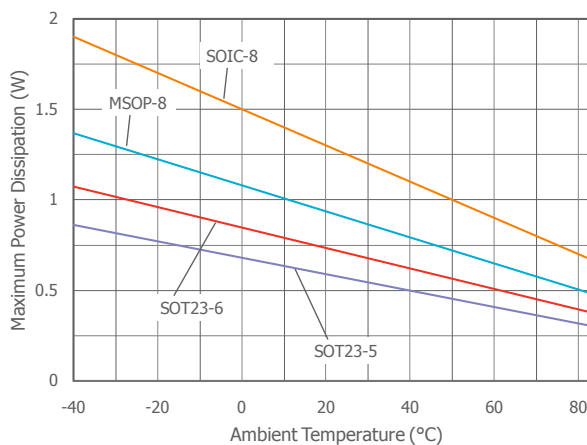


Figure 5. Maximum Power Derating

## Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance,  $R_S$ , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

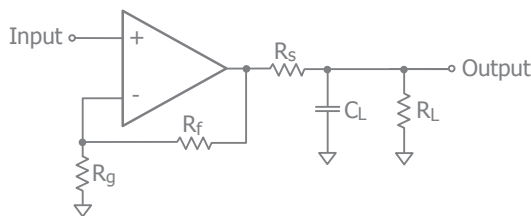


Figure 6. Addition of  $R_S$  for Driving Capacitive Loads

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC1009, CLC1019, and CLC2009 will typically recover in less than 20ns from an overdrive condition. Figure 7 shows the CLC1009 in an overdriven condition.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Resurgent Semiconductor has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1009 in TSOT23
CEB003	CLC1009 in SOIC
CEB006	CLC2009 in SOIC

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-14. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -Vs pin of the amplifier is not directly connected to the ground plane.

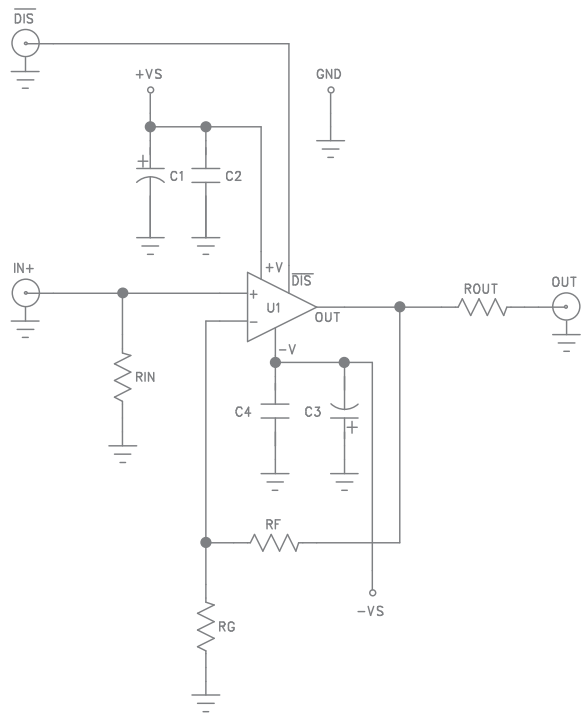


Figure 8. CEB002 & CEB003 Schematic

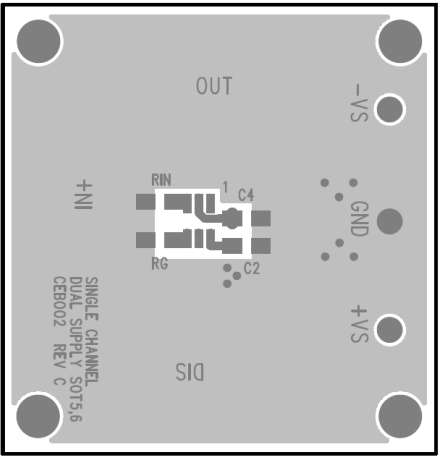


Figure 9. CEB002 Top View

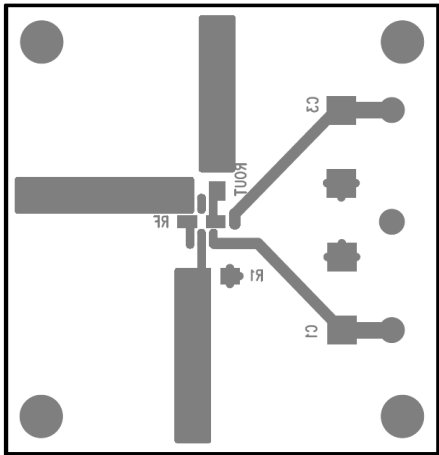


Figure 10. CEB002 Bottom View

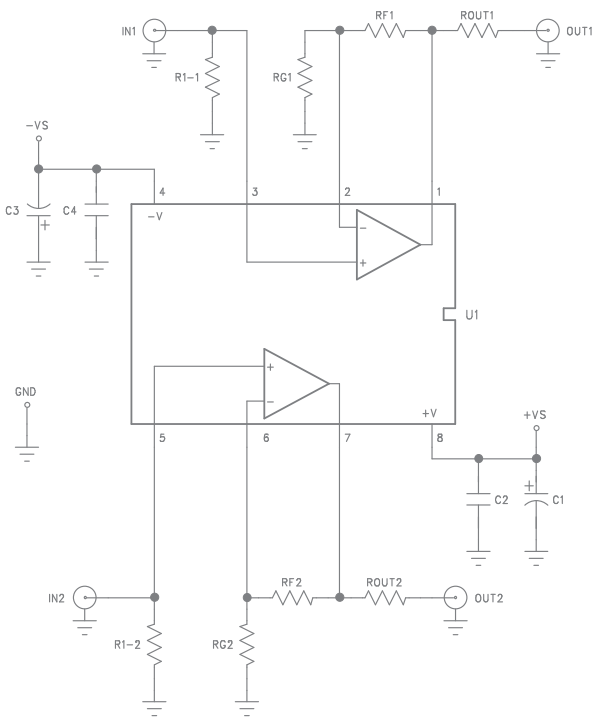


Figure 11. CEB006 & CEB010 Schematic

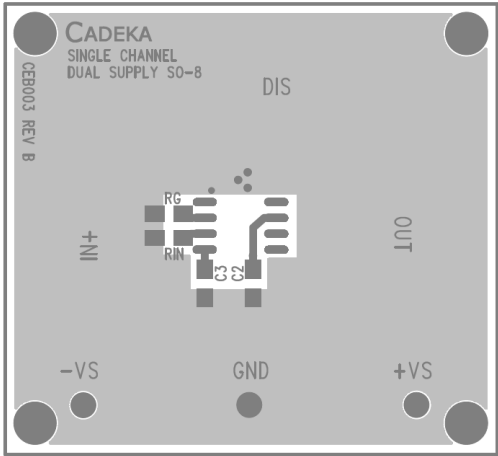


Figure 11. CEB003 Top View

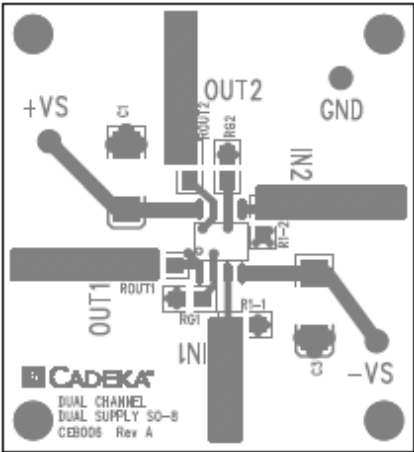


Figure 12. CEB006 Top View

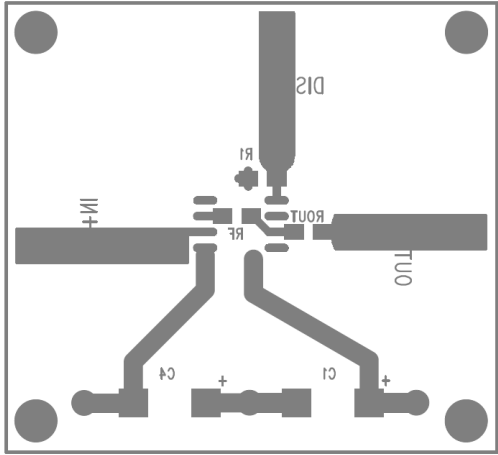


Figure 12. CEB003 Bottom View

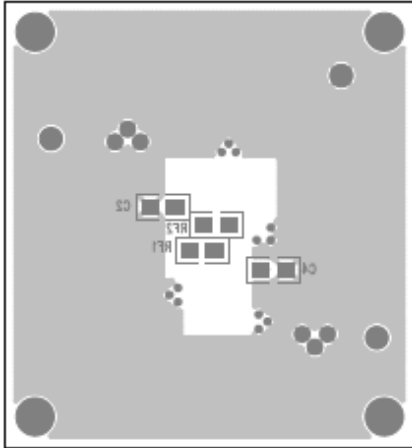
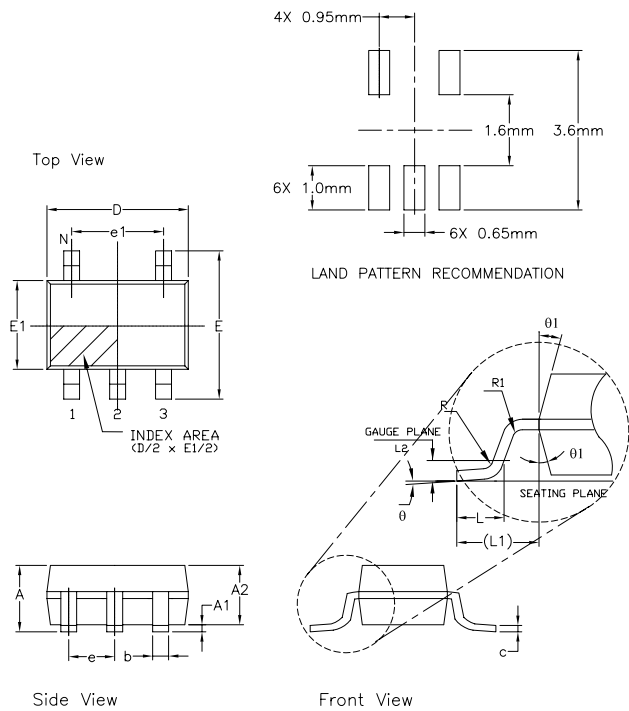


Figure 13. CEB006 Bottom View



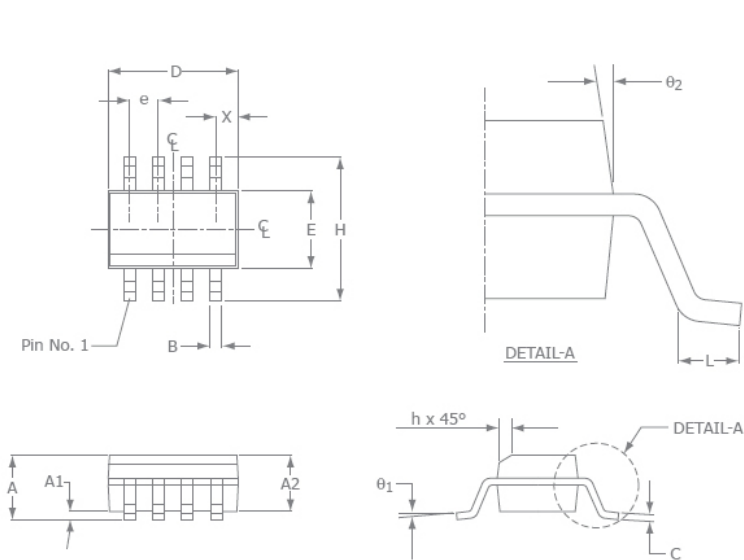
Mechanical Dimensions

TSOT-5 Package



5 Pin TSOT (OPTION 2)						
SYMBOLS	DIMENSION IN MM (Control Unit)			DIMENSION IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	0.80	0.030	—	0.031
A1	0.00	—	0.05	0.000	—	0.002
A2	0.70	0.75	0.78	0.028	0.030	0.031
b	0.35	—	0.50	0.012	—	0.020
c	0.10	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.37	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	5			5		

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ1	0°	8°
X	0.55 ref	
θ2	7° BSC	

- NOTE:**
1. All dimensions are in millimeters.
  2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
  3. Package surface finishing: VDI 24~27
  4. All dimension excluding mold flashes.
  5. The lead width, B to be determined at 0.1905mm from the lead tip.



## Revision History

Revision	Date	Description
1D.R	July 2018	Updated to Resurgent Semiconductor.

For Further Assistance:

[www.resurgentsemi.net](http://www.resurgentsemi.net)

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