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## REVISION HISTORY

### 7/2017—Rev. D to Rev. E

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### 8/2016—Rev. C to Rev. D

Changed ADuM330x to ADuM3300/ADuM3301 ... Throughout	
Changed 3 V to 3.3 V and 2.7 to 3.0 V .....	Throughout
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### 4/2014—Rev. B to Rev. C

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### 2/2012—Rev. A to Rev. B

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### 6/2007—Rev. 0 to Rev. A

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### 3/2006—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground.  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ ; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ .

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I <sub>DD1 (Q)</sub>		0.66	0.97	mA	
Output Supply Current per Channel, Quiescent	I <sub>DDO (Q)</sub>		0.39	0.55	mA	
ADuM3300, Total Supply Current, Four Channels <sup>1</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>		2.4	3.3	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>		1.1	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		7.0	8.1	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		2.7	3.6	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (90)</sub>		54	77	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (90)</sub>		15	31	mA	45 MHz logic signal freq.
ADuM3301, Total Supply Current, Four Channels <sup>1</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>		2.0	3.1	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>		1.6	2.3	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		5.5	6.9	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		3.9	5.4	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (90)</sub>		41	57	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (90)</sub>		28	41	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>ID</sub> , I <sub>E1</sub> , I <sub>E2</sub>	−10	+0.01	+10	μA	0 V ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> , V <sub>ID</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 V ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>	2.0			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>			0.8	V	
Logic High Output Voltages	V <sub>OAH</sub> , V <sub>OBH</sub> , V <sub>OCH</sub> , V <sub>ODH</sub>	(V <sub>DD1</sub> or V <sub>DD2</sub> ) − 0.1	5.0		V	I <sub>OX</sub> = −20 μA, V <sub>IX</sub> = V <sub>IXH</sub>
		(V <sub>DD1</sub> or V <sub>DD2</sub> ) − 0.4	4.8		V	I <sub>OX</sub> = −3.2 mA, V <sub>IX</sub> = V <sub>IXH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub> , V <sub>OCL</sub> , V <sub>ODL</sub>		0.0	0.1	V	I <sub>OX</sub> = 20 μA, V <sub>IX</sub> = V <sub>IXL</sub>
			0.04	0.1	V	I <sub>OX</sub> = 400 μA, V <sub>IX</sub> = V <sub>IXL</sub>
			0.2	0.4	V	I <sub>OX</sub> = 3.2 mA, V <sub>IX</sub> = V <sub>IXL</sub>
SWITCHING SPECIFICATIONS						
ADuM3300ARWZ/ADuM3301ARWZ						
Minimum Pulse Width <sup>2</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	65	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> − t <sub>PHL</sub>   <sup>4</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>6</sup>	t <sub>PSKCD/OD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>ADuM3300BRWZ/ADuM3301BRWZ</b>						
Minimum Pulse Width <sup>2</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	32	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>   <sup>4</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			15	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>6</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>ADuM3300CRWZ/ADuM3301CRWZ</b>						
Minimum Pulse Width <sup>2</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	18	27	32	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>   <sup>4</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			10	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>6</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>For All Models</b>						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance-to-High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		2.5		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output <sup>7</sup>	CM <sub>H</sub>	25	35		kV/μs	V <sub>IX</sub> = V <sub>DD1</sub> or V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>7</sup>	CM <sub>L</sub>	25	35		kV/μs	V <sub>IX</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>		1.2		Mbps	
Input Dynamic Supply Current per Channel <sup>8</sup>	I <sub>DDI</sub> (D)		0.20		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>8</sup>	I <sub>DDO</sub> (D)		0.05		mA/Mbps	

<sup>1</sup> The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V<sub>DD1</sub> and V<sub>DD2</sub> supply currents as a function of data rate for ADuM3300/ADuM3301 channel configurations.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>3</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>4</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>IX</sub> signal to the 50% level of the falling edge of the V<sub>OX</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>IX</sub> signal to the 50% level of the rising edge of the V<sub>OX</sub> signal.

<sup>5</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>6</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>7</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>8</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

**ELECTRICAL CHARACTERISTICS—3.3 V OPERATION**

All voltages are relative to their respective ground.  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ ; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ .

**Table 2.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$		0.37	0.57	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$		0.25	0.37	mA	
<b>ADuM3300, Total Supply Current, Four Channels<sup>1</sup></b>						
<b>DC to 2 Mbps</b>						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$		1.4	1.9	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$		3.8	5.3	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$		1.5	2.1	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(90)}$		28	41	mA	45 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(90)}$		8.2	11	mA	45 MHz logic signal freq.
<b>ADuM3301, Total Supply Current, Four Channels<sup>1</sup></b>						
<b>DC to 2 Mbps</b>						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$		1.1	1.6	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$		0.9	1.4	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$		3.0	4.1	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$		2.2	2.9	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(90)}$		22	31	mA	45 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(90)}$		15	21	mA	45 MHz logic signal freq.
<b>For All Models</b>						
Input Currents	$I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or $V_{DD2}$ , $0\text{ V} \leq V_{E1}, V_{E2} \leq V_{DD1}$ or $V_{DD2}$
Logic High Input Threshold	$V_{IH}, V_{EH}$	1.6			V	
Logic Low Input Threshold	$V_{IL}, V_{EL}$			0.4	V	
Logic High Output Voltages	$V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}$	$(V_{DD1}$ or $V_{DD2}) - 0.1$	3.0		V	$I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$
		$(V_{DD1}$ or $V_{DD2}) - 0.4$	2.8		V	$I_{OX} = -3.2\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	$V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}$		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.04	0.1	V	$I_{OX} = 400\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 3.2\text{ mA}, V_{IX} = V_{IXL}$
<b>SWITCHING SPECIFICATIONS</b>						
<b>ADuM3300ARWZ/ADuM3301ARWZ</b>						
Minimum Pulse Width <sup>2</sup>	PW			1000	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>3</sup>		1			Mbps	$C_L = 15\text{ pF}$ , CMOS signal levels
Propagation Delay <sup>4</sup>	$t_{PHL}, t_{PLH}$	50	75	100	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>4</sup>	PWD			40	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>5</sup>	$t_{PSK}$			50	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching <sup>6</sup>	$t_{PSKCD/OD}$			50	ns	$C_L = 15\text{ pF}$ , CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>ADuM3300BRWZ/ADuM3301BRWZ</b>						
Minimum Pulse Width <sup>2</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	38	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>   <sup>4</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			22	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>6</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>ADuM3300CRWZ/ADuM3301CRWZ</b>						
Minimum Pulse Width <sup>2</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	34	45	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>   <sup>4</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			16	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>6</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>For All Models</b>						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance-to-High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		3		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output <sup>7</sup>	CM <sub>H</sub>	25	35		kV/μs	V <sub>ix</sub> = V <sub>DD1</sub> or V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>7</sup>	CM <sub>L</sub>	25	35		kV/μs	V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>		1.1		Mbps	
Input Dynamic Supply Current per Channel <sup>8</sup>	I <sub>DDI</sub> (D)		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>8</sup>	I <sub>DDO</sub> (D)		0.03		mA/Mbps	

<sup>1</sup> The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V<sub>DD1</sub> and V<sub>DD2</sub> supply currents as a function of data rate for ADuM3300/ADuM3301 channel configurations.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>3</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>4</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>ix</sub> signal to the 50% level of the falling edge of the V<sub>Ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>ix</sub> signal to the 50% level of the rising edge of the V<sub>Ox</sub> signal.

<sup>5</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>6</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>7</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>8</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OR 3.3 V/5 V OPERATION**

All voltages are relative to their respective ground. 5 V/3.3 V operation:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ . 3.3 V/5 V operation:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD1} = 3.3\text{ V}$ ,  $V_{DD2} = 5\text{ V}$  or  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ .

**Table 3.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$					
5 V/3 V Operation			0.66	0.97	mA	
3 V/5 V Operation			0.37	0.57	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.25	0.37	mA	
3 V/5 V Operation			0.39	0.55	mA	
<b>ADuM3300, Total Supply Current, Four Channels<sup>1</sup></b>						
<b>DC to 2 Mbps</b>						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			2.4	3.3	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.4	1.9	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.1	2.1	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			7.0	8.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.8	5.3	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.5	2.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.7	3.6	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(90)}$					
5 V/3 V Operation			54	77	mA	45 MHz logic signal freq.
3 V/5 V Operation			28	41	mA	45 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(90)}$					
5 V/3 V Operation			8.2	11	mA	45 MHz logic signal freq.
3 V/5 V Operation			15	31	mA	45 MHz logic signal freq.
<b>ADuM3301, Total Supply Current, Four Channels<sup>1</sup></b>						
<b>DC to 2 Mbps</b>						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			2.0	3.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.1	1.6	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.6	2.3	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			5.5	6.9	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	4.1	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			2.2	2.9	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.9	5.4	mA	5 MHz logic signal freq.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1</sub> (90)					
5 V/3 V Operation			41	57	mA	45 MHz logic signal freq.
3 V/5 V Operation			22	31	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2</sub> (90)					
5 V/3 V Operation			15	21	mA	45 MHz logic signal freq.
3 V/5 V Operation			28	41	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>ID</sub> , I <sub>E1</sub> , I <sub>E2</sub>	−10	+0.01	+10	μA	0 V ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> , V <sub>ID</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 V ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V <sub>OA</sub> H, V <sub>OB</sub> H, V <sub>OC</sub> H, V <sub>OD</sub> H	(V <sub>DD1</sub> or V <sub>DD2</sub> ) − 0.1	(V <sub>DD1</sub> or V <sub>DD2</sub> )		V	I <sub>OX</sub> = −20 μA, V <sub>IX</sub> = V <sub>IXH</sub>
		(V <sub>DD1</sub> or V <sub>DD2</sub> ) − 0.4	(V <sub>DD1</sub> or V <sub>DD2</sub> ) − 0.2		V	I <sub>OX</sub> = −3.2 mA, V <sub>IX</sub> = V <sub>IXH</sub>
Logic Low Output Voltages	V <sub>OA</sub> L, V <sub>OB</sub> L, V <sub>OC</sub> L, V <sub>OD</sub> L		0.0	0.1	V	I <sub>OX</sub> = 20 μA, V <sub>IX</sub> = V <sub>IXL</sub>
			0.04	0.1	V	I <sub>OX</sub> = 400 μA, V <sub>IX</sub> = V <sub>IXL</sub>
			0.2	0.4	V	I <sub>OX</sub> = 3.2 mA, V <sub>IX</sub> = V <sub>IXL</sub>
SWITCHING SPECIFICATIONS						
ADuM3300ARWZ/ADuM3301ARWZ						
Minimum Pulse Width <sup>2</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	70	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> − t <sub>PHL</sub>   <sup>4</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>6</sup>	t <sub>PSKCD</sub> /OD			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
ADuM3300BRWZ/ADuM3301BRWZ						
Minimum Pulse Width <sup>2</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	15	35	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> − t <sub>PHL</sub>   <sup>4</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			22	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>6</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
ADuM3300CRWZ/ADuM3301CRWZ						
Minimum Pulse Width <sup>2</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>3</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	30	40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> − t <sub>PHL</sub>   <sup>4</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>5</sup>	t <sub>PSK</sub>			14	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>6</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels



Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
For All Models						
Output Disable Propagation Delay (High/Low-to-High Impedance)	$t_{PHZ}, t_{PLH}$		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Enable Propagation Delay (High Impedance-to-High/Low)	$t_{PZH}, t_{PZL}$		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Rise/Fall Time (10% to 90%)	$t_R/t_F$					$C_L = 15 \text{ pF}$ , CMOS signal levels
5 V/3.3 V Operation			3.0		ns	
3.3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output <sup>7</sup>	$ CM_H $	25	35		kV/ $\mu\text{s}$	$V_{IX} = V_{DD1}$ or $V_{DD2}$ , $V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>7</sup>	$ CM_L $	25	35		kV/ $\mu\text{s}$	$V_{IX} = 0 \text{ V}$ , $V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$					
5 V/3.3 V Operation			1.2		Mbps	
3.3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel <sup>8</sup>	$I_{DDI(D)}$					
5 V/3.3 V Operation			0.20		mA/Mbps	
3.3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>8</sup>	$I_{DDO(D)}$					
5 V/3.3 V Operation			0.05		mA/Mbps	
3.3 V/5 V Operation			0.03		mA/Mbps	

<sup>1</sup> The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total  $V_{DD1}$  and  $V_{DD2}$  supply currents as a function of data rate for ADuM3300/ADuM3301 channel configurations.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>3</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>4</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{IX}$  signal to the 50% level of the falling edge of the  $V_{OX}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{IX}$  signal to the 50% level of the rising edge of the  $V_{OX}$  signal.

<sup>5</sup>  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>6</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>7</sup>  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8 \text{ V}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>8</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.



## PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	f = 1 MHz
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>		2.2		pF	
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 1	θ <sub>JCI</sub>		33		°C/W	
IC Junction-to-Case Thermal Resistance, Side 2	θ <sub>JCO</sub>		28		°C/W	

<sup>1</sup> The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM3300/ADuM3301 is approved by the organizations listed in Table 5. See Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

UL	CSA	VDE	CQC
Recognized under UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 <sup>2</sup>	Approved under CQC11-471543-2015
Single protection, 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak	Basic insulation per GB4943.1-2011, 760 V rms (1075 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 meters Reinforced insulation per GB4943.1-2011, 380 V rms (537 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 meters
File E214100	File 205078	File 2471900-4880-0001	File CQC16001160843

<sup>1</sup> In accordance with UL1577, the ADuM3300/ADuM3301 are proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, the ADuM3300/ADuM3301 are proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (\*) marking branded on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (\*) marking on the package denotes DIN V VDE V 0884-10 approval for 560 V peak working voltage.

**Table 7.**

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage $\leq 150$ V rms For Rated Mains Voltage $\leq 300$ V rms For Rated Mains Voltage $\leq 400$ V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		$V_{IORM}$	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$ , 100% production test, $t_m = 1$ sec, partial discharge $< 5$ pC	$V_{PR}$	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, partial discharge $< 5$ pC	$V_{PR}$		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, partial discharge $< 5$ pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ seconds	$V_{TR}$	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		$T_S$	150	°C
Side 1 Current		$I_{S1}$	265	mA
Side 2 Current		$I_{S2}$	335	mA
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	$> 10^9$	$\Omega$

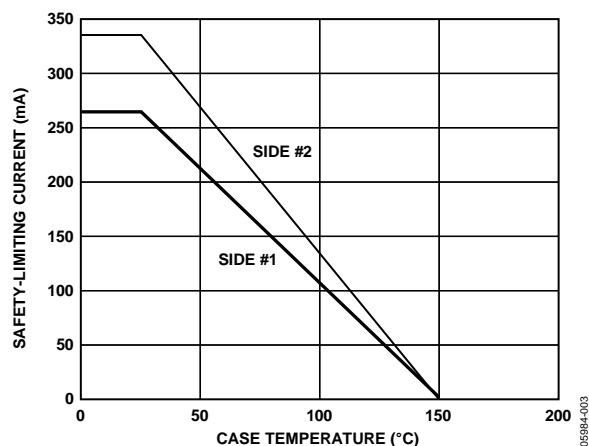


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

**RECOMMENDED OPERATING CONDITIONS****Table 8.**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	$T_A$	-40	+105	°C
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	3.0	5.5	V
Input Signal Rise and Fall Times			1.0	ms

<sup>1</sup> All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T <sub>ST</sub>	−65	+150	°C
Ambient Operating Temperature	T <sub>A</sub>	−40	+105	°C
Supply Voltages <sup>1</sup>	V <sub>DD1</sub> , V <sub>DD2</sub>	−0.5	+7.0	V
Input Voltage <sup>1,2</sup>	V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> , V <sub>ID</sub> , V <sub>E1</sub> , V <sub>E2</sub>	−0.5	V <sub>DDI</sub> + 0.5	V
Output Voltage <sup>1,2</sup>	V <sub>OA</sub> , V <sub>OB</sub> , V <sub>OC</sub> , V <sub>OD</sub>	−0.5	V <sub>DDO</sub> + 0.5	V
Average Output Current per Pin <sup>3</sup>				
Side 1	I <sub>O1</sub>	−23	+23	mA
Side 2	I <sub>O2</sub>	−30	+30	mA
Common-Mode Transients <sup>4</sup>	CM <sub>H</sub> , CM <sub>L</sub>	−100	+100	kV/μs

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> V<sub>DDI</sub> and V<sub>DDO</sub> refer to the supply voltages on the input and output sides of a given channel, respectively.

<sup>3</sup> See Figure 3 for maximum rated current values for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage<sup>1</sup>

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

<sup>1</sup> Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

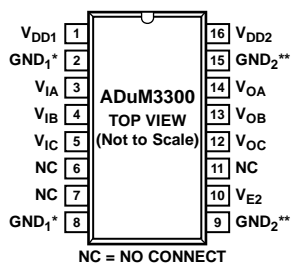
Table 11. Truth Table (Positive Logic)

V <sub>IX</sub> Input <sup>1</sup>	V <sub>EX</sub> Input <sup>2</sup>	V <sub>DDI</sub> State <sup>1</sup>	V <sub>DDO</sub> State <sup>1</sup>	V <sub>OX</sub> Output <sup>1</sup>	Notes
H	H or NC	Powered	Powered	H	Outputs return to the input state within 1 μs of V <sub>DDI</sub> power restoration
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	
X	L	Unpowered	Powered	Z	Outputs return to the input state within 1 μs of V <sub>DDO</sub> power restoration if V <sub>EX</sub> state is H or NC Outputs return to high impedance state within 8 ns of V <sub>DDO</sub> power restoration if V <sub>EX</sub> state is L
X	X	Powered	Unpowered	Indeterminate	

<sup>1</sup> V<sub>IX</sub> and V<sub>OX</sub> refer to the input and output signals of a given channel (A, B, or C). V<sub>EX</sub> refers to the output enable signal on the same side as the V<sub>OX</sub> outputs. V<sub>DDI</sub> and V<sub>DDO</sub> refer to the supply voltages on the input and output sides of the given channel, respectively.

<sup>2</sup> In noisy environments, connecting V<sub>EX</sub> to an external logic high or low is recommended.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



\*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND<sub>1</sub> IS RECOMMENDED.

\*\*PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND<sub>2</sub> IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3301 AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

05984-004

Figure 4. ADuM3300 Pin Configuration

Table 12. ADuM3300 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground Reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>IC</sub>	Logic Input C.
6, 7, 11	NC	No Connect.
9, 15	GND <sub>2</sub>	Ground 2. Ground Reference for Isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
12	V <sub>OC</sub>	Logic Output C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.

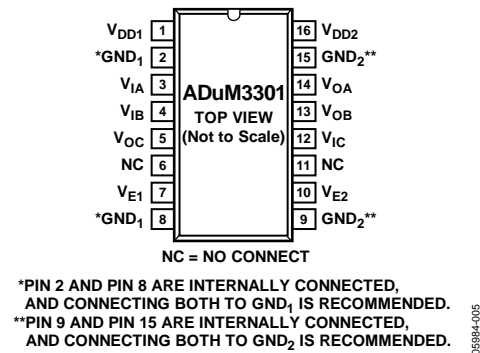


Figure 5. ADuM3301 Pin Configuration

Table 13. ADuM3301 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>OC</sub>	Logic Output C.
6, 11	NC	No Connect.
7	V <sub>E1</sub>	Output Enable 1. Active high logic input. V <sub>OC</sub> output is enabled when V <sub>E1</sub> is high or disconnected. V <sub>OC</sub> is disabled when V <sub>E1</sub> is low. In noisy environments, connecting V <sub>E1</sub> to an external logic high or low is recommended.
9, 15	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> and V <sub>OB</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> and V <sub>OB</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
12	V <sub>IC</sub>	Logic Input C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.

## TYPICAL PERFORMANCE CHARACTERISTICS

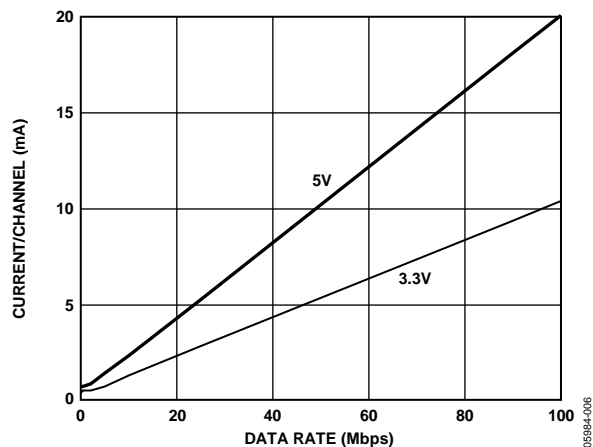


Figure 6. Typical Input Supply Current per Channel vs. Data Rate (No Load)

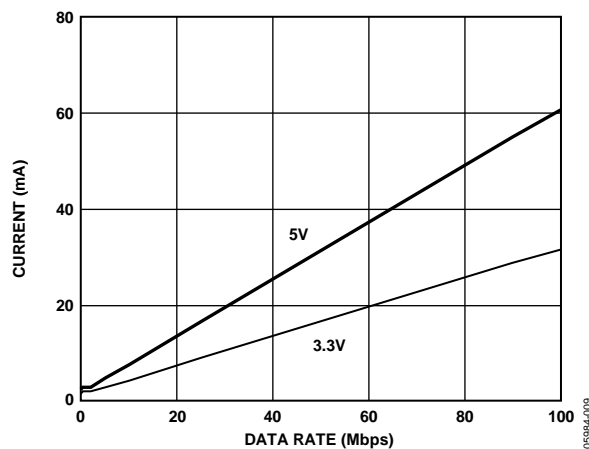
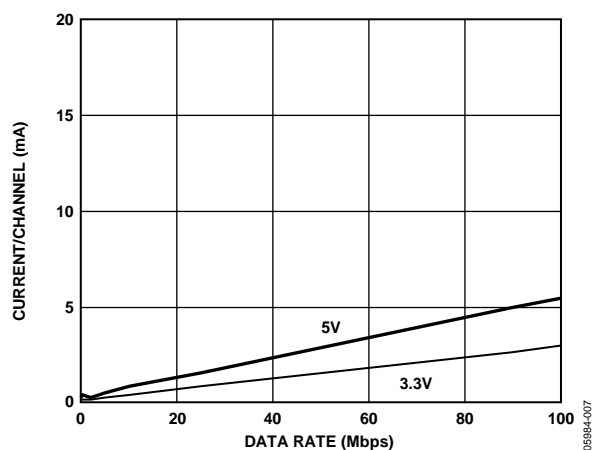
Figure 9. Typical ADuM3300  $V_{DD1}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 7. Typical Output Supply Current per Channel vs. Data Rate (No Load)

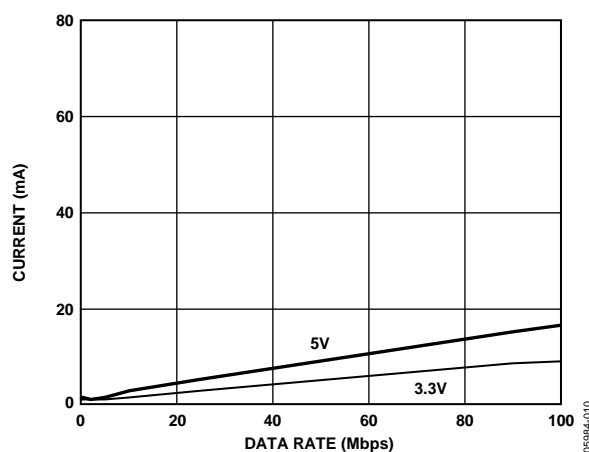
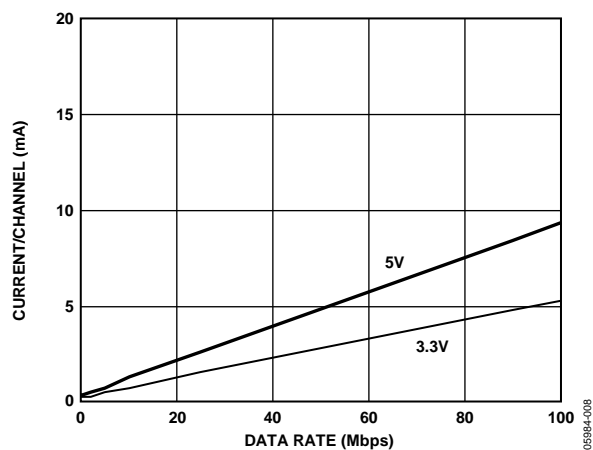
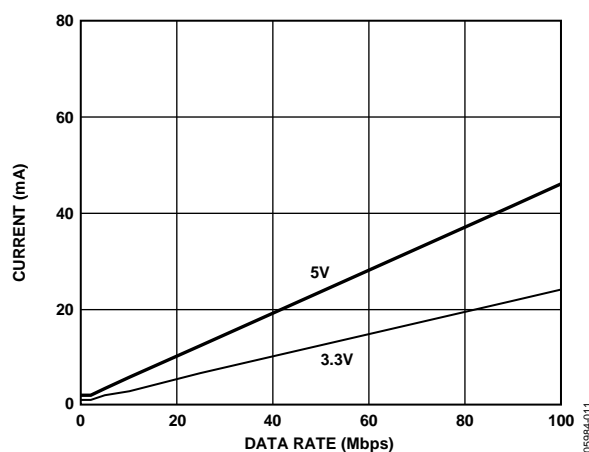
Figure 10. Typical ADuM3300  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 8. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load)

Figure 11. Typical ADuM3301  $V_{DD1}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation

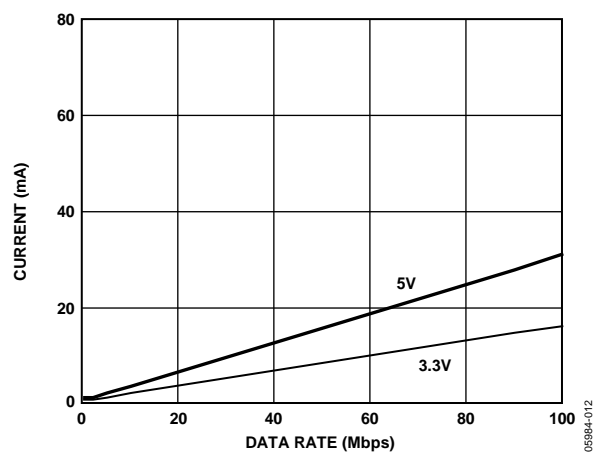


Figure 12. Typical ADuM3301  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation

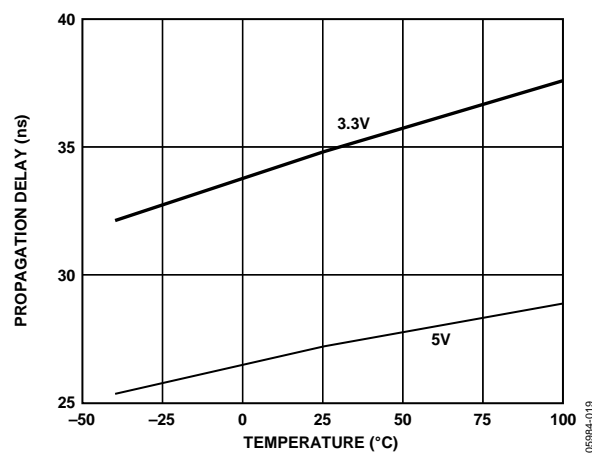


Figure 13. Propagation Delay vs. Temperature, C Grade



## APPLICATION INFORMATION

### PC BOARD LAYOUT

The ADuM3300/ADuM3301 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 14). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for  $V_{DD1}$  and between Pin 15 and Pin 16 for  $V_{DD2}$ . The capacitor value should be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should be considered unless the ground pair on each package side is connected close to the package.

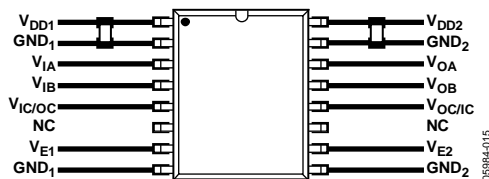


Figure 14. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's absolute maximum ratings, thereby leading to latch-up or permanent damage.

See the [AN-1109 Application Note](#) for board layout guidelines.

### SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM3300/ADuM3301 incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM3300/ADuM3301 improve system-level ESD reliability, they are no substitute for a robust system-level design. See [Application Note AN-793 ESD/Latch-Up Considerations with iCoupler Isolation Products](#) for detailed recommendations on board layout and system-level design.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high.

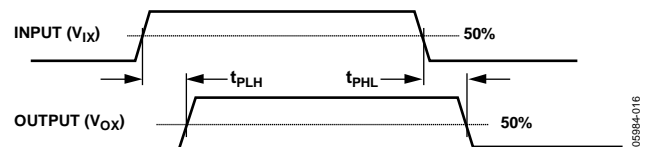


Figure 15. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM3300/ADuM3301 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM3300/ADuM3301 components operating under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow ( $\sim 1$  ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than  $\sim 1$   $\mu\text{s}$ , a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5  $\mu\text{s}$ , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 11) by the watchdog timer circuit.

The limitation on the ADuM3300/ADuM3301 magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3300/ADuM3301 are examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is magnetic flux density (gauss).

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

$N$  is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM330x and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 16.

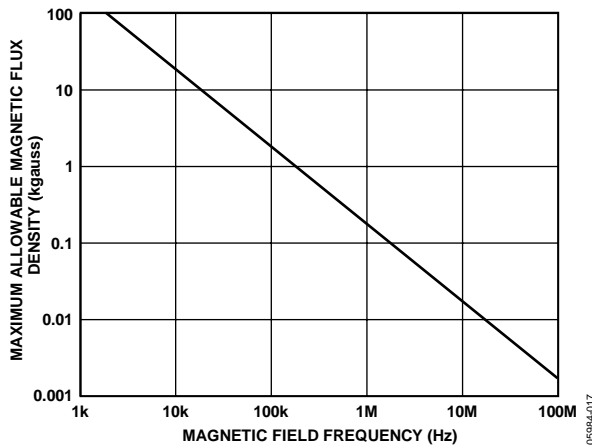


Figure 16. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM3300/ADuM3301 transformers. Figure 17 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM3300/ADuM3301 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component (see Figure 17). For the 1 MHz example noted, a 0.5 kA current would have to be placed 5 mm away from the ADuM3300/ADuM3301 to affect the component's operation.

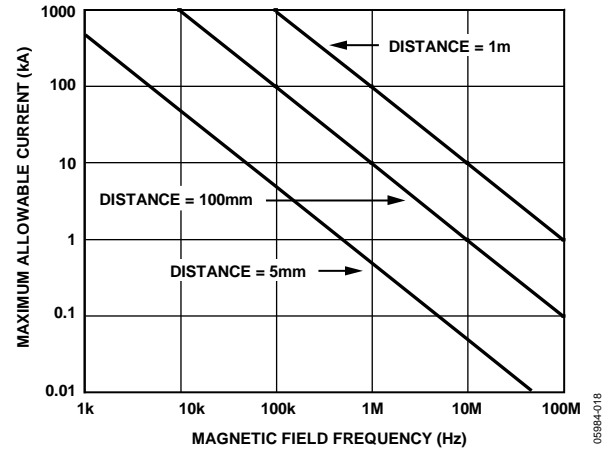


Figure 17. Maximum Allowable Current for Various Current-to-ADuM3300/ADuM3301 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM3300/ADuM3301 isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5 f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$C_L$  is the output load capacitance (pF).

$V_{DDO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

$f_r$  is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

To calculate the total  $I_{DD1}$  and  $I_{DD2}$  supply current, the supply currents for each input and output channel corresponding to  $V_{DD1}$  and  $V_{DD2}$  are calculated and totaled. Figure 6 provides per-channel input supply current as a function of data rate. Figure 7 and Figure 8 provide per-channel output supply current as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 12 provide total  $V_{DD1}$  and  $V_{DD2}$  supply current as a function of data rate for ADuM3300/ADuM3301 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices executes an extensive set of evaluations to determine the lifetime of the insulation structure within the [ADuM3300/ADuM3301](#).

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 10 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life.

The insulation lifetime of the [ADuM3300/ADuM3301](#) depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 18, Figure 19, and Figure 20 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 19 or Figure 20 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 10.

Note that the voltage presented in Figure 19 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

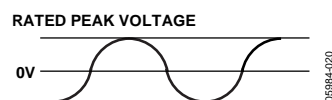


Figure 18. Bipolar AC Waveform

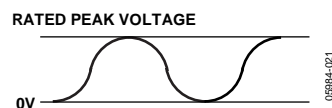


Figure 19. Unipolar AC Waveform

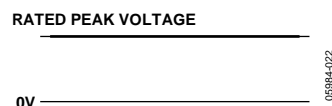
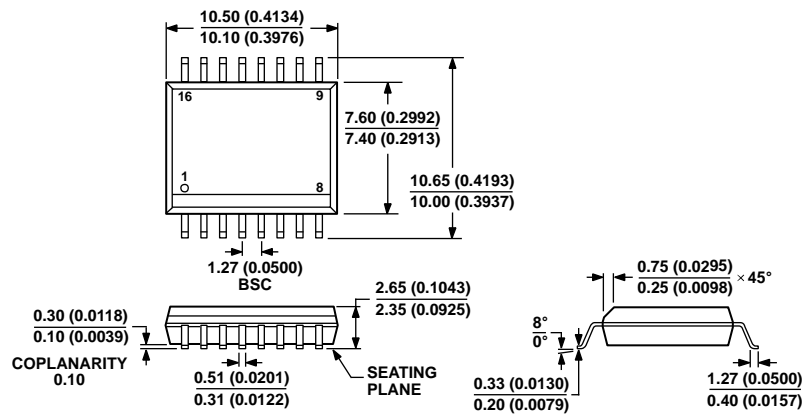


Figure 20. DC Waveform

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 21. 16-Lead Standard Small Outline Package [SOIC\_W]  
Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model <sup>1, 2</sup>	Temperature Range (°C)	Number of Inputs, V <sub>DD1</sub> Side	Number of Inputs, V <sub>DD2</sub> Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Package Option <sup>3</sup>
ADuM3300ARWZ	−40 to +105	3	0	1	100	40	RW-16
ADuM3300ARWZ-RL	−40 to +105	3	0	1	100	40	RW-16
ADuM3300BRWZ	−40 to +105	3	0	10	50	3	RW-16
ADuM3300BRWZ-RL	−40 to +105	3	0	10	50	3	RW-16
ADuM3300CRWZ	−40 to +105	3	0	90	32	2	RW-16
ADuM3300CRWZ-RL	−40 to +105	3	0	90	32	2	RW-16
ADuM3301ARWZ	−40 to +105	2	1	1	100	40	RW-16
ADuM3301ARWZ-RL	−40 to +105	2	1	1	100	40	RW-16
ADuM3301BRWZ	−40 to +105	2	1	10	50	3	RW-16
ADuM3301BRWZ-RL	−40 to +105	2	1	10	50	3	RW-16
ADuM3301CRWZ	−40 to +105	2	1	90	32	2	RW-16
ADuM3301CRWZ-RL	−40 to +105	2	1	90	32	2	RW-16

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> Tape and reel are available. The addition of an “-RL” suffix designates a 13” (1,000 units) tape and reel option.

<sup>3</sup> RW-16 = 16-lead wide body SOIC.