AD8143* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- AD8143 Evaluation Board

Documentation

Data Sheet

- AD8143: High-Speed, Triple Differential Receiver with Comparators Data Sheet

User Guides

- UG-862: Evaluation Board for the AD8143/AD8145 High Speed, Triple Differential Receivers with Comparators

Reference Materials

Product Selection Guide

- Amplifiers for Video Distribution
- High Speed Amplifiers Selection Table

Design Resources

- AD8143 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD8143 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

Downloaded from Arrow.com.

TABLE OF CONTENTS

REVISION HISTORY

4/16—Rev. 0 to Rev. A

Changes to Figure 3 and Table 6 ... 10
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

10/05—Revision 0: Initial Version

Downloaded from Arrow.com.

SPECIFICATIONS

V_S = ±12 V, T_A = 25°C, REF = 0 V, R_L = 150 Ω, C_L = 2 pF, G = 1, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		260		MHz
	V_{OUT} = 2 V p-p		160		MHz
Bandwidth for 0.1dB Flatness	V_{OUT} = 0.2 V p-p		45		MHz
Slew Rate	V_{OUT} = 2 V p-p, R_L = 1 kΩ		1000		V/µs
Settling Time	V_{OUT} = 2 V p-p, 1%		8		ns
	V_{OUT} = 2 V p-p, 0.1%		31		ns
Output Overdrive Recovery			50		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 2 V p-p, 1 MHz		−70		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 1 MHz		−80		dBc
Crosstalk	V_{OUT} = 1 V p-p, 10 MHz		−70		dB
Input Voltage Noise (RTI)	f ≥ 10 kHz		14		nV/√Hz
Differential Gain Error	NTSC, 200 IRE, R_L ≥ 150 Ω		0.03		%
Differential Phase Error	NTSC, 200 IRE, R_L ≥ 150 Ω		0.06		Degrees
INPUT CHARACTERISTICS					
Common-Mode Rejection	DC, V_{CM} = −3.5 V to +3.5 V	86	90		dB
	V_{CM} = 1 V p-p, f = 10 MHz		65		dB
	V_{CM} = 1 V p-p, f = 100 MHz		28		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		±10.5		V
Differential Operating Range			±2.5		V
Resistance	Differential		5		MΩ
	Common-mode		3		MΩ
Capacitance	Differential		2		pF
	Common-mode		3		pF
DC PERFORMANCE					
Open-Loop Gain	V_{OUT} = ±1 V		70		dB
Closed-Loop Gain Error	DC		0.25		%
Input Offset Voltage		−4.3		+4.3	mV
	T_{MIN} to T_{MAX}		15		µV/°C
Input Bias Current (+IN, −IN)		−3.0		+3.0	µA
Input Bias Current (REF, FB)		−4.6		+3.7	µA
Input Bias Current Drift	T_{MIN} to T_{MAX} (+IN, −IN)		16		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)	−2.55		+1.45	µA
Input Offset Current Drift	T_{MIN} to T_{MAX}		±3		nA/°C
OUTPUT PERFORMANCE					
Voltage Swing	R_{LOAD} = 1 kΩ	−10.80		+10.82	V
Output Current			40		mA
Short Circuit Current	Short to GND, source/sink		107/147		mA
COMPARATOR PERFORMANCE					
V_{OH}		3.135	3.3		V
V_{OL}			0.2	0.255	V
Hysteresis Width			41		mV
Input Bias Current	Input driven low		3.5		µA
Propagation Delay, t_{PLH}	R_L = 10 kΩ		20		ns
Propagation Delay, t_{PHL}	R_L = 10 kΩ		15		ns
Output Rise Time	25% to 75%, R_L = 10 kΩ		15		ns
Output Fall Time	25% to 75%, R_L = 10 kΩ		11		ns

Downloaded from Arrow.com.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN PERFORMANCE					
Power-Down V_{IH}			V_{S+} − 1.5		V
Power-Down V_{IL}			V_{S+} − 2.5		V
Power-Down I_{IH}	PD = V_{CC}		1.0		µA
Power-Down I_{IL}	PD = GND		800		µA
Power-Down Assert Time			0.5		µs
POWER SUPPLY					
Operating Range		4.5		24	V
Quiescent Current, Positive Supply			44.0	57.5	mA
Quiescent Current, Negative Supply			37.0	51.0	mA
PSRR, Positive Supply	DC		−75	−71	dB
PSRR, Negative Supply	DC		−82	−81	dB

Downloaded from Arrow.com.

V_S = ±5 V, T_A = 25°C, REF = 0 V, R_L = 150 Ω, C_L = 2 pF, G = 1, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		230		MHz
	V_{OUT} = 2 V p-p		130		MHz
Bandwidth for 0.1dB Flatness	V_{OUT} = 0.2 V p-p		45		MHz
Slew Rate	V_{OUT} = 2 V p-p, R_L = 1 kΩ		1000		V/µs
Settling Time	V_{OUT} = 2 V p-p, 1%		10		ns
	V_{OUT} = 2 V p-p, 0.1%		23		ns
Output Overdrive Recovery			50		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 1 V p-p, 1 MHz		−68		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 1 MHz		−82		dBc
Crosstalk	V_{OUT} = 1 V p-p, 10 MHz		−70		dB
Input Voltage Noise (RTI)	f ≥ 10 kHz		14		nV/√Hz
Differential Gain Error	NTSC, 200 IRE, R_L ≥ 150 Ω		0.3		%
Differential Phase Error	NTSC, 200 IRE, R_L ≥ 150 Ω		0.6		Degrees
INPUT CHARACTERISTICS					
Common-Mode Rejection	DC, V_{CM} = −3.5 V to +3.5 V	84	90		dB
	V_{CM} = 1 V p-p, f = 10 MHz		65		dB
	V_{CM} = 1 V p-p, f = 100 MHz		28		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		±3.8		V
Differential Operating Range			±2.5		V
Resistance	Differential		5		MΩ
	Common-mode		3		MΩ
Capacitance	Differential		2		pF
	Common-mode		3		pF
DC PERFORMANCE					
Open-Loop Gain	V_{OUT} = ±1 V		70		dB
Closed-Loop Gain Error	DC		0.25		%
Input Offset Voltage		−3.7		+3.7	mV
	T_{MIN} to T_{MAX}		15		µV/°C
Input Bias Current (+IN, −IN)		−3.0		+2.7	µA
Input Bias Current (REF, FB)		−4.3		+3.0	µA
Input Bias Current Drift	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		16		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)	−2.9		1.9	µA
Input Offset Current Drift	T_{MIN} to T_{MAX}		±3		nA/°C
OUTPUT PERFORMANCE					
Voltage Swing	R_{LOAD} = 150 Ω	−3.53		+3.53	V
Output Current			40		mA
Short Circuit Current	Short to GND, source/sink		107/147		mA
COMPARATOR PERFORMANCE					
V_{OH}	R_L = 10 kΩ	3.02	3.14		V
V_{OL}	R_L = 10 kΩ		0.19	0.25	V
Hysteresis Width			32		mV
Input Bias Current	Input driven low		3.5		µA
Propagation Delay, t_{PLH}			20		ns
Propagation Delay, t_{PHL}			15		ns
Output Rise Time	10% to 90%		15		ns
Output Fall Time	10% to 90%		11		ns

Downloaded from Arrow.com.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN PERFORMANCE					
Power-Down V_{IH}			V_{S+} − 1.5		V
Power-Down V_{IL}			V_{S+} − 2.5		V
Power-Down I_{IH}	PD = V_{CC}		1		µA
Power-Down I_{IL}	PD = GND		230		µA
Power-Down Assert Time			0.5		µs
POWER SUPPLY					
Operating Range		4.5		24	V
Quiescent Current, Positive Supply			39.0	49.5	mA
Quiescent Current, Negative Supply			34.5	43.5	mA
PSRR, Positive Supply	DC		−80	−74	dB
PSRR, Negative Supply	DC		−80	−75	dB

Downloaded from Arrow.com.

V_S = 5 V, T_A = 25°C, REF = +2.5 V, R_L = 150 Ω, C_L = 2 pF, G = 1, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		220		MHz
	V_{OUT} = 2 V p-p		125		MHz
Bandwidth for 0.1dB Flatness	V_{OUT} = 0.2 V p-p		45		MHz
Slew Rate	V_{OUT} = 2 V p-p, R_L = 1 kΩ		1000		V/µs
Settling Time	V_{OUT} = 2 V p-p, 1%		10		ns
	V_{OUT} = 2 V p-p, 0.1%		23		ns
Output Overdrive Recovery			50		ns
NOISE					
Crosstalk	V_{OUT} = 1 V p-p, 10 MHz		−70		dB
Input Voltage Noise (RTI)	f ≥ 10 kHz		14		nV/√Hz
INPUT CHARACTERISTICS					
Common-Mode Rejection	DC, V_{CM} = −3.5 V to +3.5 V	76	90		dB
	V_{CM} = 1 V p-p, f = 10 MHz		65		dB
	V_{CM} = 1 V p-p, f = 100 MHz		32		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		1.3 to 3.7		V
Differential Operating Range			±2.5		V
Resistance	Differential		5		MΩ
	Common-mode		3		MΩ
Capacitance	Differential		2		pF
	Common-mode		3		pF
DC PERFORMANCE					
Open-Loop Gain	V_{OUT} = ±1 V		70		dB
Closed-Loop Gain Error	DC, measured at G = 11		0.25		%
Input Offset Voltage		−3.4		+3.4	mV
	T_{MIN} to T_{MAX}		15		µV/°C
Input Bias Current (+IN, −IN)		−3		+2.7	µA
Input Bias Current (REF, FB)		−4.5		+3	µA
Input Bias Current Drift	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		16		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)	−2.3		+1.3	µA
Input Offset Current Drift	T_{MIN} to T_{MAX}		±3		nA/°C
OUTPUT PERFORMANCE					
Voltage Swing	R_{LOAD} = 150 Ω	0.88		3.58	V
Output Current			40		mA
Short Circuit Current	Short to GND		150		mA
COMPARATOR PERFORMANCE					
V_{OH}	R_L = 10 kΩ	3.02			V
V_{OL}	R_L = 10 kΩ			0.25	V
Hysteresis Width			32		mV
Input Bias Current	Input driven low		3.5		µA
Propagation Delay, t_{PLH}			20		ns
Propagation Delay, t_{PHL}			15		ns
Output Rise Time	10% to 90%		15		ns
Output Fall Time	10% to 90%		11		ns
POWER-DOWN PERFORMANCE					
Power-Down V_{IH}			V_{S+} − 1.5		V
Power-Down V_{IL}			V_{S+} − 2.5		V
Power-Down I_{IH}	PD = V_{CC}		1		µA
Power-Down I_{IL}	PD = GND		230		µA
Power-Down Assert Time			0.5		µs

Downloaded from Arrow.com.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		24	V
Quiescent Current, Positive Supply			31.5	38.8	mA
PSRR, Positive Supply	DC		−86	−76	dB

Downloaded from Arrow.com.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	24 V
Power Dissipation	See Figure 2
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface, which is thermally connected to a copper plane.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5 mm × 5 mm, 32-Lead LFCSP	45	7	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8143 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8143. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipation due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through-holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface which is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 32-lead LFCSP (45°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad which is thermally connected to a PCB plane. Extra thermal relief is required for operation at high supply voltages. See the Applications Information section for details. θ_{JA} values are approximations.

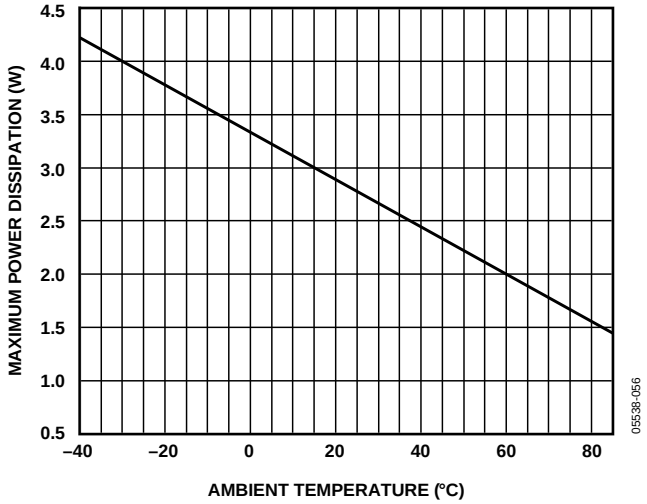

Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Downloaded from Arrow.com.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

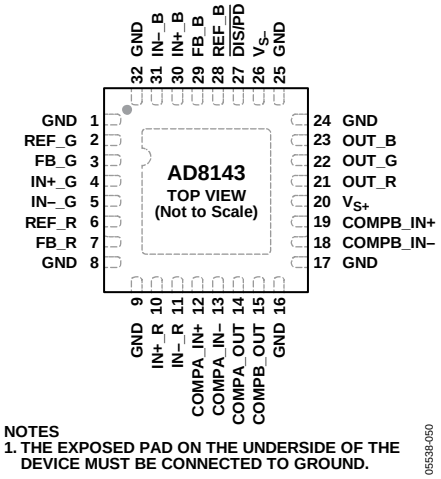

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9,16, 17, 24, 25, 32	GND	Signal Ground and Thermal Plane Connection (See the Applications Information Section)
2	REF_G	Reference Input, Green Channel
3	FB_G	Feedback Input, Green Channel
4	IN+_G	Noninverting Input, Green Channel
5	IN–_G	Inverting Input, Green Channel
6	REF_R	Reference Input, Red Channel
7	FB_R	Feedback Input, Red Channel
10	IN+_R	Noninverting Input, Red Channel
11	IN–_R	Inverting Input, Red Channel
12	COMPA_IN+	Positive Input, Comparator A
13	COMPA_IN–	Negative Input, Comparator A
14	COMPA_OUT	Output, Comparator A
15	COMPB_OUT	Output, Comparator B
18	COMPB_IN–	Negative Input, Comparator B
19	COMPB_IN+	Positive Input, Comparator B
20	V_{S+}	Positive Power Supply
21	OUT_R	Output, Red Channel
22	OUT_G	Output, Green Channel
23	OUT_B	Output, Blue Channel
26	V_{S-}	Negative Power Supply
27	$\overline{\text{DIS/PD}}$	Disable/Power Down
28	REF_B	Reference Input, Blue Channel
29	FB_B	Feedback Input, Blue Channel
30	IN+_B	Noninverting Input, Blue Channel
31	IN–_B	Inverting Input, Blue Channel
0	EPAD	Exposed Pad. The exposed pad on the underside of the device must be connected to ground (see the Applications Information section).

Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, G = 1, R_L = 150 Ω, C_L = 2 pF, V_S = ±5 V, T_A = 25°C. Refer to the circuit in Figure 38.

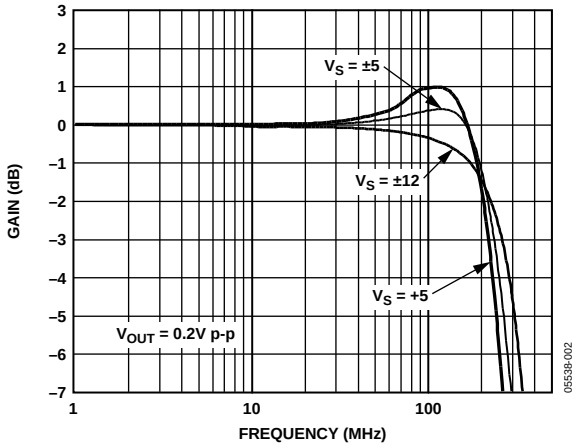

Figure 4. Small Signal Frequency Response at Various Power Supplies, G = 1

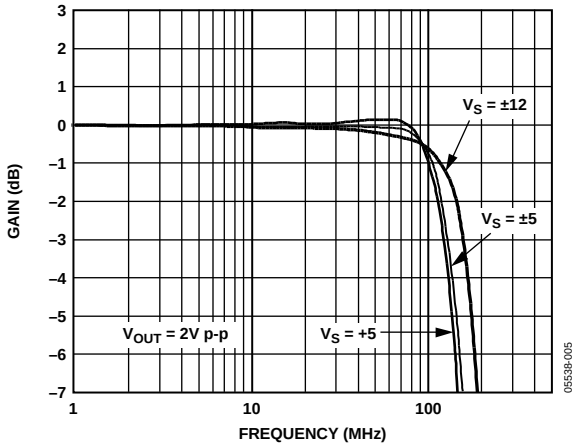

Figure 7. Large Signal Frequency Response at Various Power Supplies, G = 1

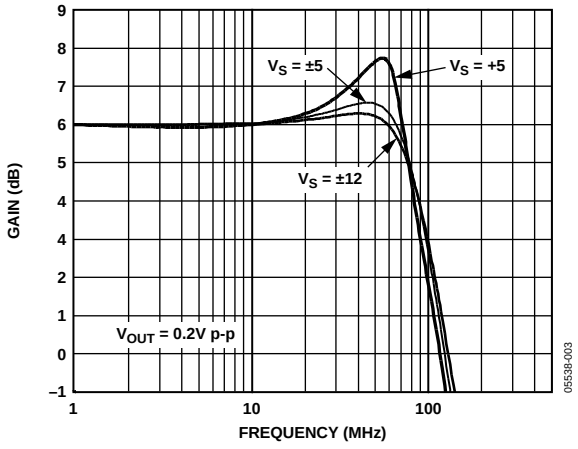

Figure 5. Small Signal Frequency Response at Various Power Supplies, G = 2

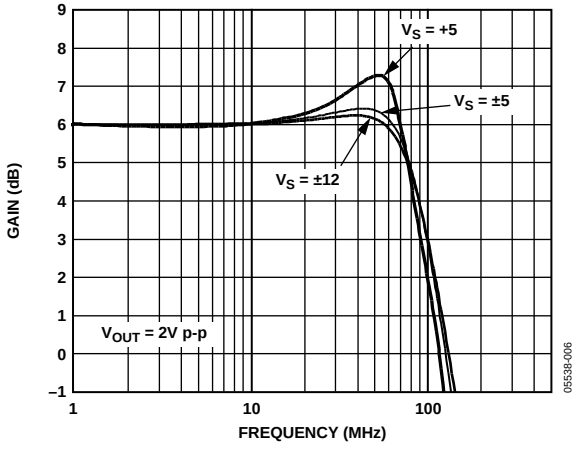

Figure 8. Large Signal Frequency Response at Various Power Supplies, G = 2

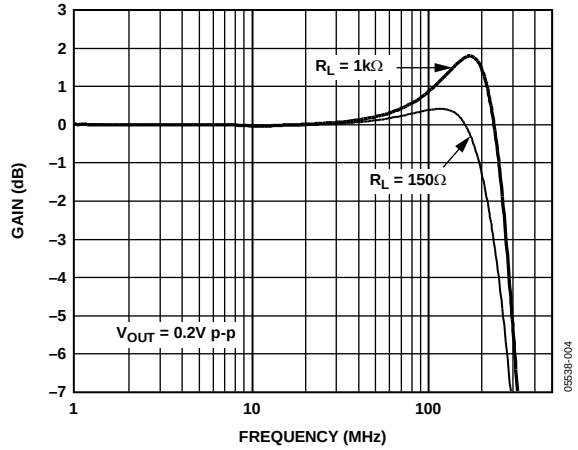

Figure 6. Small Signal Frequency Response at Various Loads

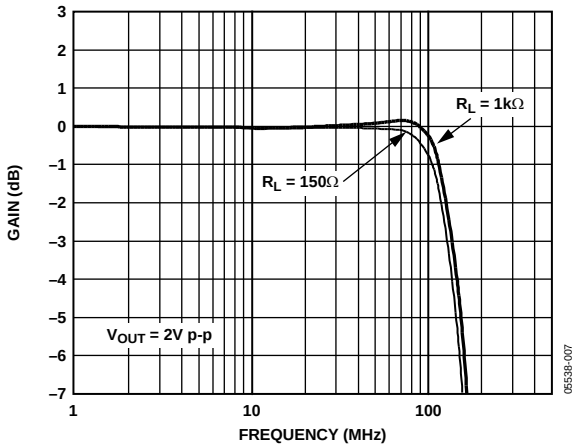

Figure 9. Large Signal Frequency Response at Various Loads

Downloaded from Arrow.com.

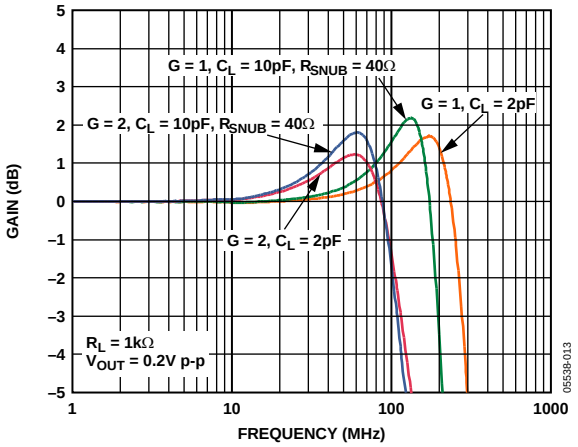

Figure 10. Small Signal Frequency Response at Various Gains and 10 pF Capacitive Load Buffered by 40 Ω Resistor

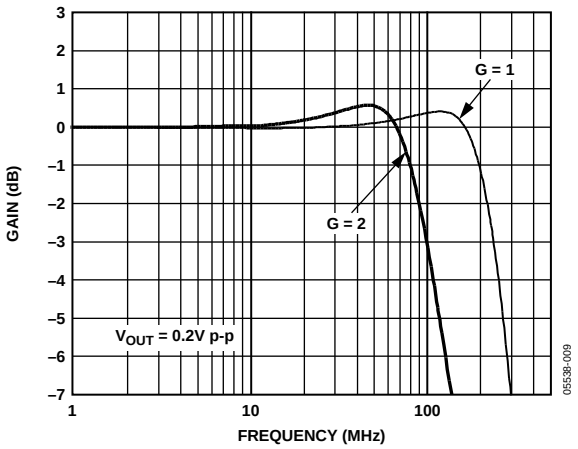

Figure 11. Small Signal Frequency Response at Various Gains

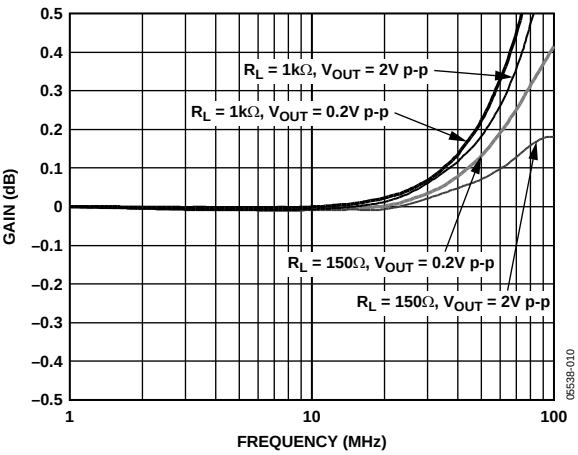

Figure 12. 0.1 dB Flatness for Various Loads and Output Amplitudes

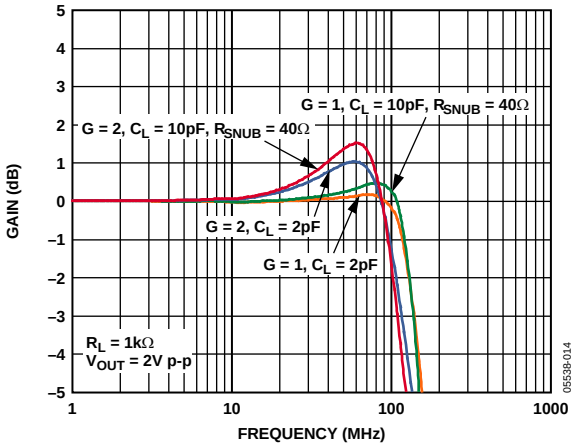

Figure 13. Large Signal Frequency Response at Various Gains and 10 pF Capacitive Load Buffered by 40 Ω Resistor

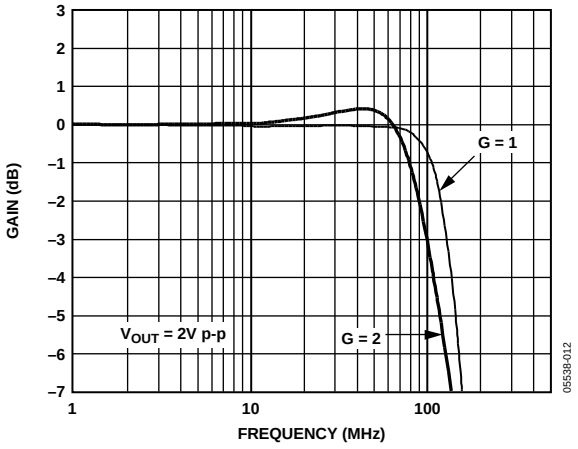

Figure 14. Large Signal Frequency Response at Various Gains

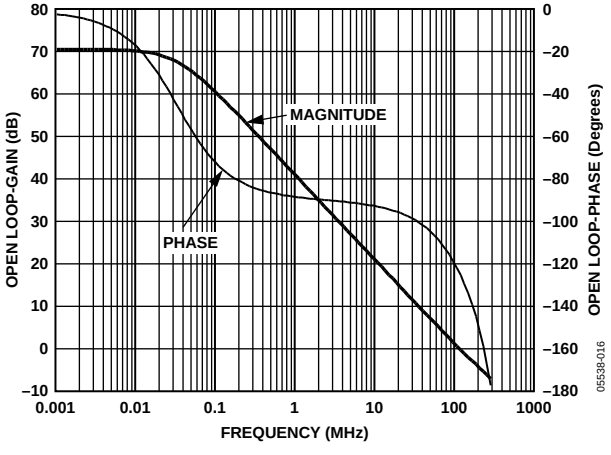

Figure 15. Open-Loop Gain and Phase Responses

Downloaded from Arrow.com.

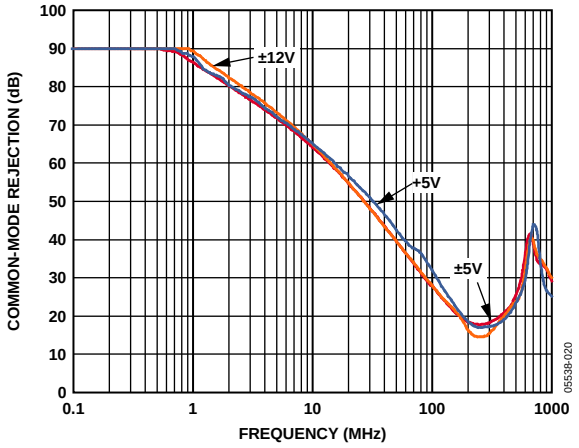

Figure 16. Common-Mode Rejection Ratio vs. Frequency at Various Supplies

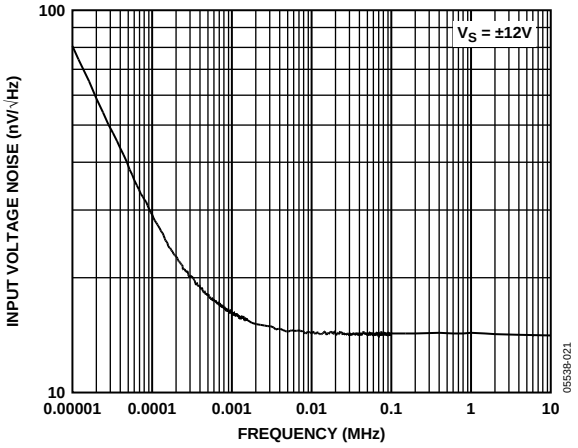

Figure 19. Input Referred Voltage Noise vs. Frequency

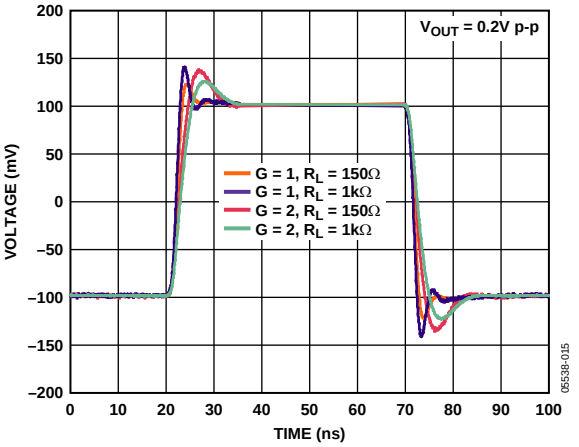

Figure 17. Small Signal Transient Response at Various Gains and Loads

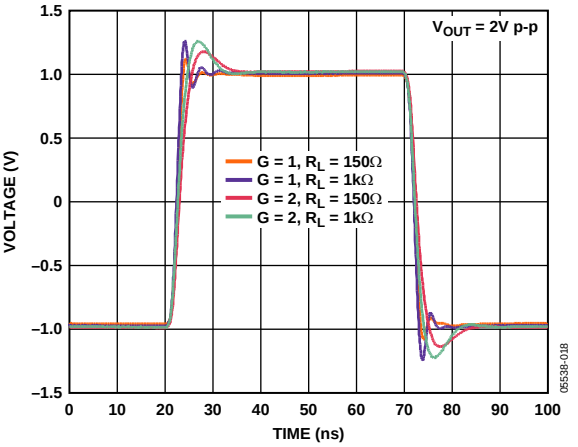

Figure 20. Large Signal Transient Response at Various Gains and Loads

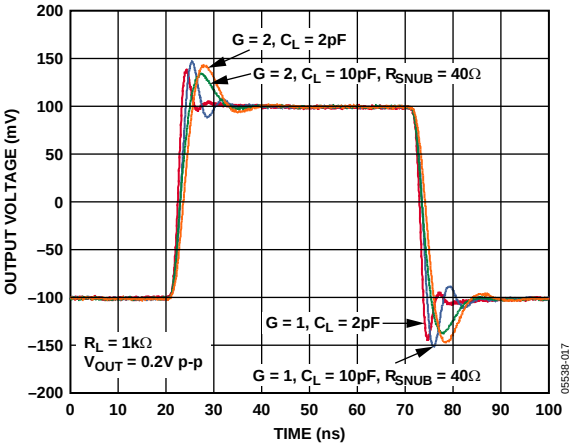

Figure 18. Small Signal Transient Response at Various Gains and 10 pF Capacitive Load Buffered by 40 Ω Resistor

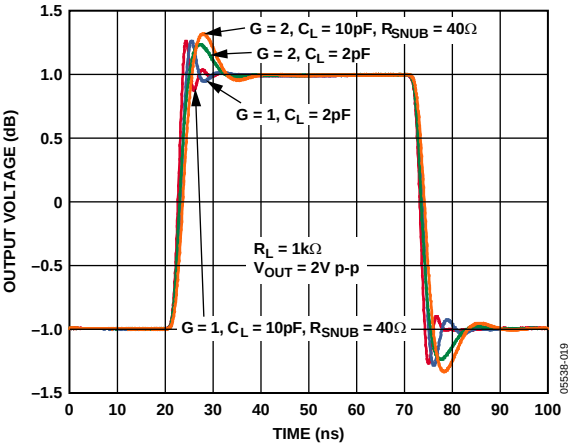

Figure 21. Large Signal Transient Response at Various Gains and 10 pF Capacitive Load Buffered by 40 Ω Resistor

Downloaded from Arrow.com.

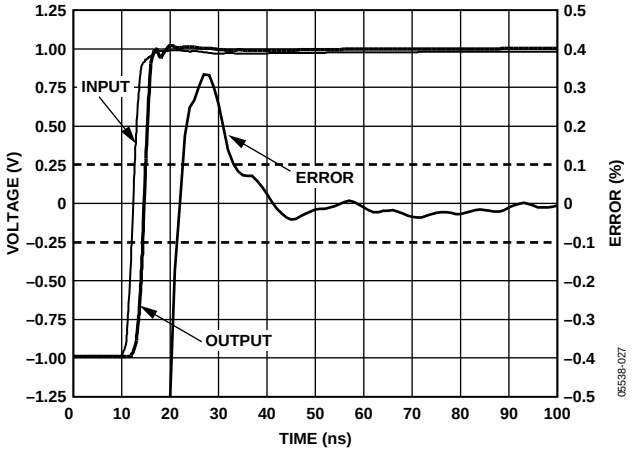

Figure 22. Settling Time (0.1%) at Various Loads

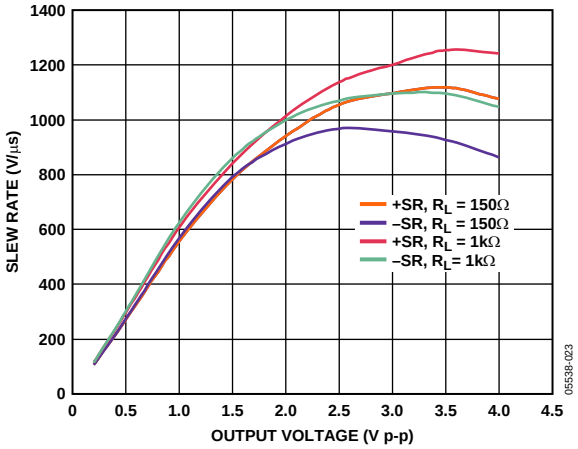

Figure 25. Slew Rate vs. Input Voltage Swing at Various Loads

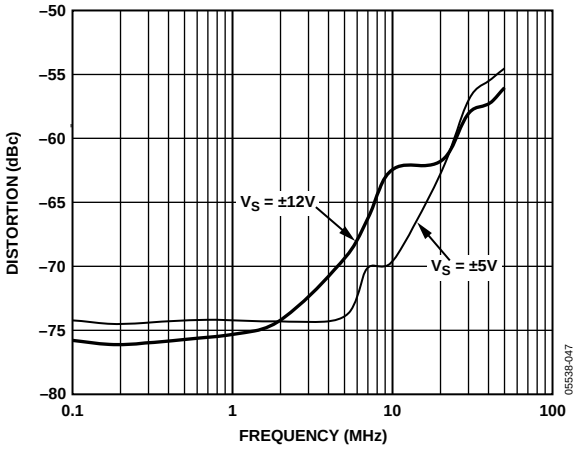

Figure 23. Second Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p, G = 2

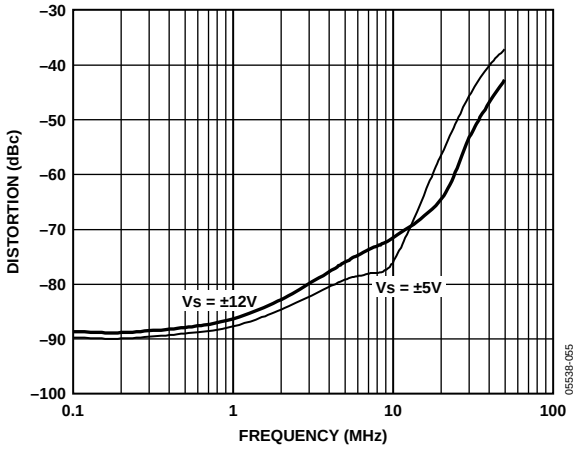

Figure 26. Third Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p, G = 2

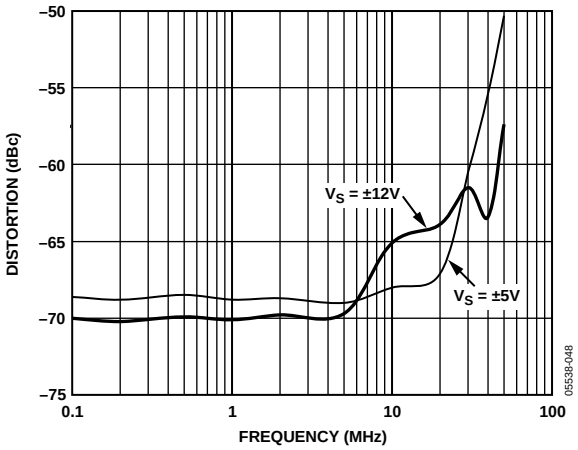

Figure 24. Second Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p

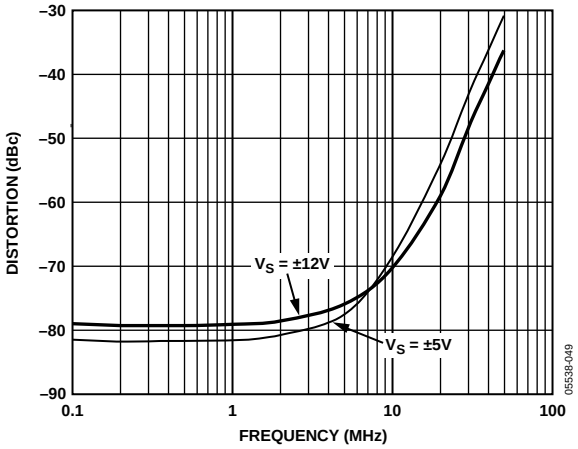

Figure 27. Third Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p

Downloaded from Arrow.com.

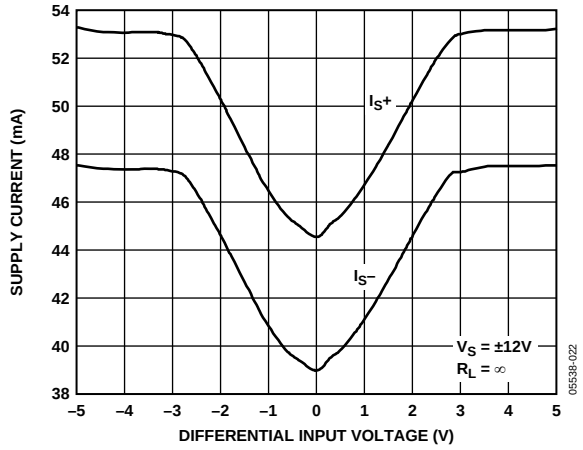

Figure 28. Power Supply Current vs. Differential Input Voltage at ±12 V Supplies

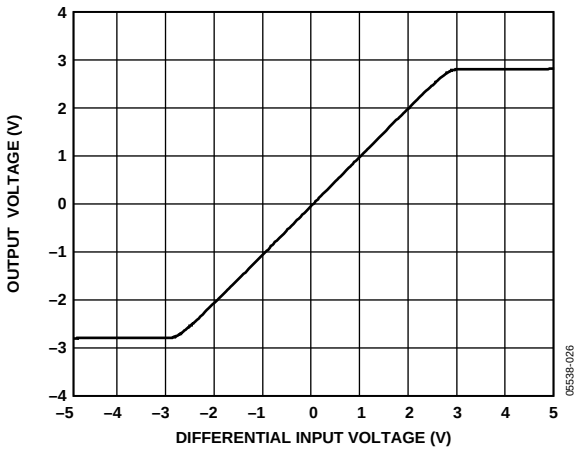

Figure 31. Differential Input Operating Range

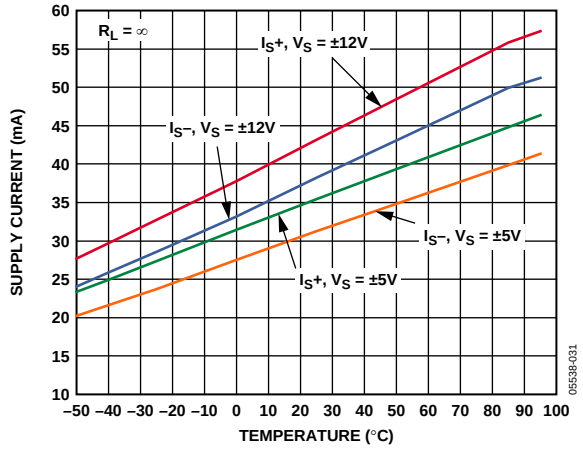

Figure 29. Power Supply Current vs. Temperature

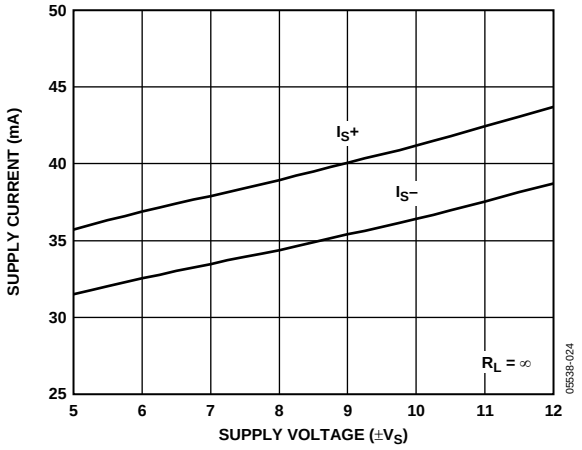

Figure 32. Power Supply Current vs. Power Supply Voltage

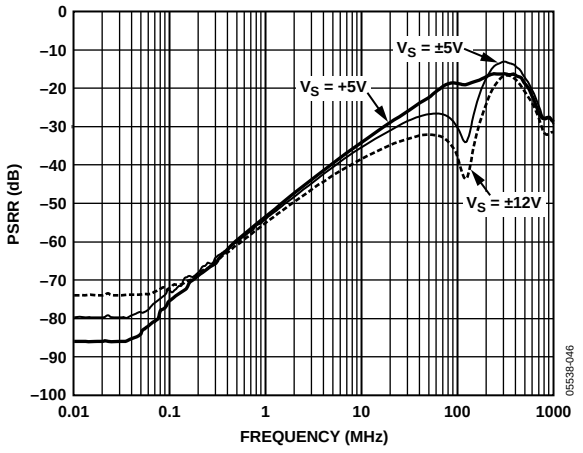

Figure 30. Positive Power Supply Rejection Ratio vs. Frequency

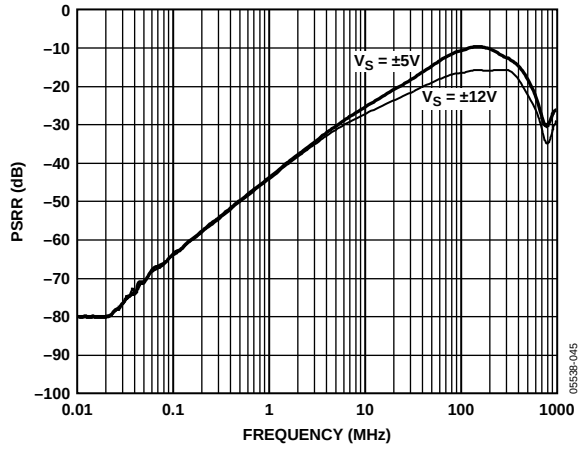

Figure 33. Negative Power Supply Rejection Ratio vs. Frequency

Downloaded from Arrow.com.

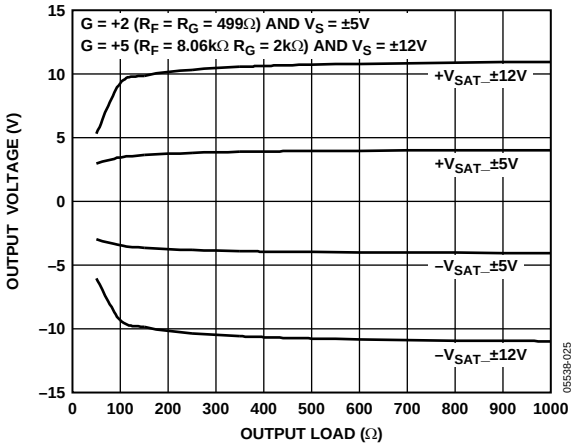

Figure 34. Output Saturation Voltage vs. Output Load

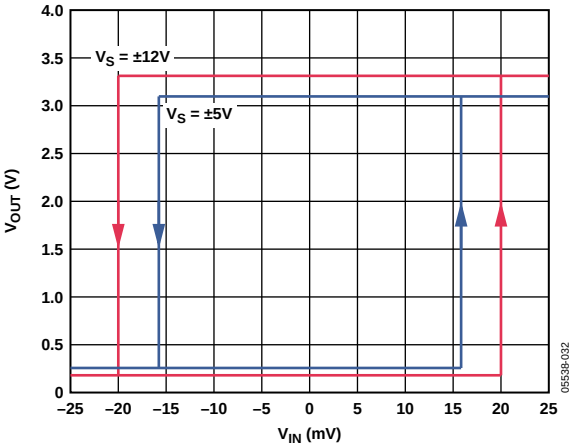

Figure 36. Comparator Hysteresis

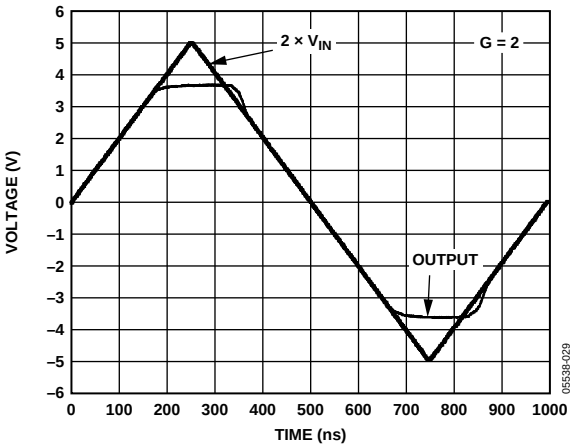

Figure 35. Output Overdrive Recovery

Downloaded from Arrow.com.

THEORY OF OPERATION

The AD8143 amplifiers use an architecture called active feedback, which differs from that of conventional op amps. The most obvious differentiating feature is the presence of two separate pairs of differential inputs compared to a conventional op amp's single pair. Typically, for the active-feedback architecture, one of these input pairs is driven by a differential input signal, while the other is used for the feedback. This active stage in the feedback path is where the term active feedback is derived.

The active feedback architecture offers several advantages over a conventional op amp in several types of applications. Among these are excellent common-mode rejection, wide input common-mode range, and a pair of inputs that are high impedance and completely balanced in a typical application. In addition, while an external feedback network establishes the gain response as in a conventional op amp, its separate path makes it entirely independent of the signal input. This eliminates any interaction between the feedback and input circuits, which traditionally causes problems with CMRR in conventional differential-input op amp circuits.

Another advantage of active feedback is the ability to change the polarity of the gain merely by switching the differential inputs. A high input impedance inverting amplifier can therefore be made. Besides high input impedance, a unity-gain inverter with the AD8143 has noise gain of unity, producing lower output noise and higher bandwidth than op amps that have noise gain equal to 2 for a unity-gain inverter.

The two differential input stages of the AD8143 are each transconductance stages that are well-matched. These stages convert the respective differential input voltages to internal currents. The currents are then summed and converted to a voltage, which is buffered to drive the output. The compensation capacitor is included in the summing circuit. When the feedback path is closed around the part, the output drives the feedback input to that voltage which causes the internal currents to sum to zero. This occurs when the two differential inputs are equal and opposite; that is, their algebraic sum is zero.

In a closed-loop application, a conventional op amp has its differential input voltage driven to near zero under non-transient conditions. The AD8143 generally has differential input voltages at each of its input pairs, even under equilibrium conditions. As a practical consideration, it is necessary to internally limit the differential input voltage with a clamp circuit. Thus, the input dynamic ranges are limited to about 2.5 V for the AD8143 (see the Specifications section for more detail). For this and other reasons, it is not recommended to reverse the input and feedback stages of the AD8143, even though some apparently normal functionality may be observed under some conditions.

Downloaded from Arrow.com.

APPLICATIONS INFORMATION

OVERVIEW

The AD8143 contains three independent active-feedback amplifiers that can be effectively applied as differential line receivers for red-green-blue (RGB) signals or component video, such as YPbPr, signals transmitted over unshielded-twisted-pair (UTP) cable. The AD8143 also contains two general-purpose comparators with hysteresis that can be used to receive digital signals or to extract video synchronization pulses from received common-mode signals that contain encoded synchronization signals.

An internal linear voltage regulator derives power for the comparators from the positive supply; therefore, the AD8143 must always have a minimum positive supply voltage of 4.5 V.

The AD8143 includes a power-down feature that can be asserted to reduce the supply current when a particular device is not in use.

BASIC CLOSED-LOOP GAIN CONFIGURATIONS

As described in the Theory of Operation section, placing a resistive feedback network between an amplifier output and its respective feedback amplifier input creates a stable negative feedback amplifier. It is important to note that the closed-loop gain of the amplifier used in the signal path is defined as the amplifier's single-ended output voltage divided by its differential input voltage. Therefore, each amplifier in the AD8143 provides differential-to-single-ended gain. Additionally, the amplifier used for feedback has two high impedance inputs—the FB input, where the negative feedback is applied, and the REF input, which can be used as an independent single-ended input to apply a dc offset to the output signal. Some basic gain configurations implemented with an AD8143 amplifier are shown in Figure 37 through Figure 39.

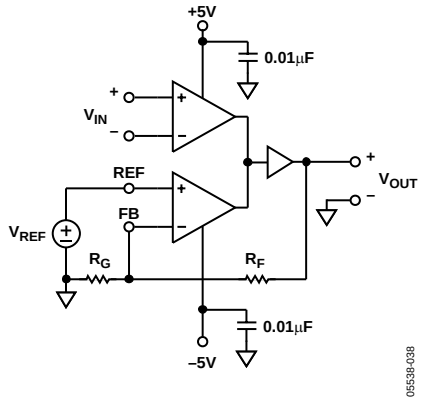

Figure 37. Basic Gain Circuit: $V_{OUT} = (V_{IN} + V_{REF})(1 + R_F/R_G)$

The gain equation for the circuit in Figure 37 is

$$V_{OUT} = (V_{IN} + V_{REF})(1 + R_F/R_G) \quad (1)$$

In this configuration, the voltage applied to the REF pin appears at the output with a gain of $1 + R_F/R_G$.

To achieve unity gain from V_{REF} to V_{OUT} in this configuration, divide V_{REF} by the same factor used in the feedback loop; the same R_F and R_G values can be used. Figure 38 illustrates this approach.

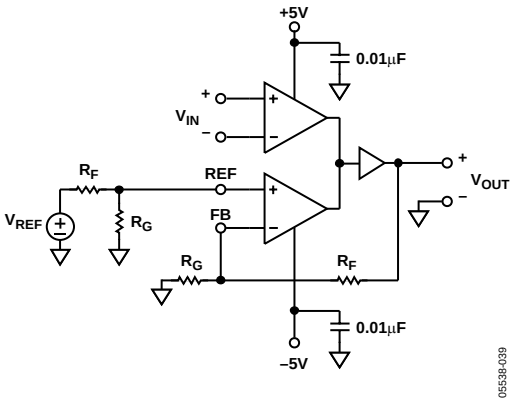

Figure 38. Basic Gain Circuit: $V_{OUT} = V_{IN}(1 + R_F/R_G) + V_{REF}$

The gain equation for the circuit in Figure 38 is

$$V_{OUT} = V_{IN}(1 + R_F/R_G) + V_{REF} \quad (2)$$

Another configuration that provides the same gain equation as Equation 2 is shown in Figure 39. In this configuration, it is important to keep the source resistance of V_{REF} much smaller than R_G to avoid gain errors.

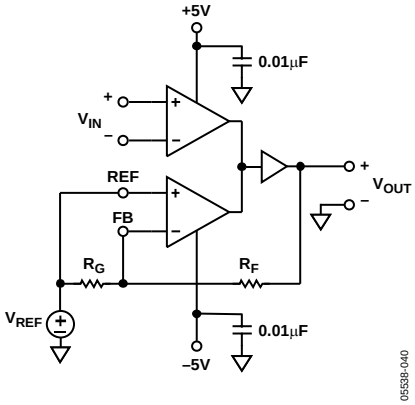

Figure 39. Basic Gain Circuit: $V_{OUT} = V_{IN}(1 + R_F/R_G) + V_{REF}$

For stability reasons, the inductance of the trace connected to the REF pin must be kept to less than 10 nH. The typical inductance of 50 Ω traces on the outer layers of the FR-4 boards is 7 nH/in, and on the inner layers, it is typically 9 nH/in. Vias must be accounted for as well. The inductance of a typical via in a 0.062-inch board is on the order of 1.5 nH. If longer traces are required, a 200 Ω resistor should be placed in series with the trace to reduce the Q-factor of the inductance.

Downloaded from Arrow.com.

In many dual-supply applications, V_{REF} can be directly connected to ground right at the device.

TERMINATING THE INPUT

One of the key benefits of the active-feedback architecture is the separation that exists between the differential input signal and the feedback network. Because of this separation, the differential input maintains its high CMRR and provides high differential and common-mode input impedances, making line termination a simple task.

Most applications that use the AD8143 involve transmitting broadband video signals over 100 Ω UTP cable and use dc-coupled terminations. The two most common types of dc-coupled terminations are differential and common-mode. Differential termination of 100 Ω UTP is implemented by simply connecting a 100 Ω resistor across the amplifier input, as shown in Figure 40.

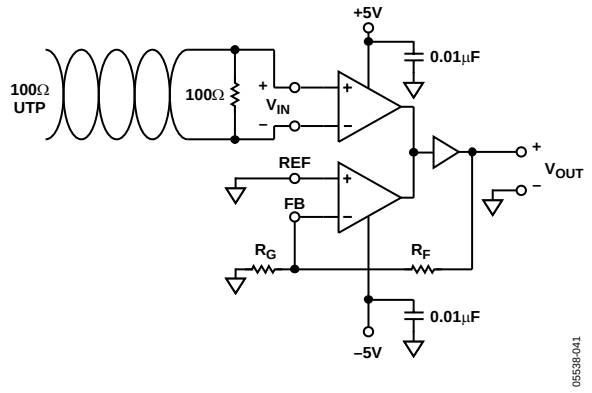

Figure 40. Differential-Mode Termination

Some applications require common-mode terminations for common-mode currents generated at the transmitter. In these cases, the 100 Ω termination resistor is split into two 50 Ω resistors. The required common-mode termination voltage is applied at the tap between the two resistors. In many of these applications, the common-mode tap is connected to ground (V_{TERM} (CM) = 0). This scheme is illustrated in Figure 41.

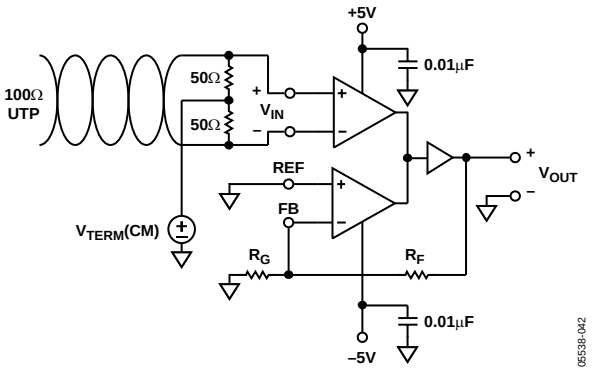

Figure 41. Common-Mode Termination

INPUT CLAMPING

The differential input that is assigned to receive the input signal includes clamping diodes that limit the differential input swing to approximately 5.5 V p-p at 25°C. Because of this, the input and feedback stages should never be interchanged. Figure 31 illustrates the clamping action at the signal input stage.

The supply current drawn by the AD8143 has a strong dependence on input signal magnitude because the input transconductance stages operate with differential input signals that can be up to a few volts peak-to-peak. This behavior is distinctly different from that of traditional op-amps, where the differential input signal is driven to essentially 0 V by negative feedback. Figure 28 illustrates the supply current dependence on input voltage.

For most applications, including receiving RGB video signals, the input signal magnitudes encountered are well within the safe operating limits of the AD8143 over its full power supply and operating temperature ranges. In some extreme applications where large differential and/or common-mode voltages can be encountered, external clamping may be necessary. Another application where external common-mode clamping is sometimes required is when an unpowered AD8143 receives a signal from an active driver. In this case, external diodes are required when the current drawn by the internal ESD diodes cannot be kept to less than 5 mA.

When using ±12 V supplies, the differential input signal must be kept to less than 4 V p-p. In applications that use ±12 V supplies where the input signals are expected to reach or exceed 4 V p-p, external differential clamping at a maximum of 4 V p-p is required.

Figure 42 shows a general approach to external differential-mode clamping.

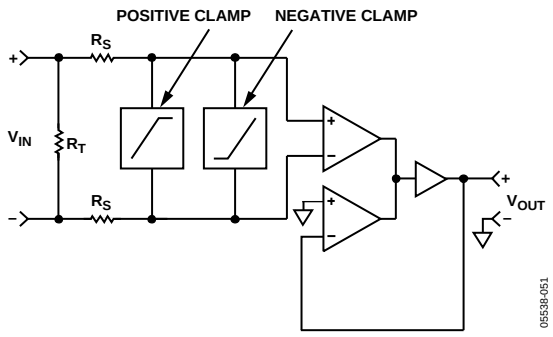

Figure 42. Differential-Mode Clamping

The positive and negative clamps are nonlinear devices that exhibit very low impedance when the voltage across them reaches a critical threshold (clamping voltage), thereby limiting the voltage across the AD8143 input. The positive clamp has a positive threshold, and the negative clamp has a negative threshold.

Downloaded from Arrow.com.

A diode is a simple example of such a clamp. Schottky diodes generally have lower clamping voltages than typical signal diodes. The clamping voltage should be larger than the largest expected signal amplitude, with enough margin to ensure that the received signal passes without being distorted.

A simple way to implement a clamp is to use a number of diodes in series. The resultant clamping voltage is then the sum of the clamping voltages of individual diodes.

A 1N4448 diode has a forward voltage of approximately 0.70 V to 0.75 V at typical current levels that are seen when it is being used as a clamp, and 2 pF maximum capacitance at 0 V bias. (The capacitance of a diode decreases as its reverse bias voltage is increased.) The series connection of two 1N4448 diodes, therefore, has a clamping voltage of 1.4 V to 1.5 V. Figure 43 shows how to limit the differential input voltage applied to an AD8143 amplifier to ±1.4 V to ±1.5 V (2.8 V p-p to 3.0 V p-p). Note that the resulting capacitance of the two series diodes is half that of one diode. Different numbers of series diodes can be used to obtain different clamping voltages.

R_T is the differential termination resistor and the series resistances, R_S, limit the current into the diodes. The series resistors should be highly matched in value to preserve high frequency CMRR.

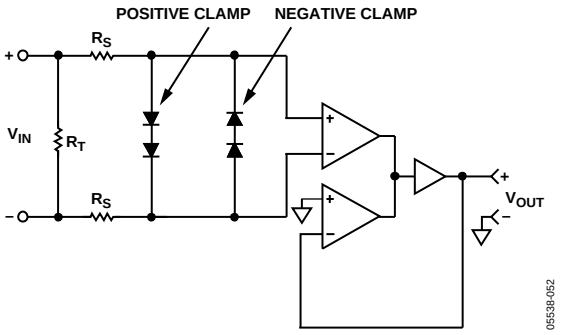

Figure 43. Using Two 1N4448 Diodes in Series as a Clamp

There are many other nonlinear devices that can be used as clamps. The best choice for a particular application depends upon the desired clamping voltage, response time, parasitic capacitance, and other factors.

When using external differential-mode clamping, it is important to ensure that the series resistors (R_S), the sum of the parasitic capacitance of the clamping devices, and the input capacitance of the AD8143 are small enough to preserve the desired signal bandwidth.

Figure 44 shows a specific example of external common-mode clamping.

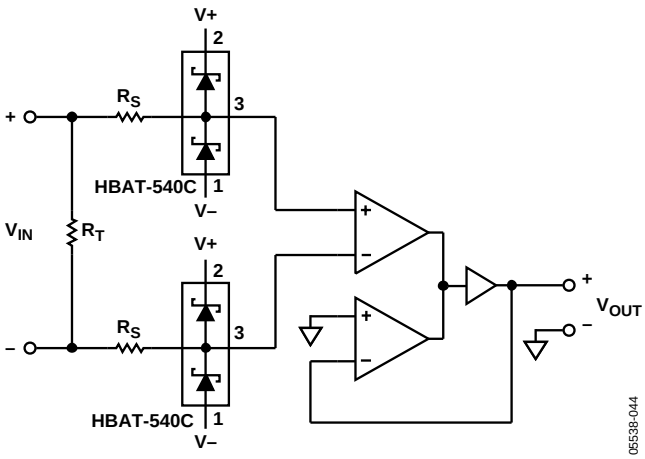

Figure 44. External Common-Mode Clamping

The series resistances, R_S, limit the current in each leg, and the Schottky diodes limit the voltages on each input to approximately 0.3 V to 0.4 V over the positive power supply, V+ and to 0.3 V to 0.4 V below the negative power supply, V−. The maximum value of R_S is determined by the required signal bandwidth, the line impedance, and the effective differential capacitance due to the AD8143 inputs and the diodes.

As with the differential clamp, the series resistors should be highly matched in value to preserve high frequency CMRR.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The two most important issues with regard to printed circuit board (PCB) layout are minimizing parasitic signal trace reactances in the feedback network and providing sufficient thermal relief.

Excessive parasitic reactances in the feedback network cause excessive peaking in the amplifier's frequency response and excessive overshoot in its step response due to a reduction in phase margin. Oscillation occurs when these parasitic reactances are increased to a critical point where the phase margin is reduced to zero. Minimizing these reactances is important to obtain optimal performance from the AD8143.

When operating at ±12 V power, it is important to pay special attention to removing heat from the AD8143.

Besides the special layout considerations previously mentioned and expounded upon in the following sections, general high speed layout practices must be adhered to when applying the AD8143. Controlled impedance transmission lines are required for incoming and outgoing signals, referenced to a ground plane.

Downloaded from Arrow.com.

Typically, the input signals are received over 100 Ω differential transmission lines. A 100 Ω differential transmission line is readily realized on the printed circuit board using two well-matched, closely-spaced 50 Ω single-ended traces that are coupled through the ground plane. The traces that carry the single-ended output signals are most often 75 Ω for video signals. Output signal connections should include series termination resistors that are matched to the impedance of the line they are driving.

Broadband power supply decoupling networks should be placed as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

Minimizing Parasitic Reactances in the Feedback Network

Parasitic trace capacitance and inductance are both reduced when the traces that connect the feedback network together are reduced in length. Removing the copper from all planes below the traces reduces trace capacitance, but increases trace inductance because the loop area formed by the trace and ground plane is increased. A reasonable compromise that works well is to void all copper directly under the feedback loop traces and component pads with margins on each side approximately equal to one trace width. Combining this technique with minimizing trace lengths is effective in keeping parasitic trace reactances in the feedback loop to a minimum. Additionally, all components used in the feedback network should be in 0402 surface-mount packages. Figure 45 illustrates the magnified view of a proven feedback network layout that provides excellent performance. Note that the internal layers are not shown.

It is strongly recommended that the layout shown in Figure 45, or something very similar, be used for the three AD8143 feedback networks.

A conservative estimate for feedback-loop trace capacitance in each loop of the layout shown in Figure 45 is 2 pF. This value is viewed as the minimum load capacitance and is reflected in the frequency response and transient response plots.

Maximizing Heat Removal

The AD8143 pinout includes ground connections on its corner pins to facilitate heat removal. These pins should be connected to the exposed paddle on the underside of the AD8143 and to a ground plane on the component side of the board. Additionally, a 5 × 5 array of thermal vias connecting the exposed pad to internal ground planes should be placed inside the PCB pad that is soldered to the exposed pad. Using these techniques is highly recommended in all applications, and is required in ±12 V applications where power dissipation is the greatest. Figure 45 illustrates how to optimize the circuit board layout for heat removal.

Designs must often conform to design-for-manufacturing (DFM) rules that stipulate how to lay out PCBs in such a way as to facilitate the manufacturing process. Some of these rules require thermal relief on pads that connect to planes, and the rules may preclude the use of the technique illustrated in Figure 45. In these cases, the ground pins should be connected to the exposed paddle and component-side ground plane using techniques that conform to the DFM requirements.

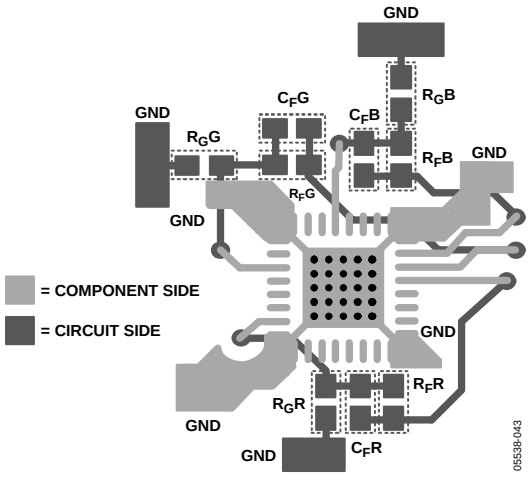

Figure 45. Recommended Layout for Feedback Loops and Grounding

Downloaded from Arrow.com.

DRIVING A CAPACITIVE LOAD

The AD8143 typically drives either high impedance loads, such as crosspoint switch inputs, or doubly terminated coaxial cables. A gain of 1 is commonly used in the high impedance case because the 6 dB transmission line termination loss is not incurred. A gain of 2 is required when driving cables to compensate for the 6 dB termination loss.

In all cases, the output must drive the parasitic capacitance of the feedback loop, conservatively estimated to be 2 pF, in addition to the capacitance presented by the actual load. When driving a high impedance input, it is recommended that a small series resistor be used to buffer the input capacitance of the device being driven. Clearly, the resistor value must be small enough to preserve the required bandwidth. In the ideal doubly terminated cable case, the AD8143 output sees a purely resistive load. In reality, there is some residual capacitance, and this is buffered by the series termination resistor. Figure 46 illustrates the high impedance case, and Figure 47 illustrates the cable-driving case.

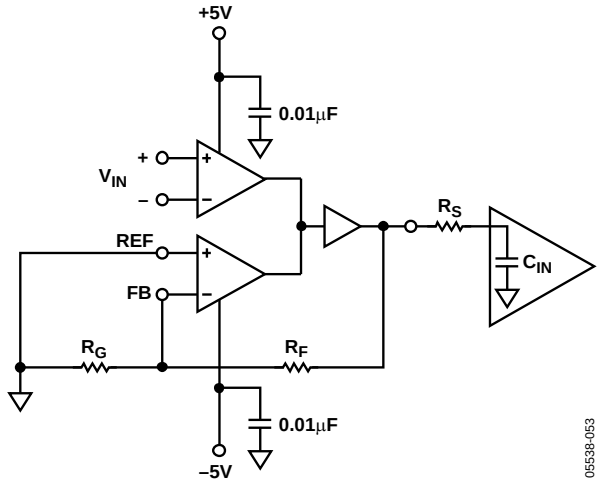

Figure 46. Buffering the Input Capacitance of a High-Z Load

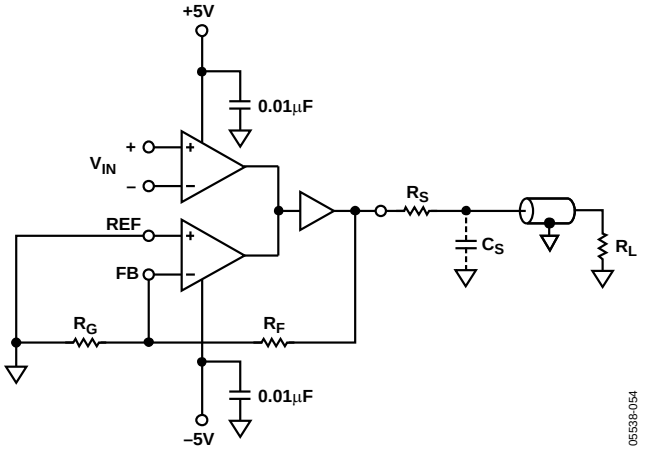

Figure 47. Driving a Doubly Terminated Cable

Small and large signal frequency responses for the High-Z case with a 40 Ω series resistor and 10 pF load capacitance are shown in Figure 10 and Figure 13; transient responses for the same conditions are shown in Figure 18 and Figure 21. In the cable driving case shown in Figure 47, C_S << 2 pF for a well-designed circuit; therefore, the feedback loop capacitance is the dominant capacitive load. The feedback loop capacitance is present for all cases, and its effect is included in the data presented in the Typical Performance Characteristics and Specifications tables.

POWER-DOWN

The power-down feature is intended to be used to reduce power consumption when a particular device is not in use, and does not place the output in a High-Z state when asserted. The power-down feature is asserted when the voltage applied to the power-down pin drops to approximately 2 V below the positive supply. The AD8143 is enabled by pulling the power-down pin to the positive supply.

COMPARATORS

In addition to general-purpose applications, the two on-chip comparators can be used to receive differential digital information or to decode video sync pulses from received common-mode voltages. Built-in hysteresis helps to eliminate false triggers from noise.

The comparator outputs are not designed to drive transmission lines. When the signals detected by the comparators are driven over cables or controlled impedance printed circuit board traces, the comparator outputs must be fed to a spare logic gate, FPGA, or other device that is capable of driving signals over transmission lines.

An internal linear voltage regulator derives power for the comparators from the positive supply; therefore, the AD8143 must always have a minimum positive supply voltage of 4.5 V.

SYNC PULSE EXTRACTION USING COMPARATORS

The AD8143 is particularly useful in keyboard video mouse (KVM) applications. KVM networks transmit and receive computer video signals, which are typically comprised of red, green, and blue (RGB) video signals and separate horizontal and vertical sync signals. Because the sync signals are separate and not embedded in the color signals, it is advantageous to transmit them using a simple scheme that encodes them among the three common-mode voltages of the RGB signals. The AD8134 triple differential driver is a natural complement to the AD8143 and performs the sync pulse encoding with the necessary circuitry on-chip.

Downloaded from Arrow.com.

The AD8134 encoding equations are given in Equation 3, Equation 4, and Equation 5.

$$Red\ V_{CM} = \frac{K}{2}(V - H) \quad (3)$$

$$Green\ V_{CM} = \frac{K}{2}(-2\ \mathrm{V}) \quad (4)$$

$$Blue\ V_{CM} = \frac{K}{2}(V + H) \quad (5)$$

where:

Red V_{CM}, *Green* V_{CM}, and *Blue* V_{CM} are the transmitted common-mode voltages of the respective color signals.
K is an adjustable gain constant that is set by the AD8134.
V and *H* are the vertical and horizontal sync pulses, defined with a weight of −1 when the pulses are in their low states, and a weight of +1 when they are in their high states.
The AD8134 data sheet contains further details regarding the encoding scheme.

Figure 48 illustrates how the AD8143 comparators can be used to extract the horizontal and vertical sync pulses that are encoded on the RGB common-mode voltages by the AD8134.

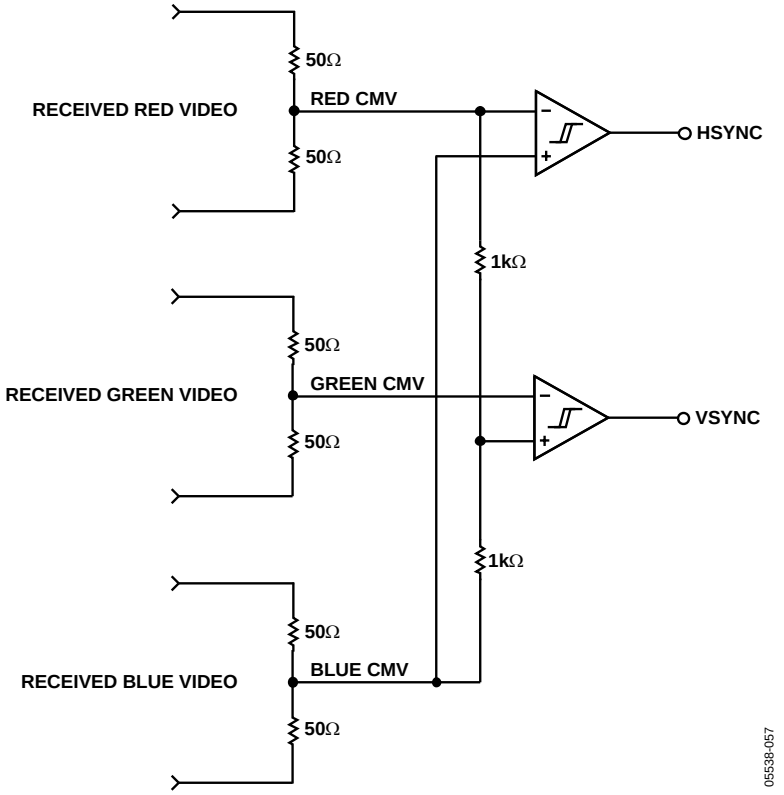

Figure 48. Extracting Sync Signals from Received Common-Mode Signals

Downloaded from Arrow.com.

OUTLINE DIMENSIONS

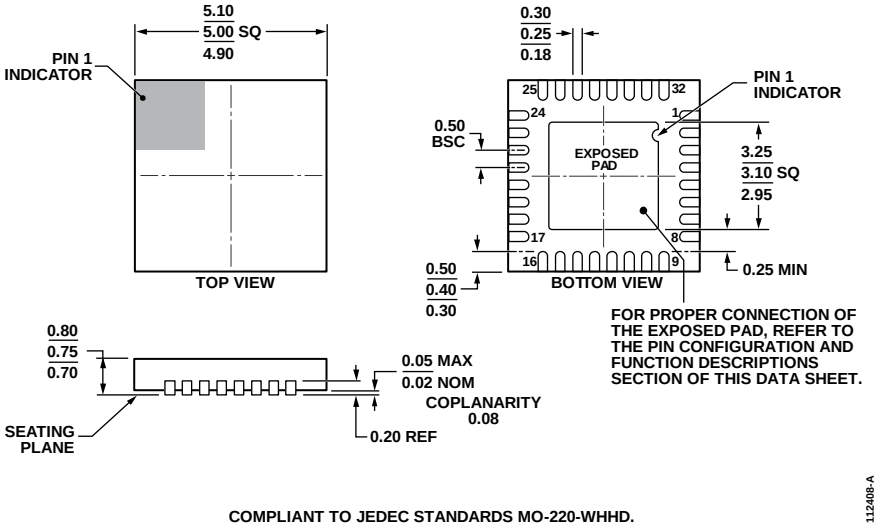

Figure 49. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8143ACPZ-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD8143ACPZ-REEL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD8143ACPZ-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD8143-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

© 2005–2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D05538-0-4/16(A)

Downloaded from Arrow.com.