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## REVISION HISTORY

**11/2019—Rev. C to Rev. D**
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**12/2005—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—10 kΩ VERSION

$V_{DD}/V_{SS}$ = ±15 V ± 10%, $V_A = V_{DD}$, $V_B = V_{SS}$ or 0 V, −40°C < $T_A$ < +125°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS RHEOSTAT MODE | | | | | | |
| Resistor Differential NL[2] | R-DNL | $R_{WB}$, $V_A$ = NC | −1 | ±0.3 | +1 | LSB |
| Resistor Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = NC | −1.5 | ±0.7 | +1.5 | LSB |
| Nominal Resistor Tolerance | $\Delta R_{AB}$ | $T_A$ = +25°C | −30 | | +30 | % |
| Resistance Temperature Coefficient[3] | $(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$ | $V_{AB} = V_{DD}$, wiper = no connect | | 35 | | ppm/°C |
| Wiper Resistance | $R_W$ | | | 50 | 100 | Ω |
| DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE | | | | | | |
| Integral Nonlinearity[4] | INL | | −1 | ±0.3 | +1 | LSB |
| Differential Nonlinearity[4] | DNL | | −1 | ±0.3 | +1 | LSB |
| Voltage Divider Temperature Coefficient | $(\Delta V_W/V_W)/\Delta T \times 10^6$ | Code = 0x80 | | 5 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = 0xFF | −6 | −4 | 0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = 0x00 | 0 | +3 | +5 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_{A, B, W}$ | | $V_{SS}$ | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_{A, B}$ | f = 1 MHz, measured to GND, code = 0x80 | | 45 | | pF |
| Capacitance[6] | $C_W$ | f = 1 MHz, measured to GND, code = 0x80 | | 60 | | pF |
| Common-Mode Leakage | $I_{CM}$ | $V_A = V_B = V_W$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High ($\overline{CS}$, CLK, SDI) | $V_{IH}$ | | 2.4 | | | V |
| Input Logic Low ($\overline{CS}$, CLK, SDI) | $V_{IL}$ | | | | 0.8 | V |
| Output Logic High (SDO) | $V_{OH}$ | $R_{Pull-up}$ = 2.2 kΩ to 5 V | 4.9 | | | V |
| Output Logic Low (SDO) | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Input Current | $I_{IL}$ | $V_{IN}$ = 0 V or 5 V | | | ±1 | µA |
| Input Capacitance[6] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Positive Supply Current | $I_{DD}$ | $V_{IH}$ = +5 V or $V_{IL}$ = 0 V, $V_{DD}/V_{SS}$ = ±15 V | | 15 | 50 | µA |
| Negative Supply Current | $I_{SS}$ | $V_{IH}$ = +5 V or $V_{IL}$ = 0 V, $V_{DD}/V_{SS}$ = ±15 V | | −0.01 | −1 | µA |
| Power Dissipation[7] | $P_{DISS}$ | $V_{IH}$ = +5 V or $V_{IL}$ = 0 V, $V_{DD}/V_{SS}$ = ±15 V | | | 765 | µW |
| Power Supply Rejection Ratio | PSRR | $\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10% | −0.15 | ±0.08 | +0.15 | %/% |

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DYNAMIC CHARACTERISTICS[6, 8, 9] | | | | | | |
| Bandwidth −3 dB | BW | Code = 0x80 | | 470 | | kHz |
| Total Harmonic Distortion | $THD_W$ | $V_A$ = 1 V rms, $V_B$ = 0 V, f = 1 kHz | | 0.006 | | % |
| $V_W$ Settling Time | $t_S$ | $V_A$ = 10 V, $V_B$ = 0 V, ±1 LSB error band | | 4 | | µs |
| Resistor Noise Voltage | $e_{N\_WB}$ | $R_{WB}$ = 5 kΩ, f = 1 kHz | | 9 | | nV/√Hz |

[1] Typical represents average reading at +25°C, $V_{DD}$ = +15 V, and $V_{SS}$ = −15 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic.
[3] All parts have a 35 ppm/°C temperature coefficient.
[4] INL and DNL are measured at $V_W$ with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B$ = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] $P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$) + abs ($I_{SS} \times V_{SS}$). CMOS logic-level inputs result in minimum power dissipation.
[8] Bandwidth, noise, and settling times are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[9] All dynamic characteristics use $V_{DD}$ = +15 V and $V_{SS}$ = −15 V.

## ELECTRICAL CHARACTERISTICS—50 KΩ, 100 KΩ VERSIONS

$V_{DD}/V_{SS}$ = ±15 V ± 10%, $V_A$ = $+V_{DD}$, $V_B$ = $V_{SS}$ or 0 V, −40°C < $T_A$ < +125°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS RHEOSTAT MODE | | | | | | |
| Resistor Differential NL[2] | R-DNL | $R_{WB}$, $V_A$ = NC | −0.5 | ±0.1 | +0.5 | LSB |
| Resistor Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = NC | −1 | ±0.5 | +1 | LSB |
| Nominal Resistor Tolerance | $\Delta R_{AB}$ | $T_A$ = +25°C | −30 | | +30 | % |
| Resistance Temperature Coefficient[3] | $(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$ | $V_{AB}$ = $V_{DD}$, wiper = no connect | | 35 | | ppm/°C |
| Wiper Resistance | $R_W$ | | | 50 | 100 | Ω |
| DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE | | | | | | |
| Integral Nonlinearity[4] | INL | | −1 | ±0.5 | +1 | LSB |
| Differential Nonlinearity[4] | DNL | | −1 | ±0.5 | +1 | LSB |
| Voltage Divider Temperature Coefficient | $(\Delta V_W/V_W)/\Delta T \times 10^6$ | Code = 0x80 | | 5 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = 0xFF | −2.5 | −1.6 | 0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = 0x00 | 0 | +0.6 | +1.5 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_{A, B, W}$ | | $V_{SS}$ | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_{A, B}$ | f = 1 MHz, measured to GND, code = 0x80 | | 45 | | pF |
| Capacitance[6] | $C_W$ | f = 1 MHz, measured to GND, code = 0x80 | | 60 | | pF |
| Common-Mode Leakage | $I_{CM}$ | $V_A$ = $V_B$ = $V_W$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High ($\overline{CS}$, CLK, SDI) | $V_{IH}$ | | 2.4 | | | V |
| Input Logic Low ($\overline{CS}$, CLK, SDI) | $V_{IL}$ | | | | 0.8 | V |
| Output Logic High (SDO) | $V_{OH}$ | $R_{Pull-up}$ = 2.2 kΩ to 5 V | 4.9 | | | V |
| Output Logic Low (SDO) | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Input Current | $I_{IL}$ | $V_{IN}$ = 0 V or 5 V | | | ±1 | μA |
| Input Capacitance[6] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Positive Supply Current | $I_{DD}$ | $V_{IH}$ = +5 V or $V_{IL}$ = 0 V, $V_{DD}/V_{SS}$ = ±15 V | | 15 | 50 | μA |
| Negative Supply Current | $I_{SS}$ | $V_{IH}$ = +5 V or $V_{IL}$ = 0 V, $V_{DD}/V_{SS}$ = ±15 V | | −0.01 | −1 | μA |
| Power Dissipation[7] | $P_{DISS}$ | $V_{IH}$ = +5 V or $V_{IL}$ = 0 V, $V_{DD}/V_{SS}$ = ±15 V | | | 765 | μW |
| Power Supply Rejection Ratio | PSRR | $\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10% | −0.05 | ±0.01 | +0.05 | %/% |

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DYNAMIC CHARACTERISTICS[6, 8, 9] | | | | | | |
| Bandwidth −3 dB | BW | $R_{AB}$ = 50 kΩ, code = 0x80 | | 90 | | kHz |
| | | $R_{AB}$ = 100 kΩ, code = 0x80 | | 50 | | kHz |
| Total Harmonic Distortion | $THD_W$ | $V_A$ = 1 V rms, $V_B$ = 0 V, f = 1 kHz | | 0.002 | | % |
| $V_W$ Settling Time | $t_S$ | $V_A$ = 10 V, $V_B$ = 0 V, ±1 LSB error band | | 4 | | µs |
| Resistor Noise Voltage | $e_{N\_WB}$ | $R_{WB}$ = 25 kΩ, f = 1 kHz | | 20 | | $nV\sqrt{Hz}$ |

[1] Typical represents average reading at +25°C, VDD = +15 V, and VSS = −15 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from an ideal value measured between successive tap positions. Parts are guaranteed monotonic.
[3] All parts have a 35 ppm/°C temperature coefficient.
[4] INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output DAC. VA = VDD and VB = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] $P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$) + abs ($I_{SS} \times V_{SS}$). CMOS logic level inputs result in minimum power dissipation.
[8] Bandwidth, noise, and settling times are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[9] All dynamic characteristics use VDD = +15 V and VSS = −15 V.

## INTERFACE TIMING CHARACTERISTICS

**Table 3.**

| Parameter [1, 2] | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock Frequency | $f_{CLK}$ | | | | 4 | MHz |
| Input Clock Pulse Width | $t_{CH}$, $t_{CL}$ | Clock level high or low | 120 | | | ns |
| Data Setup Time | $t_{DS}$ | | 30 | | | ns |
| Data Hold Time | $t_{DH}$ | | 20 | | | ns |
| CLK to SDO Propagation Delay[3] | $t_{PD}$ | $R_{Pull\text{-}up}$ = 2.2 kΩ, $C_L$ < 20 pF | 10 | | 100 | ns |
| $\overline{CS}$ Setup Time | $t_{CSS}$ | | 120 | | | ns |
| $\overline{CS}$ High Pulse Width | $t_{CSW}$ | | 150 | | | ns |
| CLK Fall to $\overline{CS}$ Fall Hold Time | $t_{CSH0}$ | | 10 | | | ns |
| CLK Rise to $\overline{CS}$ Rise Hold Time | $t_{CSH}$ | | 120 | | | ns |
| $\overline{CS}$ Rise to Clock Rise Setup | $t_{CS1}$ | | 120 | | | ns |

[1] See Figure 3 for the location of the measured values. All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of 1.6 V. Switching characteristics are measured using $V_{DD}$ = +15 V and $V_{SS}$ = −15 V.
[2] Guaranteed by design and not subject to production test.
[3] Propagation delay depends on the value of $V_{DD}$, $R_{Pull\text{-}up}$, and $C_L$.

# 3-WIRE DIGITAL INTERFACE

Data is loaded MSB first.

**Table 4. AD5290 Serial Data-Word Format**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| D7<br>MSB<br>$2^7$ | D6 | D5 | D4 | D3 | D2 | D1 | D0<br>LSB<br>$2^0$ |

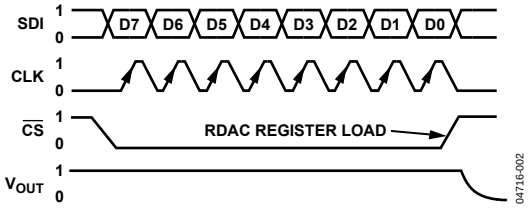


*Figure 2. AD5290 3-Wire Digital Interface Timing Diagram ($V_A = V_{DD}$, $V_B = 0$ V, $V_W = V_{OUT}$)*

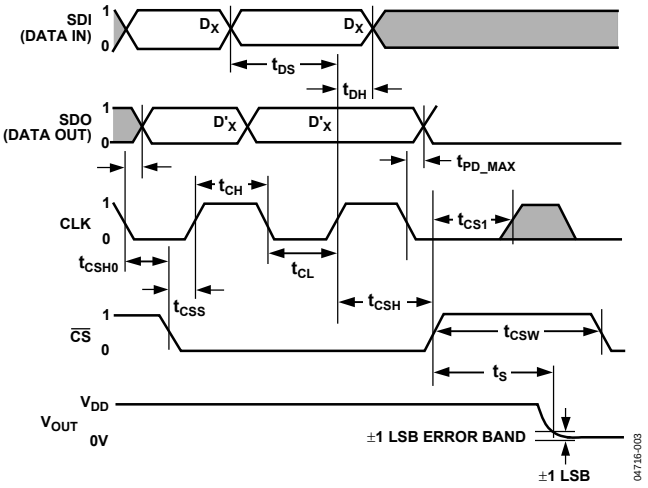


*Figure 3. Detail Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = +25°C, unless otherwise noted.

**Table 5.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V, +35 V |
| $V_{SS}$ to GND | +0.3 V, −16.5 V |
| $V_{DD}$ to $V_{SS}$ | −0.3 V, +35 V |
| $V_A$, $V_B$, $V_W$ to GND | $V_{SS}$, $V_{DD}$ |
| Maximum Current | |
| $I_{WB}$, $I_{WA}$ Pulsed | ±20 mA |
| $I_{WB}$ Continuous ($R_{WB}$ ≤ 6 kΩ, A Open, $V_{DD}/V_{SS}$ = 30 V/0 V)[1] | ±5 mA |
| $I_{WA}$ Continuous ($R_{WA}$ ≤ 6 kΩ, B Open, $V_{DD}/V_{SS}$ = 30 V/0 V)[1] | ±5 mA |
| Digital Input and Output Voltages to GND | 0 V, +7 V |
| Operating Temperature Range | −40°C to +125°C |
| Maximum Junction Temperature ($T_{JMAX}$)[2] | +150°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec to 30 sec) | 245°C |
| Thermal Resistance[2] $\theta_{JA}$: MSOP-10 | 230°C/W |

[1] The maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and the maximum applied voltage across any two of the following at a given resistance: A terminal, B terminal, and W terminal.
[2] Package power dissipation = ($T_{JMAX}$ − $T_A$)/$\theta_{JA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND DESCRIPTIONS

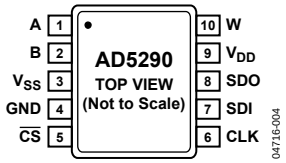


*Figure 4. AD5290 Pin Configuration*

**Table 6. AD5290 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | A | A Terminal. $V_{SS} \le V_A \le V_{DD}$. |
| 2 | B | B Terminal. $V_{SS} \le V_B \le V_{DD}$. |
| 3 | $V_{SS}$ | Negative Supply. Connect to 0 V for single-supply applications. |
| 4 | GND | Digital Ground. |
| 5 | $\overline{CS}$ | Chip Select Input; Active Low. When $\overline{CS}$ returns high, data is loaded into the wiper register. |
| 6 | CLK | Serial Clock Input. Positive edge triggered. |
| 7 | SDI | Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first. |
| 8 | SDO | Serial Data Output Pin. Internal N-Ch FET with open-drain output that requires external pull-up resistor. It shifts out the previous eight SDI bits that allow daisy-chain operation of multiple packages. |
| 9 | $V_{DD}$ | Positive Power Supply. |
| 10 | W | W Terminal. $V_{SS} \le V_W \le V_{DD}$. |

# TYPICAL PERFORMANCE CHARACTERISTICS

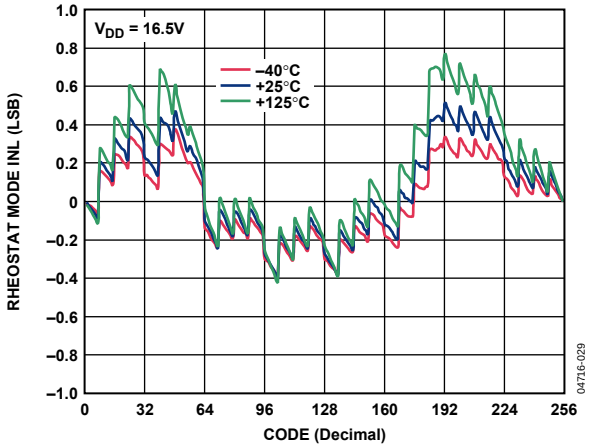


Figure 5. Resistance Step Position Nonlinearity Error vs. Code

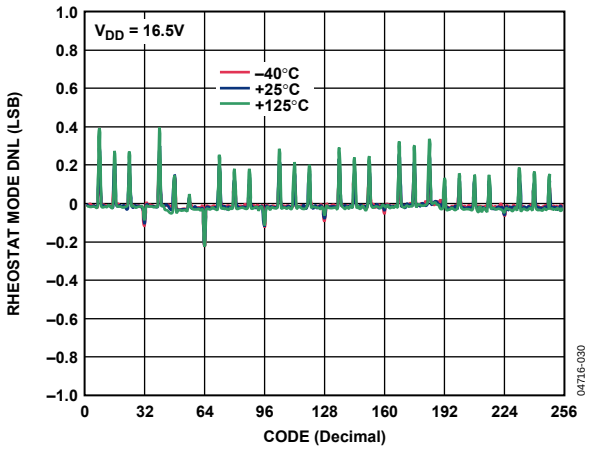


Figure 6. Resistance Step Change Differential Nonlinearity Error vs. Code

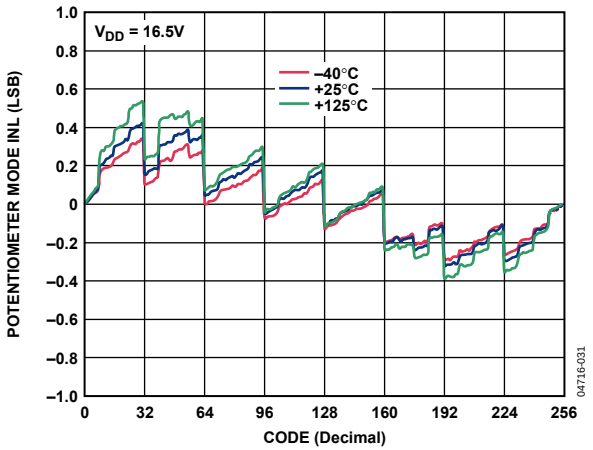


Figure 7. Potentiometer Divider Nonlinearity Error vs. Code

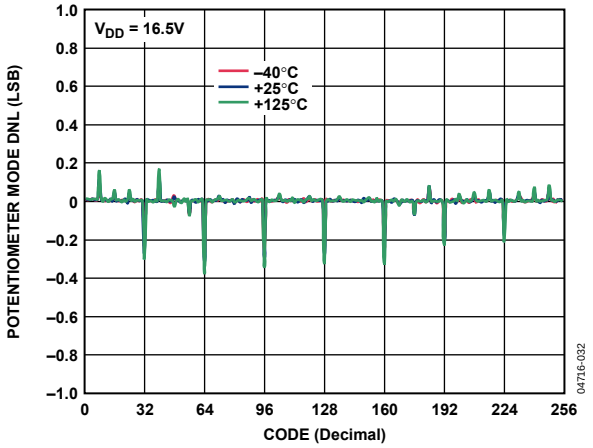


Figure 8. Potentiometer Divider Differential Nonlinearity Error vs. Code

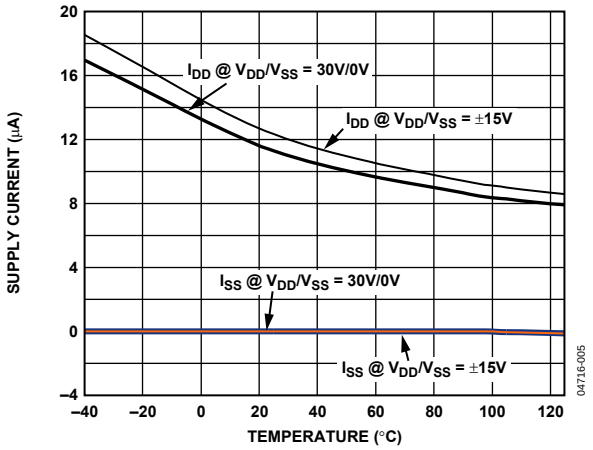


Figure 9. Supply Current $I_{DD}$ vs. Temperature

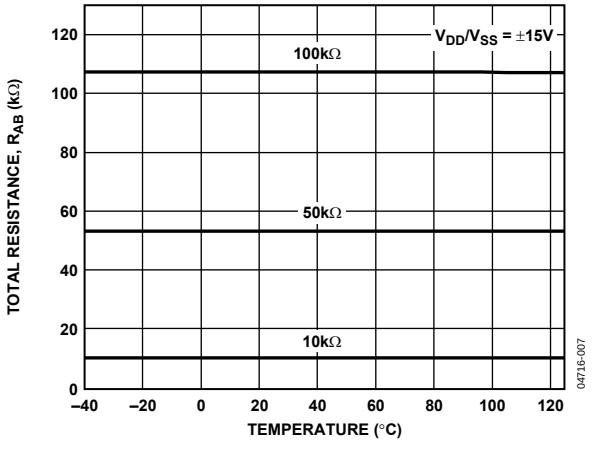


Figure 10. Total Resistance vs. Temperature

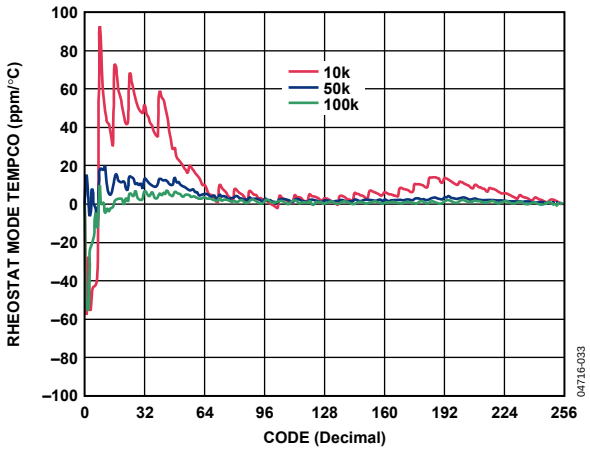


Figure 11. ($\Delta R_{WB}/R_{WB}$)/$\Delta T$ Rheostat Mode Tempco

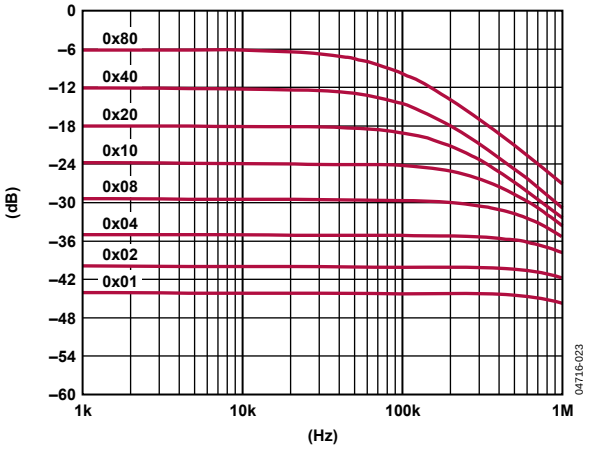


Figure 14. 50 kΩ Gain vs. Frequency vs. Code

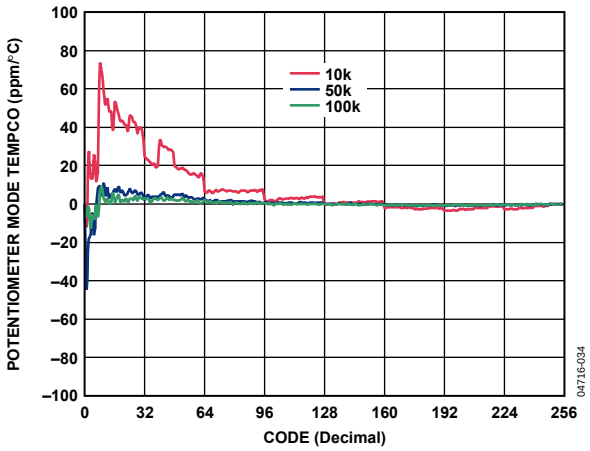


Figure 12. ($\Delta V_{WB}/V_{WB}$)/$\Delta T$ Potentiometer Mode Tempco

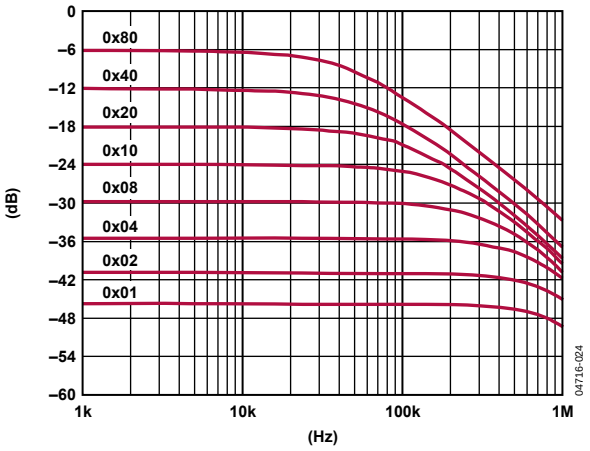


Figure 15. 100 kΩ Gain vs. Frequency vs. Code

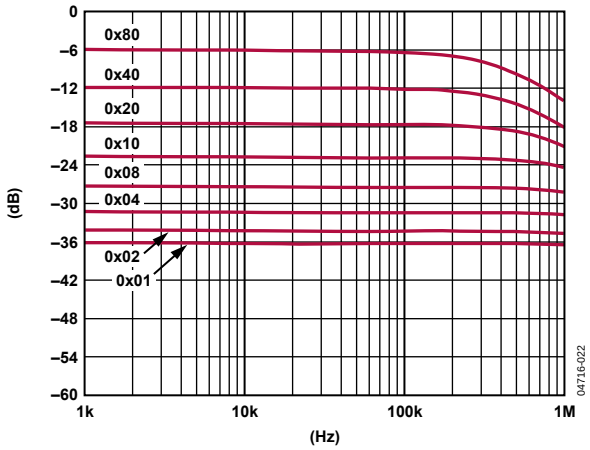


Figure 13. 10 kΩ Gain vs. Frequency vs. Code

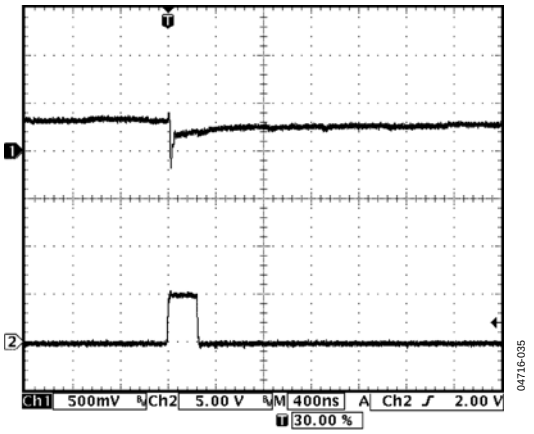


Figure 16. Midscale Transition Glitch

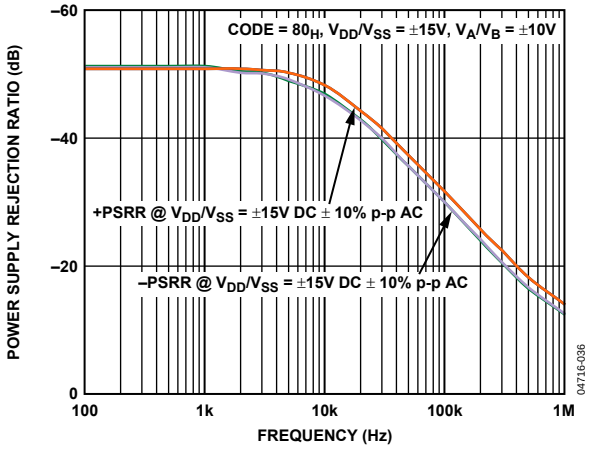


Figure 17. Power Supply Rejection vs. Frequency

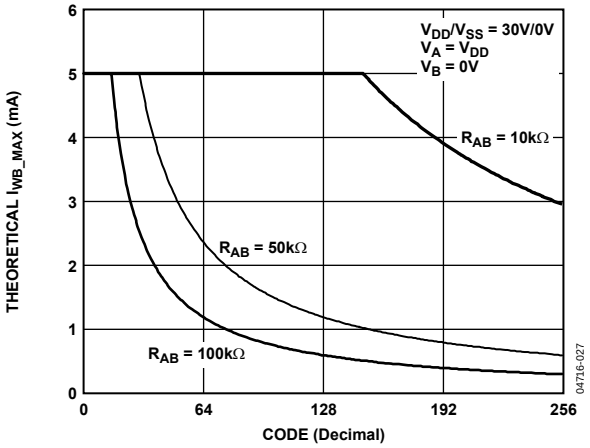


Figure 20. Theoretical Maximum Current vs. Code

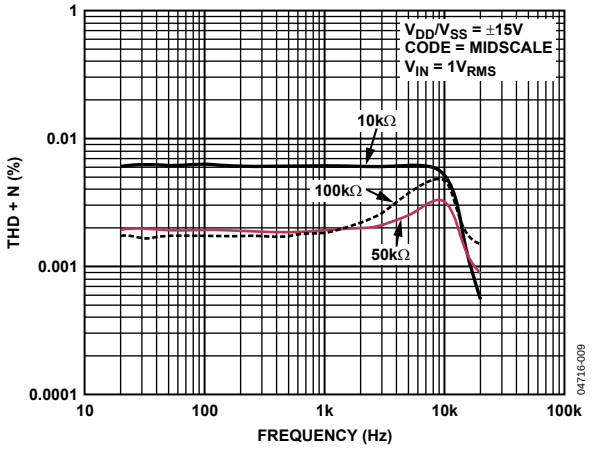


Figure 18. Total Harmonic Distortion Plus Noise vs. Frequency

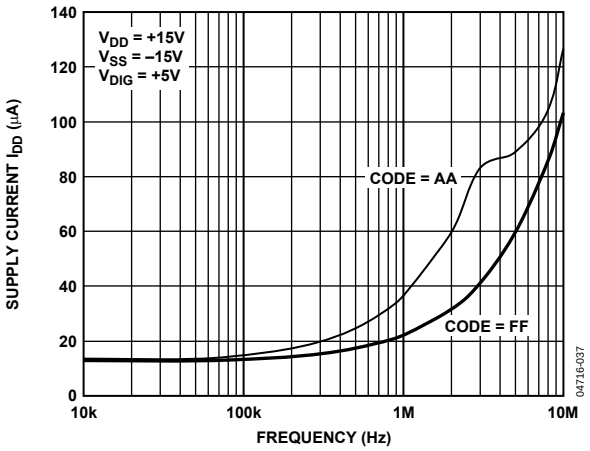


Figure 21. Supply Current $I_{DD}$ vs. Frequency

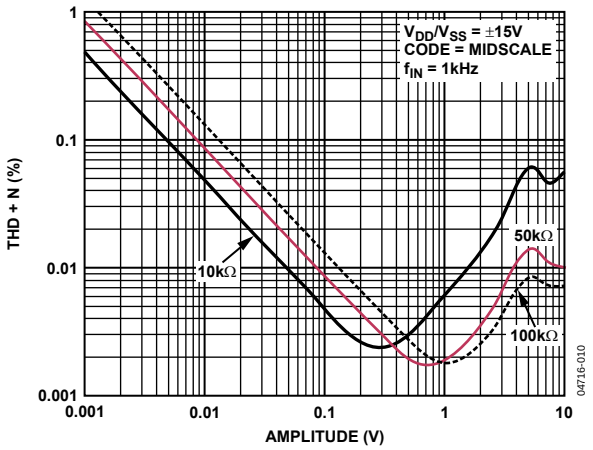


Figure 19. Total Harmonic Distortion Plus Noise vs. Amplitude

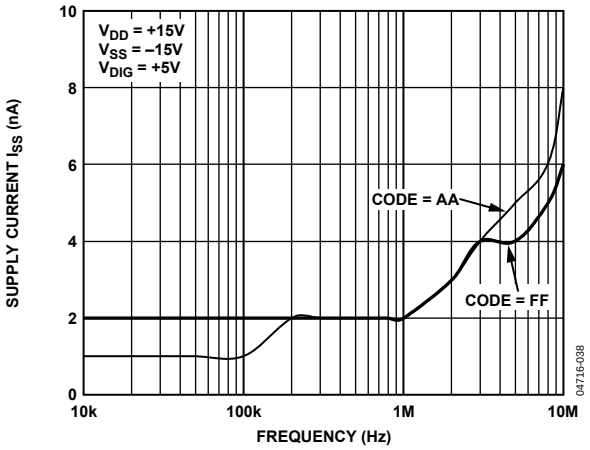


Figure 22. Supply Current $I_{SS}$ vs. Frequency

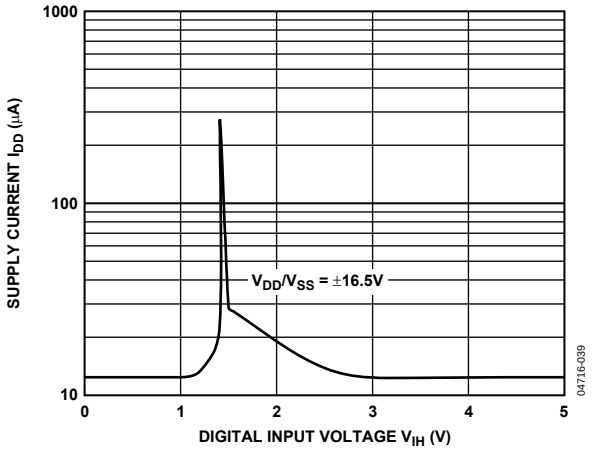


Figure 23. Supply Current vs. Digital Input Voltage

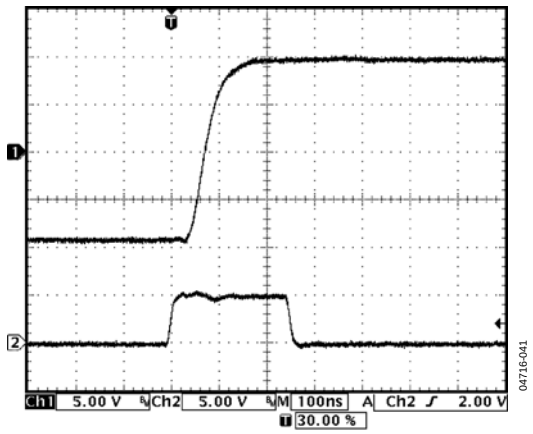


Figure 25. Large Signal Settling Time, Code = 0x00 to 0xFF

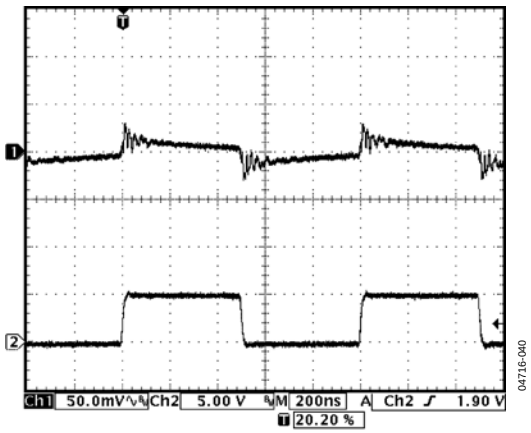


Figure 24. Digital Feedthrough

# THEORY OF OPERATION

## PROGRAMMING THE VARIABLE RESISTOR

### *Rheostat Operation*

The part operates in the rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating or tied to the W terminal as shown in Figure 26.

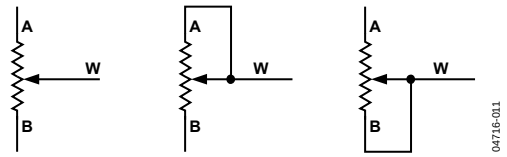


*Figure 26. Rheostat Mode Configuration*

The nominal resistance between Terminal A and Terminal B, $R_{AB}$, is available in 10 kΩ, 50 kΩ, and 100 kΩ with ±30% tolerance and has 256 tap points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Figure 27 shows a simplified RDAC structure.

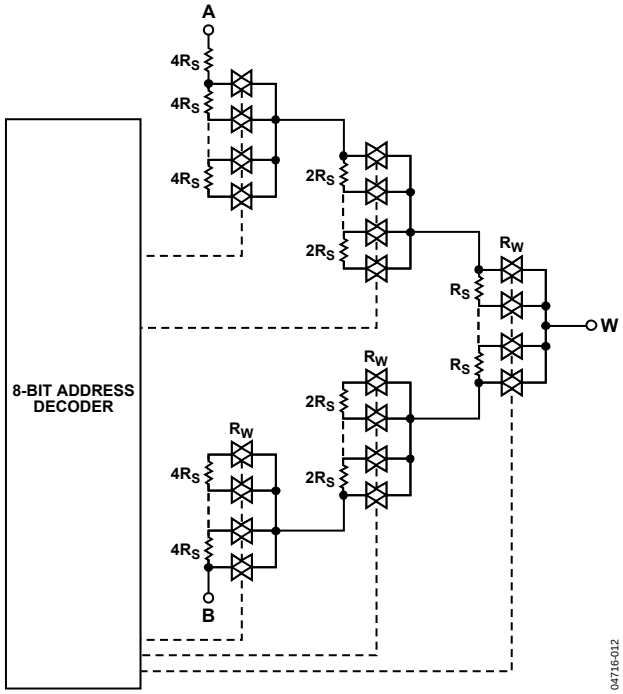


*Figure 27. AD5290 Simplified RDAC Circuit ($R_S$ = Step Resistor, $R_W$ = Wiper Resistor)*

In order to achieve optimum cost performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5290 employs a 3-stage segmentation approach as shown in Figure 27. As a result, the general equation determining the digitally programmed output resistance between the W terminal and B terminal is as follows:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 3 \times R_W \quad (1)$$

where:
$D$ is the decimal equivalent of the binary code loaded in the 8-bit RDAC register from 0 to 255.
$R_{AB}$ is the end-to-end resistance.
$R_W$ is one of the wiper resistances contributed by the on resistance of an internal switch.

The AD5290 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from $V_{DD}$. The wiper resistance, RW, is a function of $V_{DD}$ and temperature. Contrary to the temperature coefficient of the $R_{AB}$, which is only 35 ppm/°C, the temperature coefficient of the wiper resistance is significantly higher because the wiper resistance doubles from 25°C to 125°C. As a result, the user must take into consideration the contribution of RW on the desirable resistance. On the other hand, the wiper resistance is insensitive to the tap point potential. As a result, RW remains relatively flat at a given $V_{DD}$ and temperature at various codes.

Assuming that an ideal 10 kΩ part is used, the wiper's first connection starts at the B terminal for the programming code of 0x00 where SWB is closed. The minimum resistance between Terminal W and Terminal B is, therefore, generally 150 Ω. The second connection is the first tap point, which corresponds to 189 Ω ($R_{WB}$ = 1/256 × $R_{AB}$ + 3$R_W$ = 39 Ω + 150 Ω) for code 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,110 Ω.

In the zero-scale condition, a finite total wiper resistance of 150 Ω is present. Regardless of which setting the part is operating in, care should be taken to limit the current between the A terminal to B terminal, W terminal to A terminal, and W terminal to B terminal, to the maximum dc current of 5 mA or pulse current of 20 mA. Otherwise, degradation, or possible destruction of the internal switch contact, can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, $R_{WA}$. $R_{WA}$ starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equation for this operation is as follows:

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 3 \times R_W \quad (2)$$

## PROGRAMMING THE POTENTIOMETER DIVIDER

### *Voltage Output Operation*

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A proportional to the input voltage at A to B. Unlike the polarity of $V_{DD}$ to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

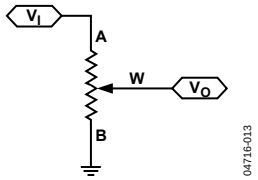


*Figure 28. Potentiometer Mode Configuration*

If ignoring the effect of the wiper resistance for simplicity, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 1 LSB less than 30 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B, divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at $V_W$ with respect to ground for any valid input voltage applied to Terminal A and Terminal B is as follows:

$$V_W(D) = \frac{D}{256} \times V_A + \frac{256 - D}{256} \times V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors $R_{WA}$ and $R_{WB}$ and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

## 3-WIRE SERIAL BUS DIGITAL INTERFACE

The AD5290 contains a 3-wire digital interface ($\overline{CS}$, CLK, and SDI). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Table 4. The positive edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge.

The data setup and data hold times in the Specifications section determine the valid timing requirements. The AD5290 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

## DAISY CHAIN OPERATION

SDO shifts out the SDI content in the previous frame; thus it can be used for daisy-chaining multiple devices. The SDO pin contains an open drain N-Ch MOSFET and requires a pull-up resistor if the SDO function is used. Users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO to SDI interface can induce time delay to the subsequent devices.

For example, in Figure 29, if two AD5290 devices are daisy-chained, a total of 16 bits of data are required for each operation. The first set of eight bits goes to U2, and the second set of eight bits goes to U1. The $\overline{CS}$ should be kept low until all 16 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.

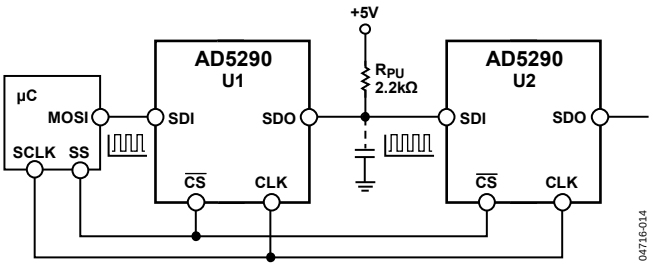


*Figure 29. Daisy Chain Configuration*

## ESD PROTECTION

All digital inputs are protected with a series input resistor and a Zener ESD structure, as shown in Figure 30. These structures apply to digital input pins, Pin $\overline{CS}$, Pin CLK, Pin SDI, and Pin SDO.

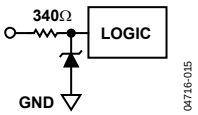


*Figure 30. Equivalent ESD Protection Circuit*

All analog terminals are also protected by Zener ESD protection diodes, as shown in Figure 31.

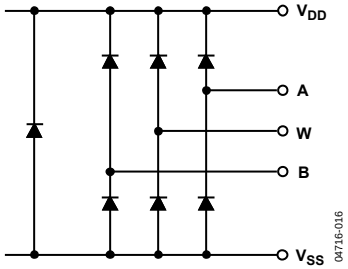


*Figure 31. Equivalent ESD Protection Analog Pins*

## TERMINAL VOLTAGE OPERATING RANGE

The AD5290 $V_{DD}$ and $V_{SS}$ power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. The AD5290 can operate in single supply from +4.5 V to +33 V or dual supply from ±4.5 V to ±16.5 V. The AD5290 is functional at low supply voltages such as 4.5 V, but the performance parameters are not guaranteed.

The voltages present on Terminal A, Terminal B, and Terminal W that are more positive than $V_{DD}$ or more negative than $V_{SS}$ are clamped by the internal forward-biased diodes (Figure 31).

## POWER-UP AND POWER-DOWN SEQUENCES

Because of the ESD protection diodes that limit the voltage compliance at Terminal A, Terminal B, and Terminal W (Figure 31), it is important to power $V_{DD}/V_{SS}$ before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diodes are forward-biased such that $V_{DD}/V_{SS}$ are powered unintentionally and affect the system. Similarly, $V_{DD}/V_{SS}$ should be powered down last. The ideal power-up sequence is as follows: GND, $V_{DD}$, $V_{SS}$, digital inputs, and $V_A/V_B/V_W$. The order of powering $V_A$, $V_B$, $V_W$, and the digital inputs is not important, as long as they are powered after $V_{DD}/V_{SS}$.

## LAYOUT AND POWER SUPPLY BIASING

It is good practice to use a compact, minimum lead-length layout design. The leads to the input should be as direct as possible, with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low equivalent series resistance (ESR), 1 µF to 10 µF tantalum or electrolytic capacitors, should be applied at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 32 illustrates the basic supply-bypassing configuration for the AD5290.

The ground pin of the AD5290 is a digital ground reference. To minimize the digital ground bounce, the AD5290 digital ground terminal should be joined remotely to the analog ground (Figure 32).

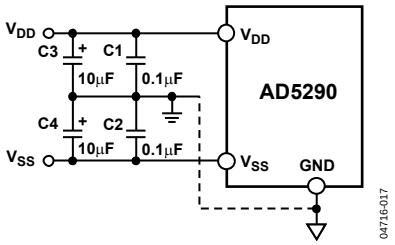


*Figure 32. Power Supply Bypassing*

# APPLICATIONS

## HIGH VOLTAGE DAC

AD5290 can be configured as a high voltage DAC, with output voltage as high as 30 V. The circuit is shown in Figure 33. The output is as follows:

$$V_O(D) = \frac{D}{256} \times [1.2\ \text{V} \times (1 + \frac{R_2}{R_1})] \quad (4)$$

where $D$ is the decimal code from 0 to 255.

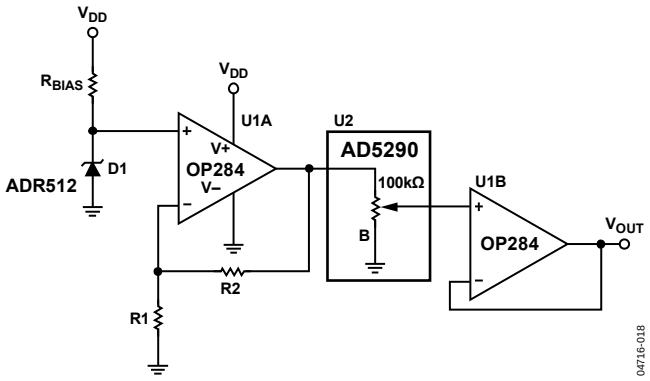


*Figure 33. High Voltage DAC*

## PROGRAMMABLE POWER SUPPLY

With a boost regulator, such as ADP1612, AD5290 can be used as the variable resistor at the regulator's FB pin to provide the programmable power supply (Figure 34). The output is as follows:

$$V_O = 1.23\ \text{V} \times [1 + \frac{(D/256) - R_{AB}}{R_2}] \quad (5)$$

AD5290 devices $V_{DD}$ is derived from the output. Initially, L1 acts as a short, and $V_{DD}$ is one diode voltage drop below +5 V. The output slowly establishes the final value.

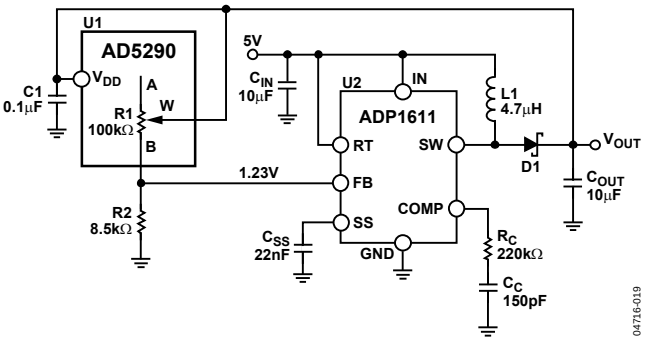


*Figure 34. Programmable Power Supply*

## AUDIO VOLUME CONTROL

Because of its good THD performance and high voltage capability, AD5290 can be used as a digital volume control. If AD5290 is used directly as an audio attenuator or gain amplifier, a large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the $\overline{CS}$ line to delay the device update until the audio signal crosses the window. Since the input signal can operate on top of any dc level rather than absolute zero volt level, zero-crossing in this case means the signal is ac-coupled, and the dc offset level is the signal zero reference point.

The configuration to reduce zipper noise (Figure 35) and the results of using this configuration are shown in Figure 36. The input is ac-coupled by C1 and attenuated down before feeding into the window comparator formed by U2, U3, and U4B (Figure 35). $U_6$ is used to establish the signal zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or 0.005 V window) in this example. This output is AND'ed with the chip select signal such that the AD5290 updates whenever the signal crosses the window. To avoid a constant update of the device, the chip select signal should be programmed as two pulses, rather than as one shown in Figure 36.

In Figure 35, the lower trace shows that the volume level changes from a quarter-scale to full-scale when a signal change occurs near the zero-crossing window.

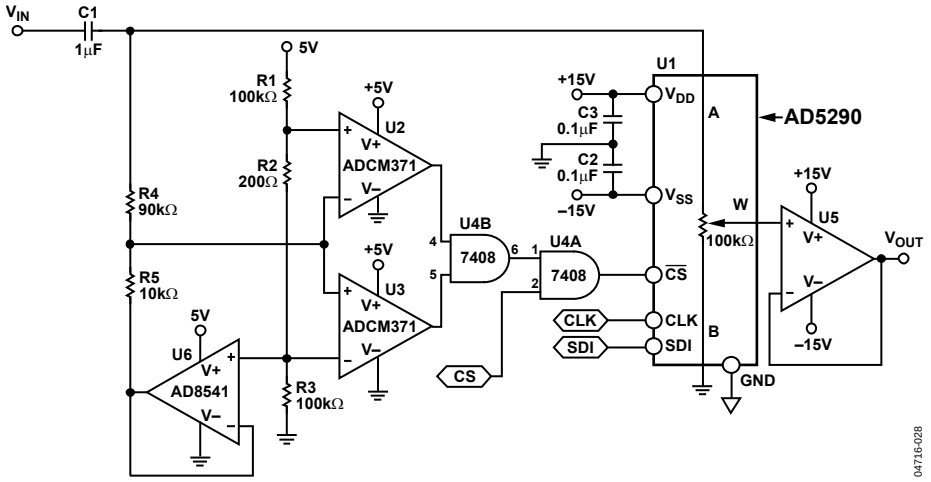


*Figure 35. Audio Volume Control with Zipper Noise Reduction*

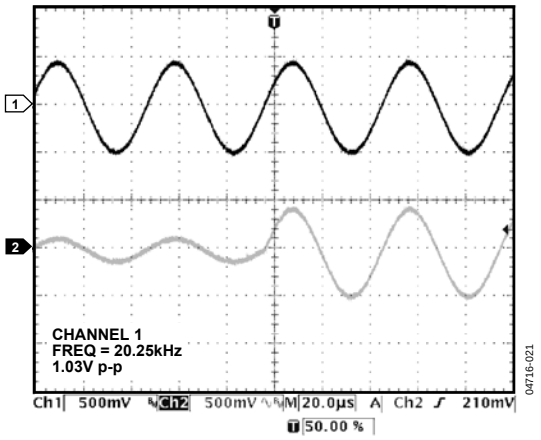


*Figure 36. Input (Trace 1) and Output (Trace 2) of the Circuit in Figure 35*
*(The Command of Volume Change May Occur at Any Time, but the Level Change Occurs Only Near the Zero-Crossing Window)*

# OUTLINE DIMENSIONS

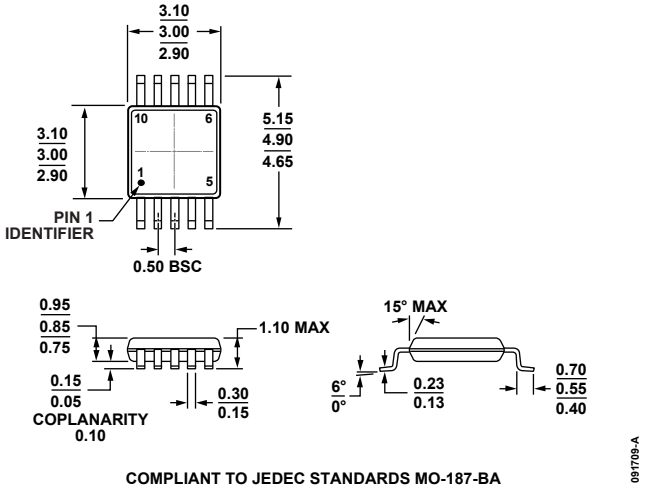


*Figure 37. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | $R_{AB}$ (kΩ) | Temperature Range | Package Description | Package Option | Marking Code |
|---|---|---|---|---|---|
| AD5290YRMZ10 | 10 | −40°C to +125°C | 10-Lead MSOP | RM-10 | D4U |
| AD5290YRMZ10-R7 | 10 | −40°C to +125°C | 10-Lead MSOP | RM-10 | D4U |
| AD5290YRMZ50 | 50 | −40°C to +125°C | 10-Lead MSOP | RM-10 | D4T |
| AD5290YRMZ50-R7 | 50 | −40°C to +125°C | 10-Lead MSOP | RM-10 | D4T |
| AD5290YRMZ100 | 100 | −40°C to +125°C | 10-Lead MSOP | RM-10 | D4V |
| AD5290YRMZ100-R7 | 100 | −40°C to +125°C | 10-Lead MSOP | RM-10 | D4V |
| EVAL-AD5290DBZ | 10 | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.