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REVISION HISTORY

7/09—Rev. B to Rev. C

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Updated Outline Dimensions, RU-14 ... 25
Changes to Ordering Guide ... 26

8/07—Rev. A to Rev. B

Updated Operating Temperature Range Throughout ... 1
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Added the Thermal Resistance Section ... 5
Changes to the Ordering Guide ... 26

11/05—Rev. 0 to Rev. A

Updated Format ... Universal
Updated Outline Dimensions ... 26
Changes to Ordering Guide ... 27

10/02—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = +15 V, V_{SS} = 0 V or V_{DD} = +5 V, V_{SS} = −5 V; V_{LOGIC} = 5 V, V_A = +V_{DD}, V_B = 0 V; −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS–RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	−1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	−1	±1/4	+1	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	$V_{AB} = V_{DD}$, wiper = no connect		30		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 3 V or 5 V		60	150	Ω
DC CHARACTERISTICS–POTENTIOMETER DIVIDER MODE (specifications apply to all VRs)						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		−1	±1/4	+1	LSB
Differential Nonlinearity[4]	DNL		−1	±1/4	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = 0x80		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, B[6]	C_A, C_B	f = 5 MHz, measured to GND, Code = 0x80		25		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, Code = 0x80		55		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
Shutdown Current	I_{SHDN}				5	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		0.7 × V_L		V_L + 0.5	V
Input Logic Low	V_{IL}		0		0.3 × V_L	V
Output Logic High (O_1, O_2)	V_{IH}		4.9			V
Output Logic Low (O_1, O_2)	V_{IL}				0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_{LOGIC}		2.7		V_{DD}	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	4.5		16.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±4.5		±5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V			60	µA
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		0.1	1	µA
Negative Supply Current	I_{SS}			0.1	1	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = −5 V		0.2	0.3	mW
Power Supply Sensitivity	PSS			0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[6, 8, 9]						
Bandwidth −3 dB	BW_20K	R_{AB} = 20 kΩ, Code = 0x80		310		kHz
	BW_50K	R_{AB} = 50 kΩ, Code = 0x80		150		kHz
	BW_200K	R_{AB} = 200 kΩ, Code = 0x80		35		kHz

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Total Harmonic Distortion	THD_W	V_A = 1 V rms, R_{AB} = 20 kΩ V_B = 0 V dc, f = 1 kHz		0.014		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 5 V, ±1 LSB error band		5		µs
Crosstalk	CT	$V_A = V_{DD}$, V_B = 0 V, measure V_{W1} with adjacent RDAC making full-scale code change		15		nV-s
Analog Crosstalk	CTA	Measure V_{W1} with V_{W2} = 5 V p-p @ f = 10 kHz		−62		dB
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 20 kΩ, f = 1 kHz		18		nV/√Hz
INTERFACE TIMING CHARACTERISTICS (applies to all parts)[6, 10, 11]						
SCL Clock Frequency	f_{SCL}		0		400	kHz
t_{BUF} Bus Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD:STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU:STA}$ Setup Time for Start Condition	t_5		0.6			µs
$t_{HD:DAT}$ Data Hold Time	t_6		0		0.9	µs
$t_{SU:DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU:STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

[1] Typicals represent average readings at 25°C, V_{DD} = +5 V, V_{SS} = −5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Wiper Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[9] All dynamic characteristics use V_{DD} = 5 V.
[10] See timing diagram (Figure 3) for location of measured values.
[11] Standard I²C mode operation is guaranteed by design.

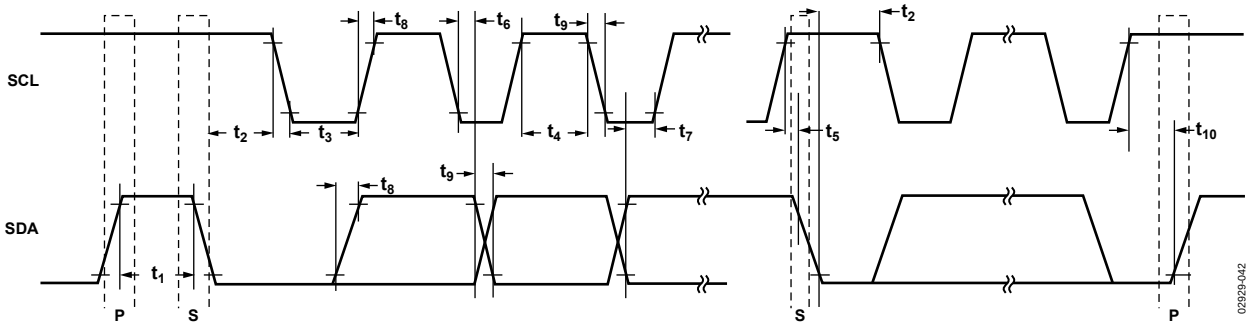

Figure 3. Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +16.5 V
V_{SS} to GND	0 V to −7 V
V_{DD} to V_{SS}	16.5 V
V_A, V_B, V_W to GND	V_{SS} to V_{DD}
A_X to B_X, A_X to W_X, B_X to W_X	
Intermittent[1]	±20 mA
Continuous	±5 mA
V_{LOGIC} to GND	0 V to 7 V
Output Voltage to GND	0 V to 7 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec

[1] Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Package power dissipation = $(T_{JMAX} - T_A)/\theta_{JA}$.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
TSSOP-14	206	°C/W
TSSOP-16	150	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

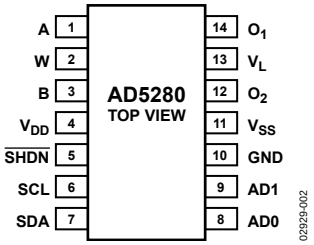

Figure 4. AD5280 Pin Configuration

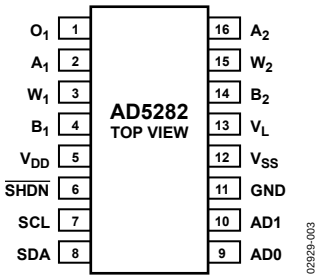

Figure 5. AD5282 Pin Configuration

Table 4. AD5280 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A	Resistor Terminal A.
2	W	Wiper Terminal W.
3	B	Resistor Terminal B.
4	V_{DD}	Positive Power Supply. Specified for operation from 5 V to 15 V (sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
5	$\overline{SHDN}$	Active Low, Asynchronous Connection of Wiper W to Terminal B and Open Circuit of Terminal A. RDAC register contents unchanged. $\overline{SHDN}$ should tie to V_L if not used. Can also be used as a programmable preset in power-up.
6	SCL	Serial Clock Input.
7	SDA	Serial Data Input/Output.
8	AD0	Programmable Address Bit 0 for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
9	AD1	Programmable Address Bit 1 for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
10	GND	Common Ground.
11	V_{SS}	Negative Power Supply. Specified for operation from 0 V to −5 V (sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
12	O_2	Logic Output Terminal O_2.
13	V_L	Logic Supply Voltage. Needs to be less than or equal to V_{DD} and at the same voltage as the digital logic controlling the AD5280.
14	O_1	Logic Output Terminal O_1.

Table 5. AD5282 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	O_1	Logic Output Terminal O_1.
2	A_1	Resistor Terminal A_1.
3	W_1	Wiper Terminal W_1.
4	B_1	Resistor Terminal B_1.
5	V_{DD}	Positive Power Supply. Specified for operation from 5 V to 15 V (sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
6	$\overline{SHDN}$	Active Low, Asynchronous Connection of Wiper W to Terminal B and Open Circuit of Terminal A. RDAC register contents unchanged. $\overline{SHDN}$ should tie to V_L if not used. Can be also used as a programmable preset in power-up.
7	SCL	Serial Clock Input.
8	SDA	Serial Data Input/Output.
9	AD0	Programmable Address Bit 0 for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
10	AD1	Programmable Address Bit 1 for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
11	GND	Common Ground.
12	V_{SS}	Negative Power Supply. Specified for operation from 0 V to −5 V (sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
13	V_L	Logic Supply Voltage. Needs to be less than or equal to V_{DD} and at the same voltage as the digital logic controlling the AD5282.
14	B_2	Resistor Terminal B_2.
15	W_2	Wiper Terminal W_2.
16	A_2	Resistor Terminal A_2.

TYPICAL PERFORMANCE CHARACTERISTICS

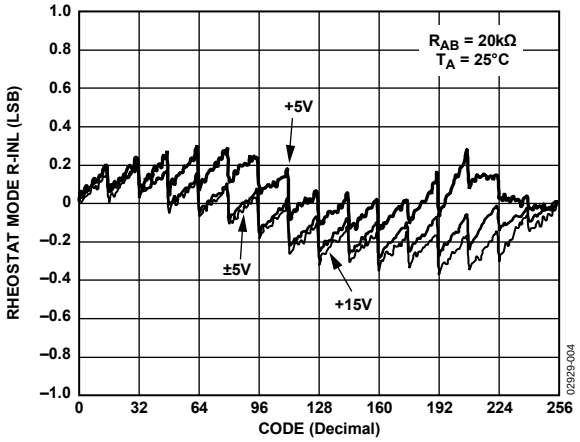

Figure 6. R-INL vs. Code vs. Supply Voltages

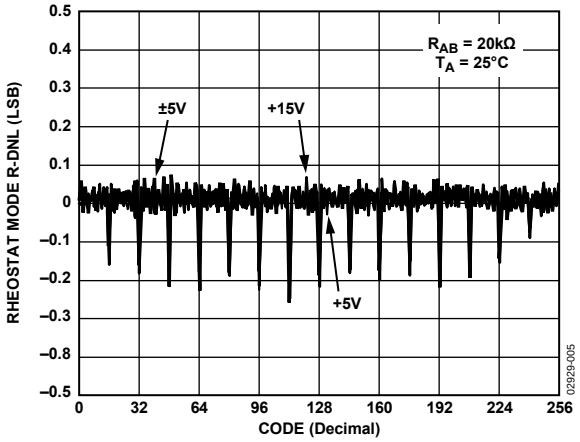

Figure 7. R-DNL vs. Code vs. Supply Voltages

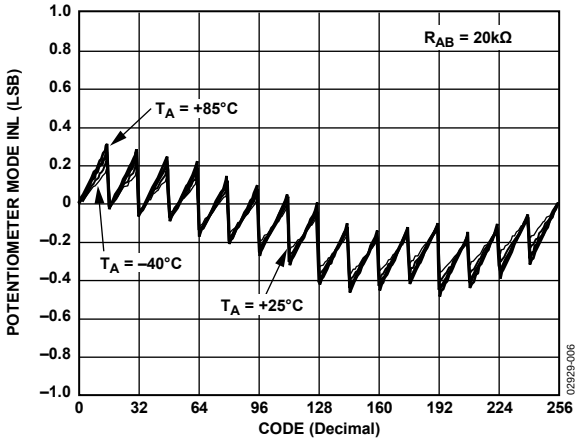

Figure 8. INL vs. Code, V_{DD}/V_{SS} = ±5 V

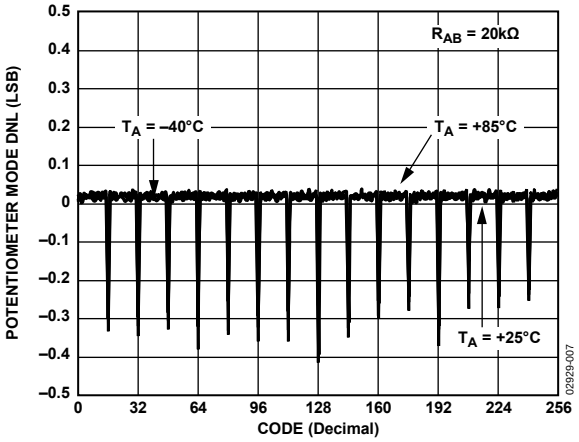

Figure 9. DNL vs. Code, V_{DD}/V_{SS} = ±5 V

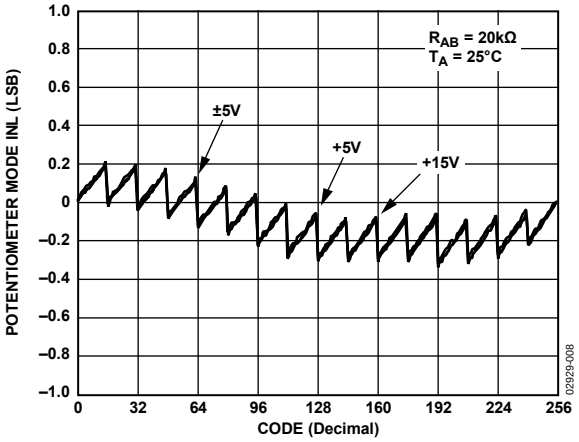

Figure 10. INL vs. Code vs. Supply Voltages

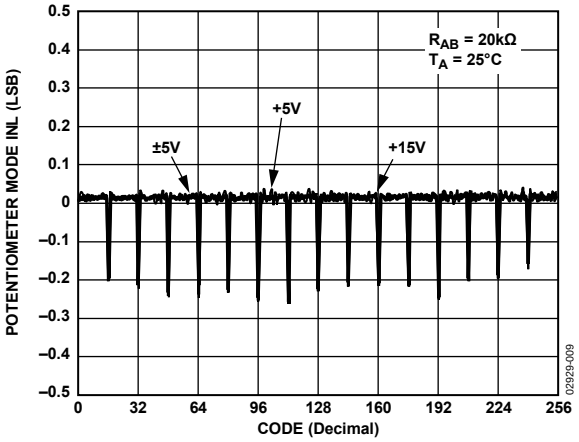

Figure 11. DNL vs. Code vs. Supply Voltages

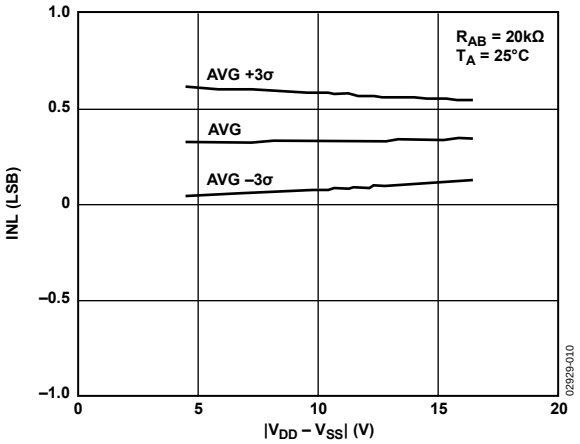

Figure 12. INL Over Supply Voltage

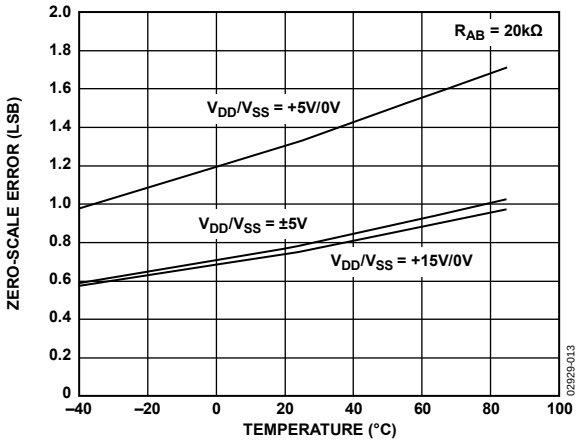

Figure 15. Zero-Scale Error

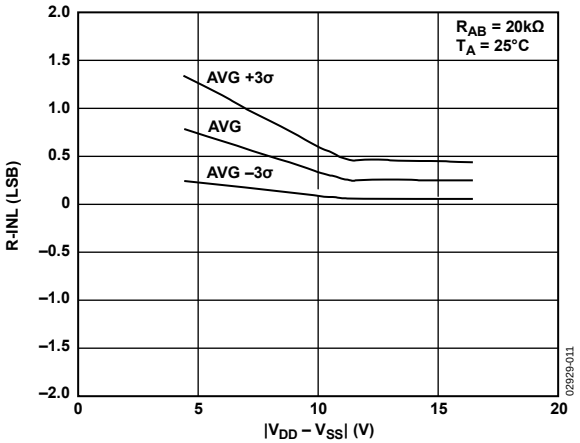

Figure 13. R-INL Over Supply Voltage

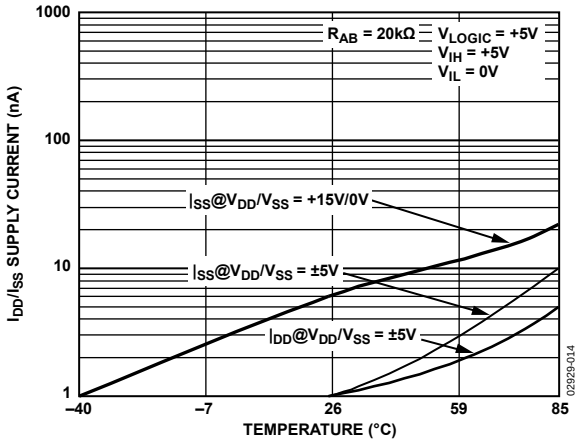

Figure 16. Supply Current vs. Temperature

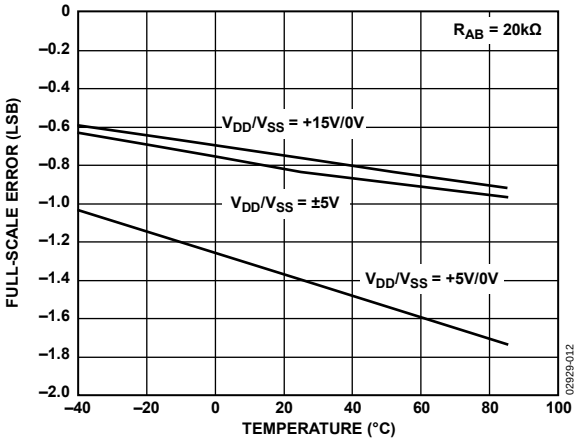

Figure 14. Full-Scale Error

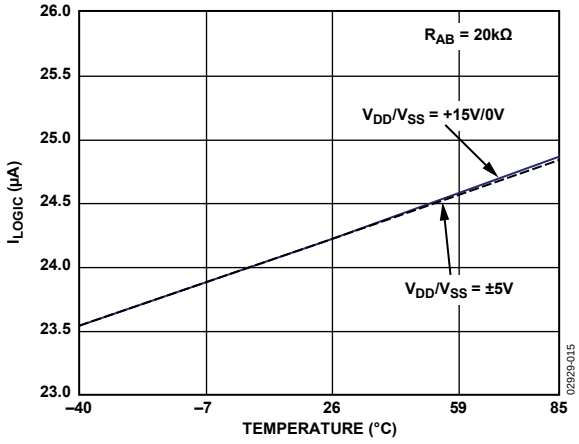

Figure 17. V_{LOGIC} Supply Current vs. Temperature

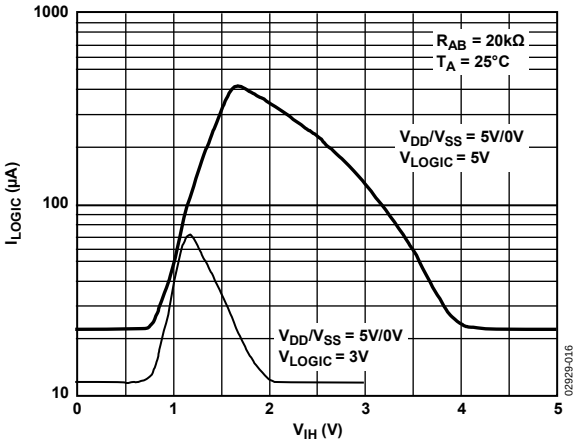

Figure 18. V_{LOGIC} Supply Current vs. Digital Input Voltage

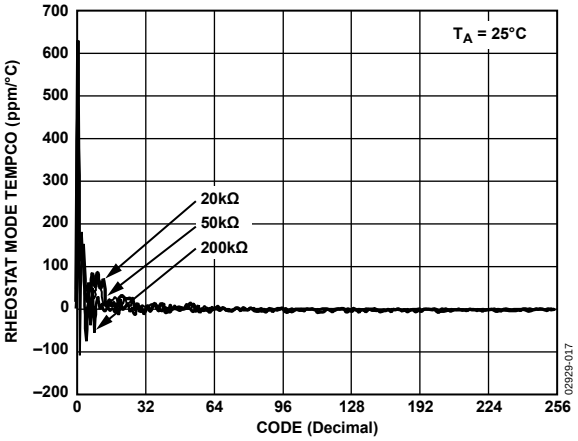

Figure 19. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code, V_{DD}/V_{SS} = ±5 V

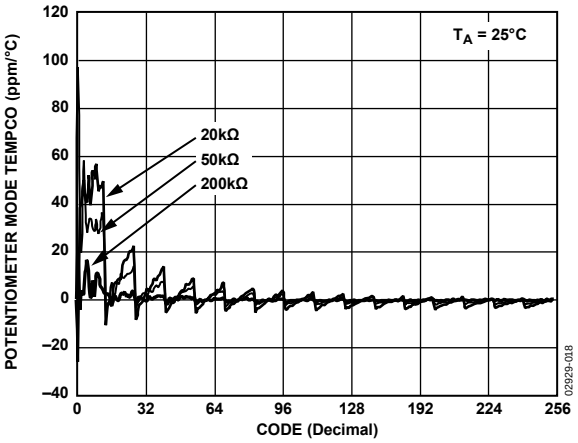

Figure 20. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code, V_{DD}/V_{SS} = ±5 V

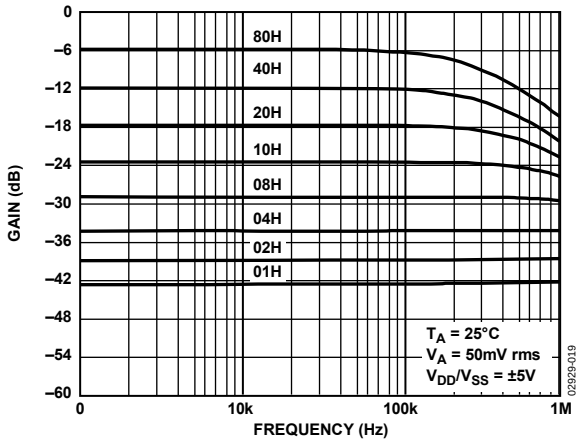

Figure 21. Gain vs. Frequency vs. Code, R_{AB} = 20 kΩ

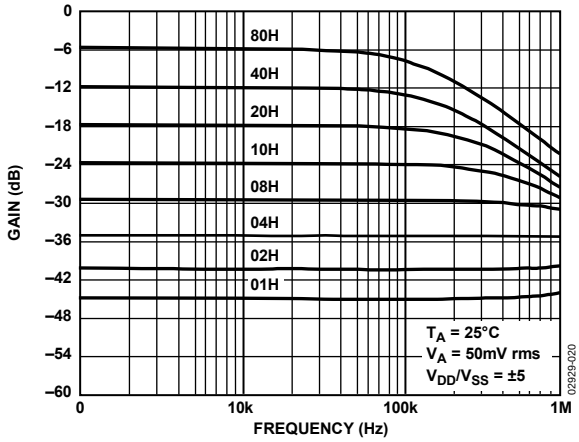

Figure 22. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

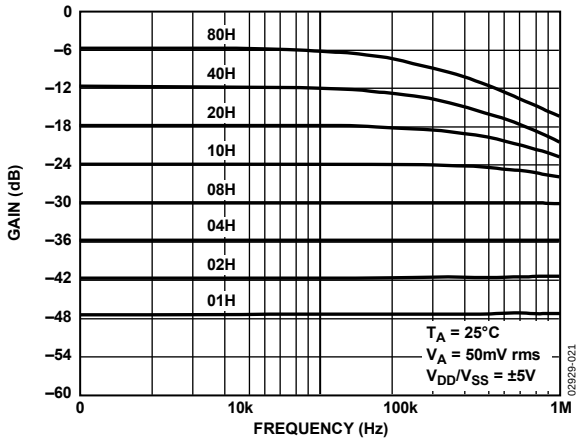

Figure 23. Gain vs. Frequency vs. Code, R_{AB} = 200 kΩ

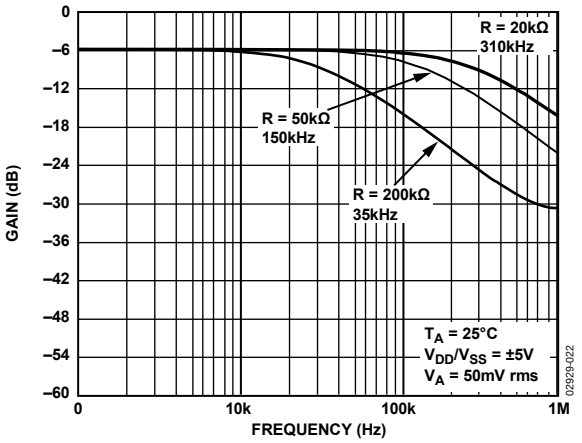

Figure 24. –3 dB Bandwidth

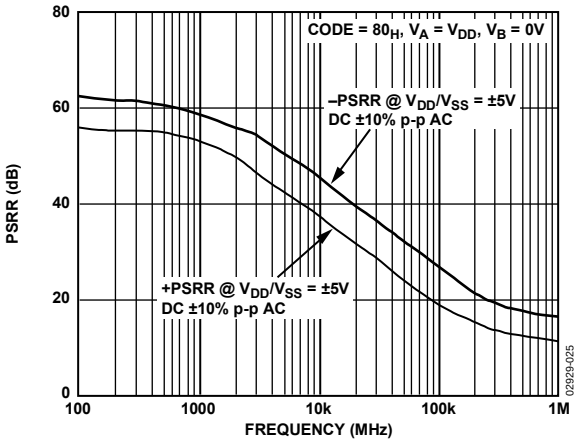

Figure 27. PSRR vs. Frequency

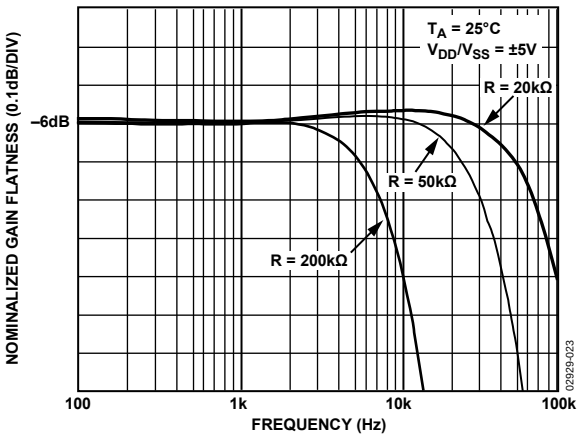

Figure 25. Normalized Gain Flatness vs. Frequency

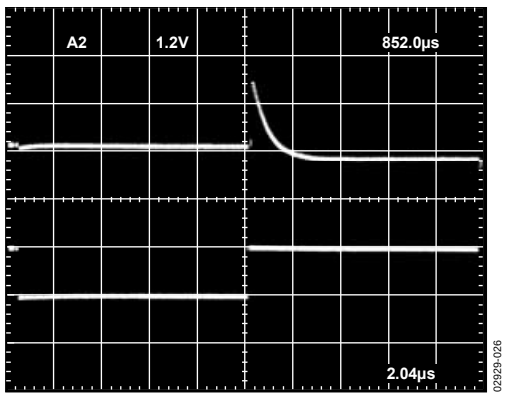

Figure 28. Midscale Glitch Energy Code 0x80 to 0x7F

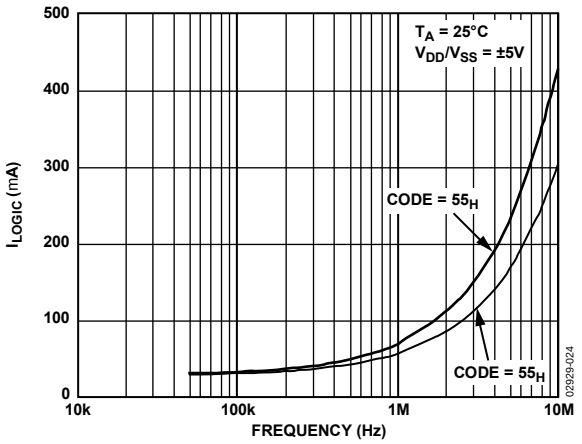

Figure 26. V_{LOGIC} Supply Current vs. Frequency

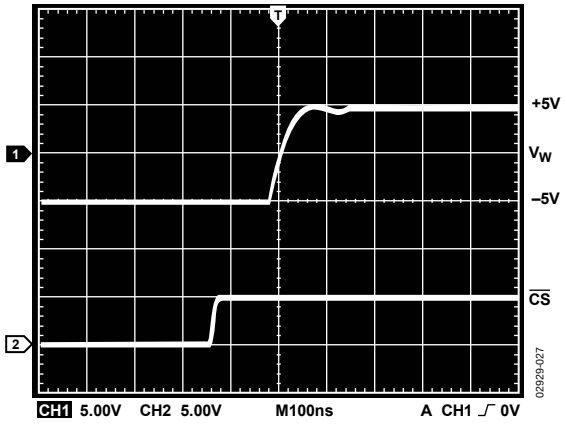

Figure 29. Large Signal Settling Time

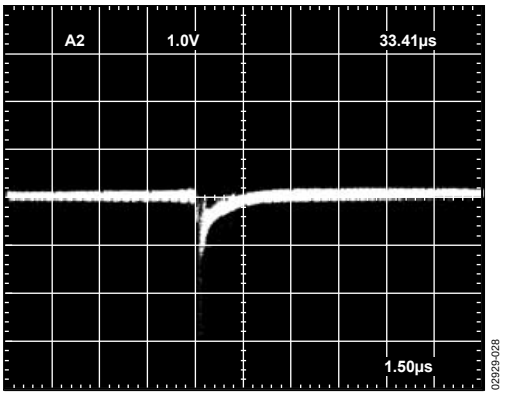

Figure 30. Digital Feedthrough vs. Time

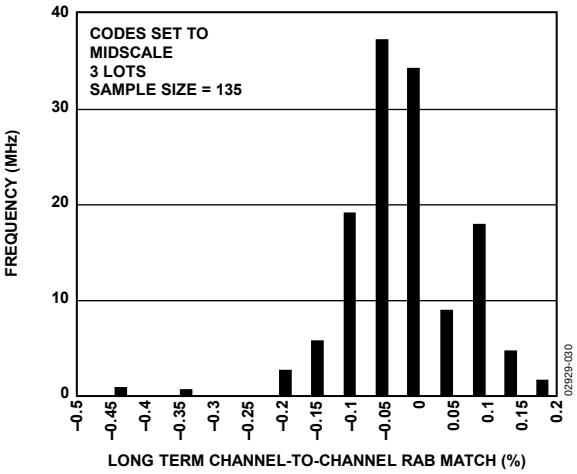

Figure 32. Channel-to-Channel Resistance Matching (AD5282)

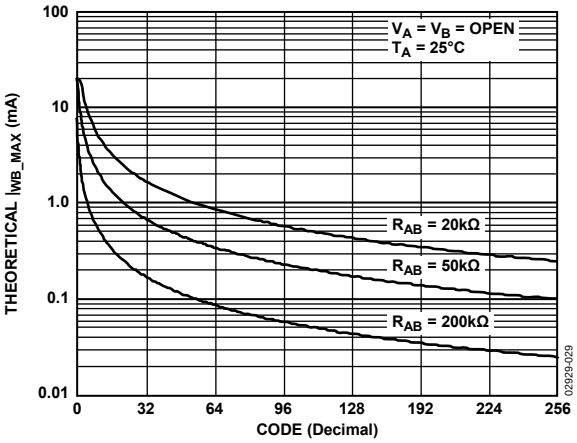

Figure 31. I_{WB_MAX} vs. Code

TEST CIRCUITS

Figure 33 to Figure 43 define the test conditions used in the product specification table.

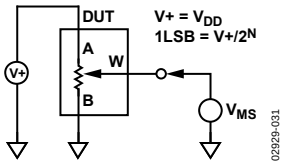

Figure 33. Potentiometer Divider Nonlinearity Error (INL, DNL)

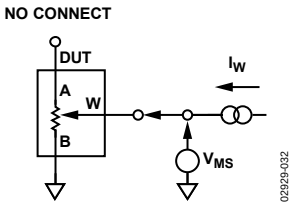

Figure 34. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

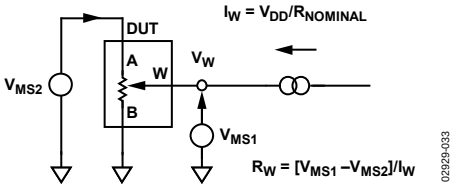

Figure 35. Wiper Resistance

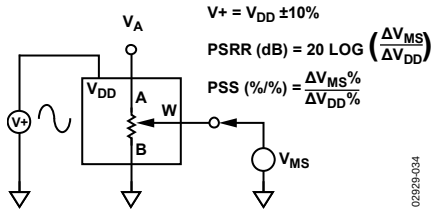

Figure 36. Power Supply Sensitivity (PSS, PSSR)

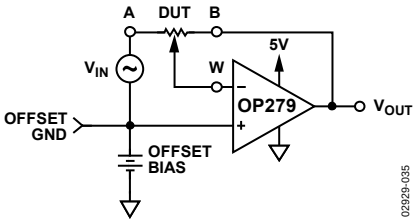

Figure 37. Inverting Gain

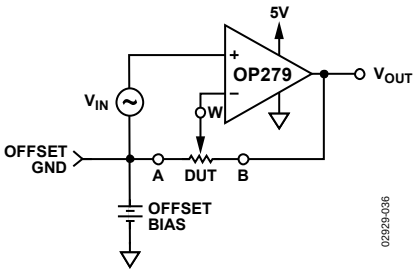

Figure 38. Noninverting Gain

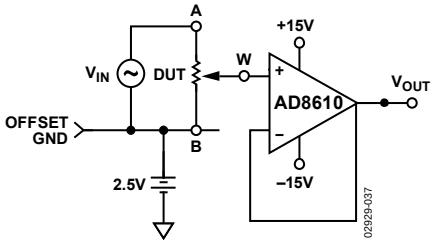

Figure 39. Gain vs. Frequency

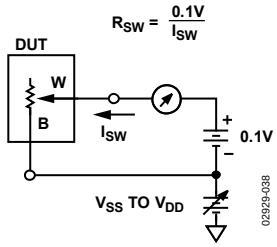

Figure 40. Incremental On Resistance

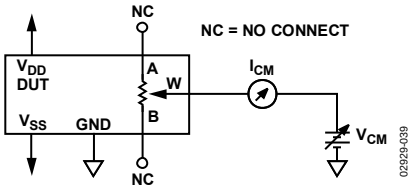

Figure 41. Common-Mode Leakage Current

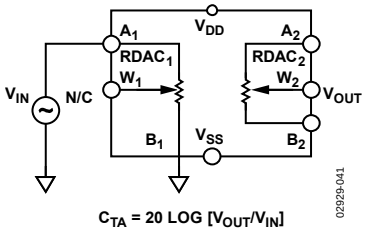

Figure 43. Analog Crosstalk (AD5282 Only)

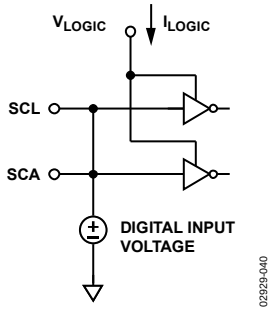

Figure 42. V_{LOGIC} Current vs. Digital Input Voltage

THEORY OF OPERATION

The AD5280/AD5282 are single-channel and dual-channel, 256-position, digitally controlled variable resistors (VRs). To program the VR settings, see the Digital Interface section. Both parts have an internal power-on preset that places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up. Operation of the power-on preset function also depends on the state of the V_L pin.

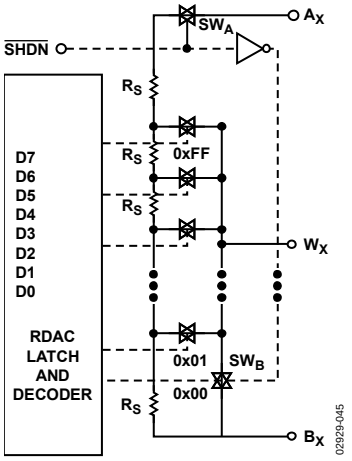

Figure 44. AD5280/AD5282 Equivalent RDAC Circuit

RHEOSTAT OPERATION

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 20 kΩ, 50 kΩ, and 200 kΩ. The final two or three digits of the part number determine the nominal resistance value, for example, 20 kΩ = 20, 50 kΩ = 50, and 200 kΩ = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The eight-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assuming that a 20 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 60 Ω wiper contact resistance, such a connection yields a minimum of 60 Ω resistance between Terminal W and Terminal B.

The second connection is the first tap point that corresponds to 138 Ω (R_{WB} = R_{AB}/256 + R_W = 78 Ω + 60 Ω) for data 0x01. The third connection is the next tap point representing 216 Ω (78 × 2 + 60) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19,982 Ω (R_{AB} – 1 LSB + R_W). Figure 46 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string is not accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the nominal end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.
Note that in the zero-scale condition, a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

As in the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

The typical distribution of the nominal resistance, R_{AB}, from channel to channel matches within ±1%. Device-to-device matching is process lot dependent, and it is possible to have a ±30% variation. Because the resistance element is processed in thin film technology, the change in R_{AB} with temperature is very small (30 ppm/°C).

POTENTIOMETER OPERATION

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A to be proportional to the input voltage at A to B. Unlike the polarity of V_{DD} – V_{SS}, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity, provided that V_{SS} is powered by a negative supply.

If the effect of the wiper resistance for approximation is ignored, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper to B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across A to B divided by the 256 positions of the potentiometer divider. Because the AD5280/AD5282 can be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any valid

input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \quad (3)$$

For a more accurate calculation that includes the effect of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in divider mode results in a more accurate operation over temperature. Unlike rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not on the absolute values; therefore, the temperature drift reduces to 5 ppm/°C.

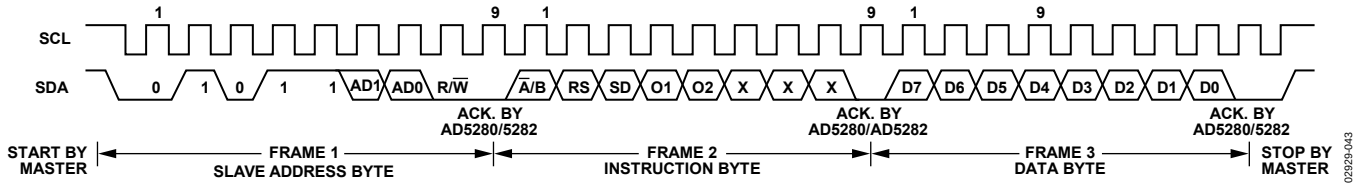

Figure 45. Writing to the RDAC Register

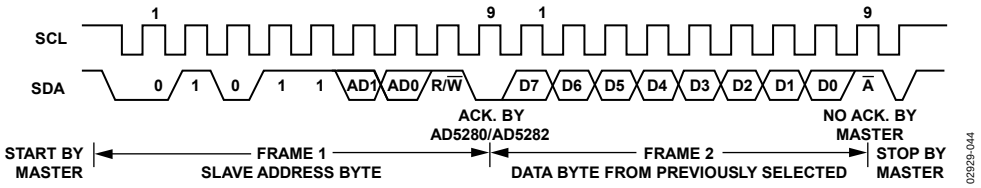

Figure 46. Reading Data from a Previously Selected RDAC Register in Write Mode

Table 6. Serial Format of Data Accepted from the I²C Bus

S	0	1	0	1	1	AD1	AD0	R/W	A	A/B	RS	SD	O1	O2	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

where:

Abbreviation	Equals
S	Start condition
P	Stop condition
A	Acknowledge
X	Don't care
AD1, AD0	Package pin programmable address bits
R/$\overline{W}$	Read enable at high and write enable at low
$\overline{A}$/B	RDAC subaddress select; 0 = RDAC1 and 1 = RDAC2
RS	Midscale reset, active high (only affects selected channel)
SD	Shutdown; same as $\overline{SHDN}$ pin operation except inverse logic (only affects selected channel)
O_2, O_1	Output logic pin latched values; default Logic 0
D7, D6, D5, D4, D3, D2, D1, D0	Data bits

DIGITAL INTERFACE

2-WIRE SERIAL BUS

The AD5280/AD5282 are controlled via an I²C-compatible serial bus. The RDACs are connected to this bus as slave devices. As shown in Figure 45, Figure 46, and Table 6, the first byte of the AD5280/AD5282 is a slave address byte. It has a 7-bit slave address and an R/$\overline{W}$ bit.

The 5 MSBs are 01011, and the two bits that follow are determined by the state of the AD0 pin and the AD1 pin of the device. AD0 and AD1 allow the user to place up to four of the I²C-compatible devices on one bus. The 2-wire I²C serial bus protocol operates as follows.

The master initiates data transfer by establishing a start condition, which happens when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 45). The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master writes to the slave device.

A write operation contains one instruction byte more than a read operation. Such an instruction byte in write mode follows the slave address byte. The most significant bit (MSB) of the instruction byte labeled $\overline{A}$/B is the RDAC subaddress select. A low selects RDAC1 and a high selects RDAC2 for the dual channel AD5282. Set $\overline{A}$/B low for the AD5280.

RS, the second MSB, is the midscale reset. A logic high on this bit moves the wiper of a selected channel to the center tap where RWA = RWB. This feature effectively writes over the contents of the register and thus, when taken out of reset mode, the RDAC remains at midscale.

SD, the third MSB, is a shutdown bit. A logic high causes the selected channel to open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. This SD bit serves the same function as the $\overline{SHDN}$ pin except that the $\overline{SHDN}$ pin reacts to active low. Also, the $\overline{SHDN}$ pin affects both channels (AD5282) as opposed to the SD bit, which affects only the channel that is being written to. Note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC.

The following two bits are O_1 and O_2. They are extra programmable logic outputs that can be used to drive other digital loads, logic gates, LED drivers, analog switches, and so on. The three LSBs are don't care bits (see Figure 45).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 45).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 46).

When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition (see Figure 45). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 46).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. During the write cycle, each data byte updates the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output updates after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte updates the output of the selected slave device. If different instructions are needed, the write mode has to start with a new slave address, instruction, and data byte again. Similarly, a repeated read function of RDAC is also allowed.

READBACK RDAC VALUE

The AD5280/AD5282 allow the user to read back the RDAC values in read mode. However, for the dual-channel AD5282, the channel of interest is the one that is previously selected in the write mode. When users need to read the RDAC values of both channels in the AD5282, they can program the first subaddress in write mode and then change to read mode to read the first channel value. After that, they can change back to write mode with the second subaddress and read the second channel value in read mode again. It is not necessary for users to issue the Frame 3 data byte in write mode for subsequent readback operation. Users should refer to Figure 45 and Figure 46 for the programming format.

ADDITIONAL PROGRAMMABLE LOGIC OUTPUT

The AD5280/AD5282 feature additional programmable logic outputs, O_1 and O_2, which can be used to drive a digital load, analog switches, and logic gates. O_1 and O_2 default to Logic 0. The logic states of O_1 and O_2 can be programmed in Frame 2 under write mode (see Figure 45). These logic outputs have adequate current driving capability to sink/source milliamperes of load.

Users can also activate O_1 and O_2 in three ways without affecting the wiper settings by programming as follows:

- Perform start, slave address, acknowledge, and instruction bytes with O_1 and O_2 specified, acknowledge, stop.
- Complete the write cycle with stop, then start, slave address byte, acknowledge, instruction byte with O_1 and O_2 specified, acknowledge, stop.
- Not complete the write cycle by not issuing the stop, then start, slave address byte, acknowledge, instruction byte with O_1 and O_2 specified, acknowledge, stop.

SELF-CONTAINED SHUTDOWN FUNCTION AND PROGRAMMABLE PRESET

Shutdown can be activated by strobing the $\overline{\text{SHDN}}$ pin or programming the SD bit in the write mode instruction byte. As shown in Figure 44, when shutdown is asserted, the AD5280/AD5282 open SW_A to let the A terminal float and short the W terminal to the B terminal. The AD5280/AD5282 consume negligible power during shutdown mode, resuming the previous setting once the $\overline{\text{SHDN}}$ pin is released.

In addition, shutdown can be implemented with the device digital output as shown in Figure 47. In this configuration, the device is shut down during power-up, but the user is allowed to program the device at any preset levels. When it is done, the user programs O_1 high with the valid coding and the device exits from shutdown and responds to the new setting. This self-contained shutdown function allows absolute shutdown during power-up, which is crucial in hazardous environments, without adding extra components. Also, the sleep mode programming feature during shutdown allows the AD5280/AD5282 to have a programmable preset at any level, a solution that can be as effective as using other high cost EEPROM devices. Because of the extra power drawn on R_{PD}, note that a high value should be chosen for the R_{PD}.

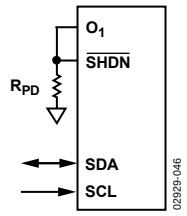

Figure 47. Shutdown by Internal Logic Output

MULTIPLE DEVICES ON ONE BUS

Figure 48 shows four AD5282 devices on the same serial bus. Each has a different slave address because the states of their Pin AD0 and Pin AD1 are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I^2C-compatible interface.

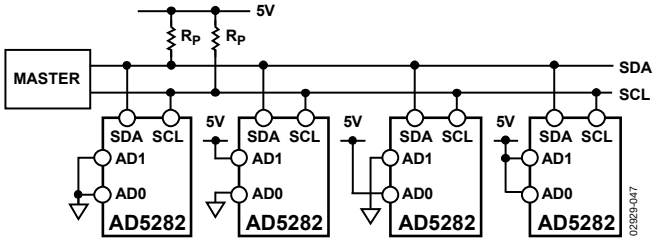

Figure 48. Multiple AD5282 Devices on One Bus

LEVEL SHIFT FOR BIDIRECTIONAL INTERFACE

While most old systems can be operated at one voltage, a new component can be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, a 3.3 V EEPROM can interface with a 5 V digital potentiometer. A level-shift scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the EEPROM. Figure 49 shows one of the implementations. M1 and M2 can be any N-channel signal FETs or low threshold FDV301N if V_{DD} falls below 2.5 V.

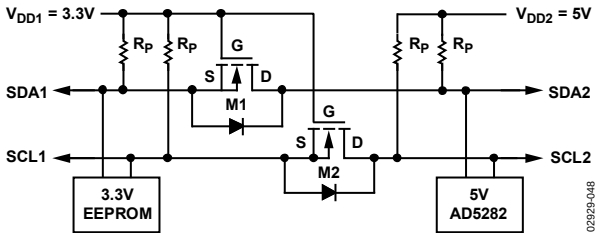

Figure 49. Level Shift for Different Potential Operation

LEVEL SHIFT FOR NEGATIVE VOLTAGE OPERATION

The digital potentiometer is popular in laser diode driver applications and certain telecommunications equipment level-setting applications. These applications are sometimes operated between ground and a negative supply voltage such that the systems can be biased at ground to avoid large bypass capacitors that may significantly impede the ac performance. Like most digital potentiometers, the AD5280/AD5282 can be configured with a negative supply (see Figure 50).

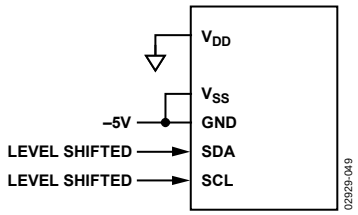

Figure 50. Biased at Negative Voltage

However, the digital inputs must also be level shifted to allow proper operation because the ground is referenced to the negative potential. Figure 51 shows one implementation with a few transistors and a few resistors. When V_{IN} is below the Q3 threshold value, Q3 is off, Q1 is off, and Q2 is on. In this state, V_{OUT} approaches 0 V. When V_{IN} is above 2 V, Q3 is on, Q1 is on, and Q2 is turned off. In this state, V_{OUT} is pulled down to V_{SS}. Be aware that proper time shifting is also needed for successful communication with the device.

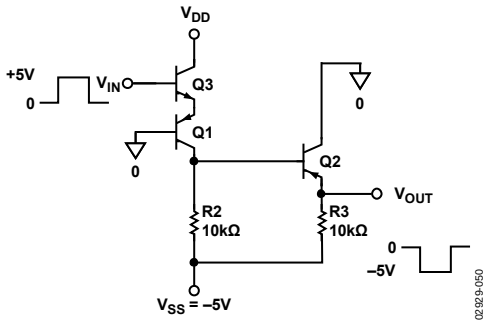

Figure 51. Level Shift for Bipolar Potential Operation

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 52. The protection applies to digital inputs SDA, SCL, and $\overline{SHDN}$.

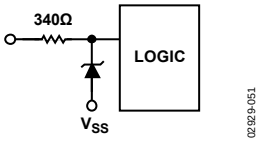

Figure 52. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

The AD5280/AD5282 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Resistor Terminal A, Resistor Terminal B, and Wiper Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 53).

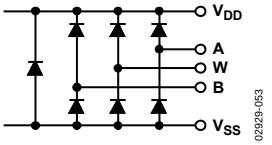

Figure 53. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Because there are ESD protection diodes that limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 53), it is important to power V_{DD}/V_{SS} before applying any voltage to the A, B, and W terminals. Otherwise, the diode is forward biased such that V_{DD}/V_{SS} is unintentionally powered, which may affect the rest of the user's circuit. The ideal power-up sequence is the following: GND, V_{DD}, V_{SS}, digital inputs, and $V_A/V_B/V_W$. The order of powering $V_A/V_B/V_W$ and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to design a layout with compact, minimum lead lengths. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and filter low frequency ripple (see Figure 54). Notice that the digital ground should also be joined remotely to the analog ground at one point to minimize digital ground bounce.

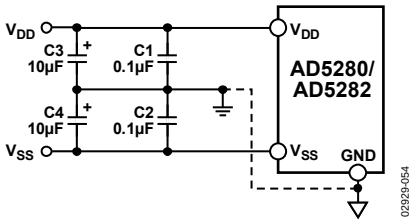

Figure 54. Power Supply Bypassing

APPLICATIONS INFORMATION

BIPOLAR DC OR AC OPERATION FROM DUAL SUPPLIES

The AD5280/AD5282 can be operated from dual supplies enabling control of ground-referenced ac signals or bipolar operation. The ac signal, as high as V_{DD}/V_{SS}, can be applied directly across Terminal A to Terminal B with the output taken from Terminal W. See Figure 55 for a typical circuit connection.

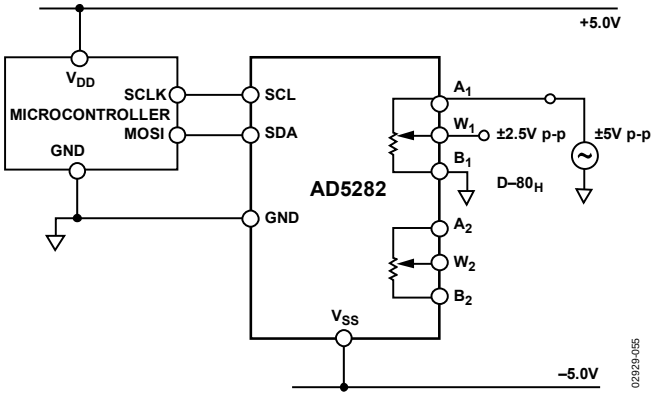

Figure 55. Bipolar Operation from Dual Supplies

GAIN CONTROL COMPENSATION

The digital potentiometer is commonly used in gain control applications such as the noninverting gain amplifier shown in Figure 56.

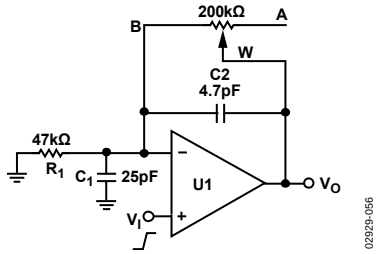

Figure 56. Typical Noninverting Gain Amplifier

Notice that the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node. It introduces a 0 for the $1/\beta_O$ term with 20 dB/decade (dec), whereas a typical op amp GBP has −20 dB/dec characteristics. A large R2 and finite C1 can cause the 0 frequency to fall well below the crossover frequency. Thus the rate of closure becomes 40 dB/dec, and the system has a 0° phase margin at the crossover frequency. The output may ring or oscillate if the input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option unless C2 is scaled as if R2 were at its maximum value. Doing so may overcompensate and compromise the performance slightly when R2 is set at low values. However, it avoids the gain peaking, ringing, or oscillation at the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of a few picofarads (pF) to no more than a few tenths of a picofarad is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown); fortunately, their effect at this node is less significant and the compensation can be avoided in most cases.

15 V, 8-BIT I²C DAC

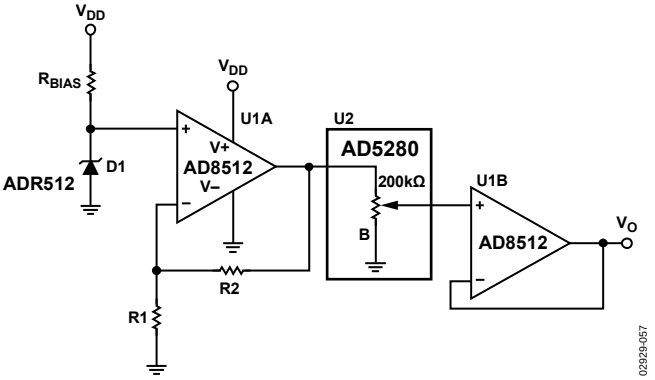

Figure 57. 8-Bit I²C DAC

AD5280/AD5282 can be configured as a high voltage DAC, as high as 15 V. The output is

$$V_O(D) = \frac{D}{256}[1.2\text{V} \times (1+\frac{R_2}{R_1})] \quad (5)$$

8-BIT BIPOLAR DAC

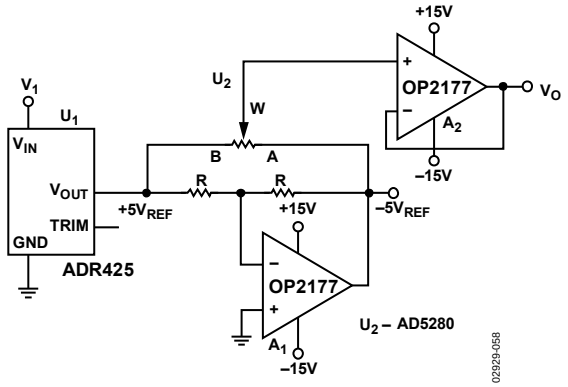

Figure 58. 8-Bit Bipolar DAC

Figure 58 shows a low cost, 8-bit, bipolar DAC. It offers the same number of adjustable steps but not the precision of conventional DACs. The linearity and temperature coefficients, especially at low value codes, are skewed by the effects of the digital potentiometer wiper resistance. The output of this circuit is

$$V_O = \left(\frac{2D}{256} - 1\right) \times V_{REF} \quad (6)$$

BIPOLAR PROGRAMMABLE GAIN AMPLIFIER

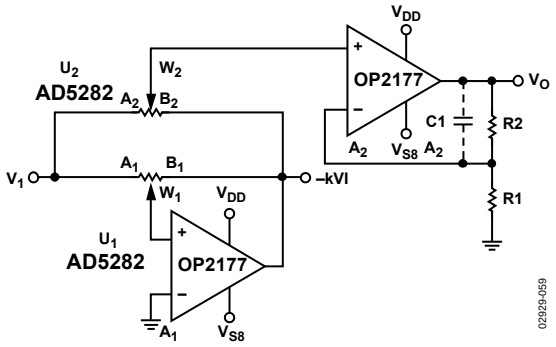

Figure 59. Bipolar Programmable Gain Amplifier

For applications that require bipolar gain, Figure 59 shows one implementation similar to the previous circuit. The digital potentiometer, U_1, sets the adjustment range. The wiper voltage at W_2 can therefore be programmed between V_i and $-KV_i$ at a given U_2 setting. Configuring A_2 in noninverting mode allows linear gain and attenuation. The transfer function is

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D2}{256} \times (1 + K) - K\right) \quad (7)$$

where K is the ratio of R_{WB1}/R_{WA1} set by U_1.

As in the previous example, in the simpler and more common case where K = 1, a single digital AD5280 potentiometer is used. U_1 is replaced by a matched pair of resistors to apply V_i and $-V_i$ at the ends of the digital potentiometer. The relationship becomes

$$V_O = \left(1 + \frac{R2}{R1}\right)\left(\frac{2D2}{256} - 1\right) \times V_i \quad (7)$$

If R2 is large, a compensation capacitor having a few pF may be needed to avoid any gain peaking.

Table 7 shows the result of adjusting D, with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and a 256-step resolution.

Table 7. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9R1
0	−1	−2	−10
64	−0.5	−1	−5
128	0	0	0
192	0.5	1	5
255	0.968	1.937	9.680

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustments, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 60).

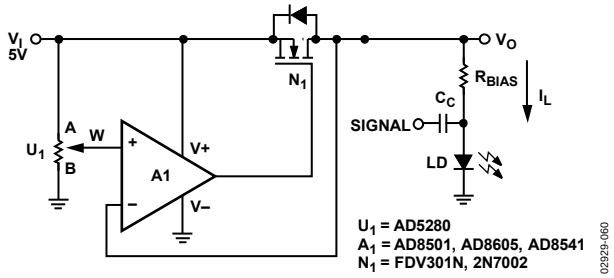

Figure 60. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{BIAS} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET N1. The N1 power handling must be adequate to dissipate $(V_i - V_O) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. A1 needs to be a rail-to-rail input type. For precision applications, a voltage reference such as ADR423, ADR292, or AD1584 can be applied at the input of the digital potentiometer.

PROGRAMMABLE CURRENT SOURCE

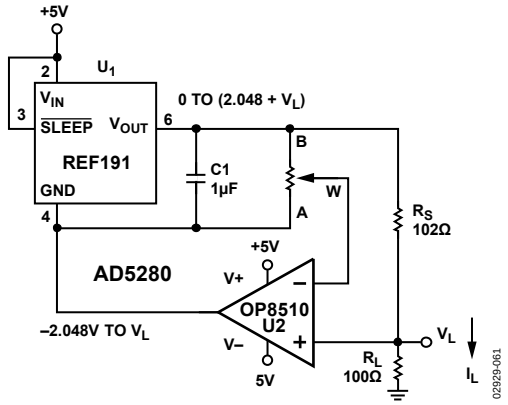

Figure 61. Programmable Current Source

A programmable current source can be implemented with the circuit shown in Figure 61. REF191 is a unique, low supply headroom and high current handling precision reference that can deliver 20 mA at 2.048 V. The load current is simply the voltage across Terminal B to Terminal W of the digital potentiometer divided by R_S.

$$I_L = \frac{V_{REF} \times D}{R_S \times 2^N} \tag{8}$$

The circuit is simple, but attention must be paid to two things. First, dual-supply op amps are ideal because the ground potential of REF191 can swing from −2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system is reduced.

For applications that demand higher current capabilities, a few changes to the circuit in Figure 61 produce an adjustable current in the range of hundreds of milliamps. First, the voltage reference needs to be replaced with a high current, low dropout regulator, such as the ADP3333, and the op amp needs to be swapped with a high current dual-supply model, such as the AD8532. Depending on the desired range of current, an appropriate value for R_S must be calculated. Because of the high current flowing to the load, the user must pay attention to the load impedance so as not to drive the op amp beyond the positive rail.

PROGRAMMABLE BIDIRECTIONAL CURRENT SOURCE

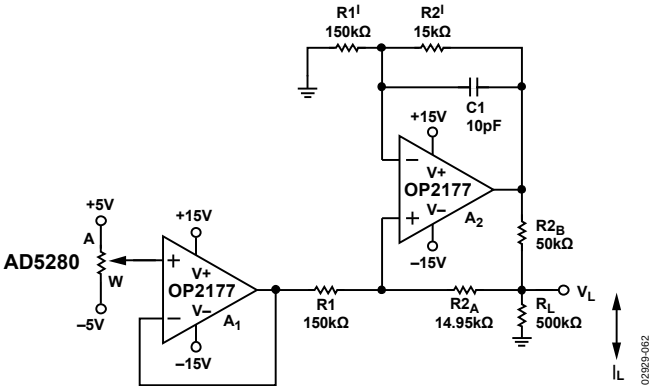

Figure 62. Programmable Bidirectional Current Source

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution (see Figure 62). If the resistors are matched, the load current is

$$I_L = \frac{\left(R2_A + R2_B\right)}{\frac{R1}{R2_B}} \times V_W \tag{9}$$

In theory, $R2_B$ can be made as small as needed to achieve the current needed within the A_2 output current driving capability. In this circuit, the OP2177 can deliver ±5 mA in either direction, and the voltage compliance approaches 15 V. It can be shown that the output impedance is

$$Z_O = \frac{R1' \times R2_B\left(R1 + R2_A\right)}{R1 \times R2' - R1'\left(R2_A + R2_B\right)} \tag{10}$$

This output impedance can be infinite if Resistor R1' and Resistor R2' match precisely with R1 and $R2_A + R2_B$, respectively. On the other hand, it can be negative if the resistors are not matched. As a result, C1 must be in the range of 1 pF to 10 pF to prevent the oscillation.

PROGRAMMABLE LOW-PASS FILTER

In analog-to-digital conversion applications, it is common to include an antialiasing filter to band-limit the sampling signal. Dual-channel digital potentiometers can be used to construct a second-order Sallen key low-pass filter (see Figure 63). The design equations are

$$\frac{V_O}{V_i} = \frac{\omega_O{}^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O{}^2} \quad (11)$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \quad (12)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (13)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2 and let R1 = R2. As a result, R1 and R2 can be adjusted to the same settings to achieve the desirable bandwidth.

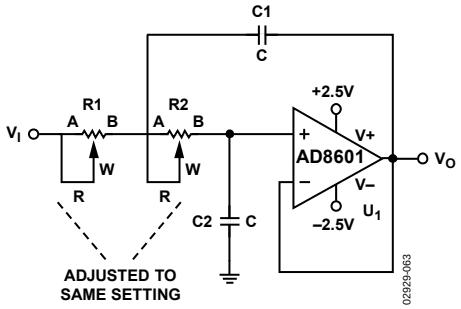

Figure 63. Sallen Key Low-Pass Filter

PROGRAMMABLE OSCILLATOR

In a classic Wien-bridge oscillator (Figure 64), the Wien network (R, R', C, C') provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, f_O, the overall phase shift is 0, and the positive feedback causes the circuit to oscillate. With R = R', C = C', and R2 = $R2_A$//($R2_B$ + R_{diode}), the oscillation frequency is

$$\omega_O = \frac{1}{RC} \text{ or } f_o = \frac{1}{2\pi RC} \quad (14)$$

where R is equal to R_{WA} such that

$$R = \frac{256 - D}{256} R_{AB} \quad (15)$$

At resonance, setting the following balances the bridge:

$$\frac{R2}{R1} = 2 \quad (16)$$

In practice, R2/R1 should be set slightly larger than 2 to ensure that oscillation can start. On the other hand, the alternate turn-on of Diode D1 and Diode D2 ensures that R2/R1 are smaller than 2 momentarily and, therefore, stabilizes the oscillation.

Once the frequency is set, the oscillation amplitude can be tuned by $R2_B$ because

$$\frac{2}{3}V_O = I_D R2_B + V_D \quad (17)$$

V_O, I_D, and V_D are interdependent variables. With proper selection of $R2_B$, an equilibrium is reached such that V_O converges. $R2_B$ can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to prevent saturation of the output.

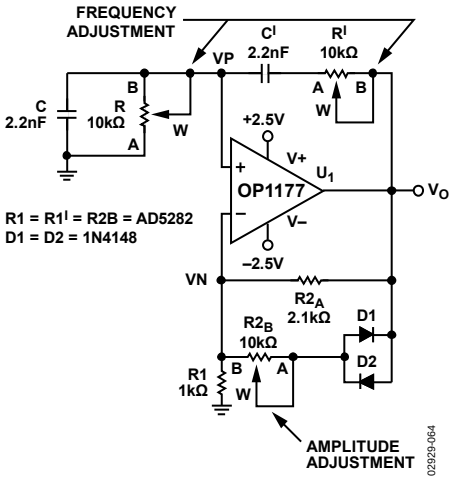

Figure 64. Programmable Oscillator with Amplitude Control

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the −3 dB bandwidth of the AD5280 (20 kΩ resistor) measures 310 kHz at half scale. Figure 24 provides the Bode plot characteristics of the three available resistor versions: 20 kΩ, 50 kΩ, and 200 kΩ. A parasitic simulation model is shown in Figure 65. A macro model net list for the 20 kΩ RDAC is provided.

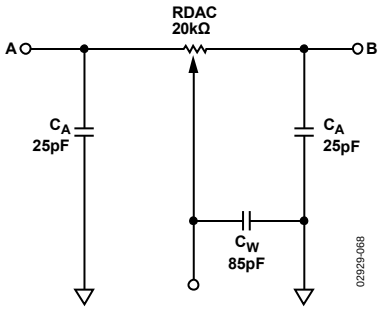

Figure 65. RDAC Circuit Simulation Model for RDAC = 20 kΩ

MACRO MODEL NET LIST FOR RDAC

```
.PARAM D=256, RDAC=20E3
*
.SUBCKT DPOT (A,W,B)
*
CA              A    0    25E-12
RWA             A    W    {(1-D/256)*RDAC+60}
CW              W    0    55E-12
RWB             W    B    {D/256*RDAC+60}
CB              B    0    25E-12
*
.ENDS DPOT
```

OUTLINE DIMENSIONS

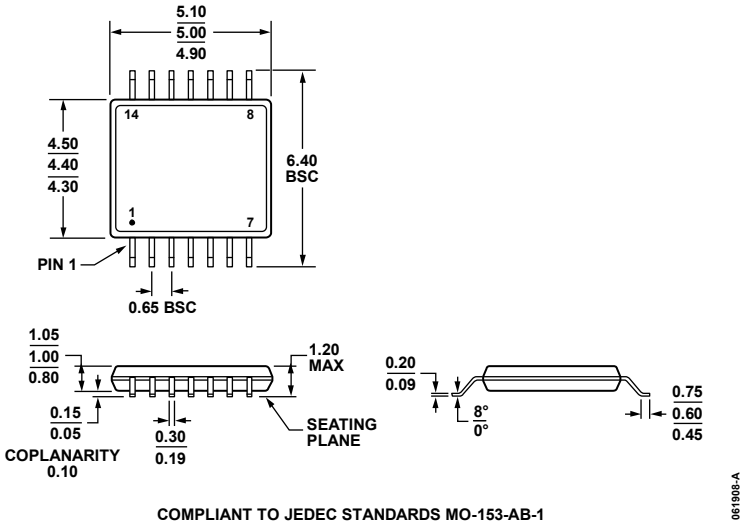

Figure 66. 14-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-14)
Dimensions shown in millimeters

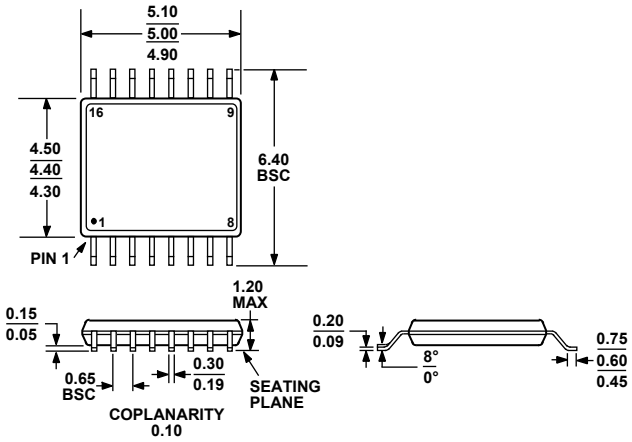

Figure 67. 16-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	No. of Channels	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity
AD5280BRU20	1	20	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5280BRU20-REEL7	1	20	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000
AD5280BRU50	1	50	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5280BRU50-REEL7	1	50	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000
AD5280BRU200-REEL7	1	200	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000
AD5280BRUZ20[2]	1	20	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5280BRUZ20-REEL7[2]	1	20	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000
AD5280BRUZ50[2]	1	50	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5280BRUZ50-REEL7[2]	1	50	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000
AD5280BRUZ200[2]	1	200	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5280BRUZ200-R7[2]	1	200	−40°C to +85°C	14-Lead TSSOP	RU-14	1,000
AD5282BRU20	2	20	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5282BRU20-REEL7	2	20	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5282BRU50	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5282BRU50-REEL7	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5282BRU200	2	200	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5282BRU200-REEL7	2	200	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5282BRUZ20[2]	2	20	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5282BRUZ20-REEL7[2]	2	20	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5282BRUZ50[2]	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5282BRUZ50-REEL7[2]	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5282BRUZ200[2]	2	200	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5282BRUZ200-R7[2]	2	200	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5282-EVAL	2	20		Evaluation Board		

[1] Line 1 contains model number, Line 2 contains ADI logo followed by the end-to-end resistance value, and Line 3 contains date code YYWW.
[2] Z = RoHS Compliant Part.

NOTES

NOTES

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