Selection Guide

Part Number	Packing	Package
~~A3946KLBTR-T*~~	1000 pieces/reel	16-pin SOIC with internally fused leads
A3946KLPTR-T	4000 pieces/reel	16-pin TSSOP with exposed thermal pad

*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 3, 2010. Deadline for receipt of LAST TIME BUY orders is October 29, 2010.

Absolute Maximum Ratings

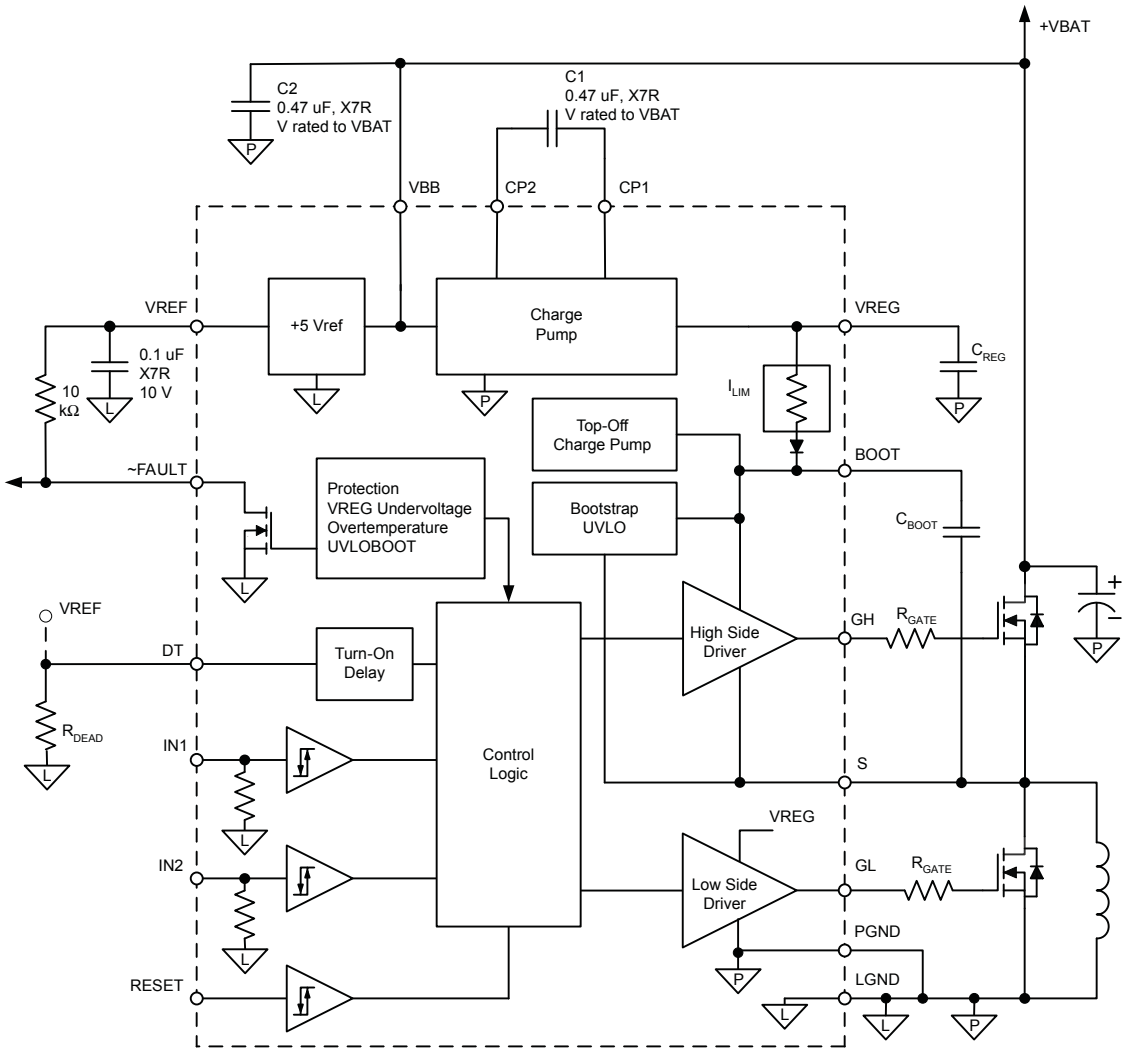
Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		60	V
Logic Inputs Voltage	V_{IN}		–0.3 to 6.5	V
Pin S Voltage	V_S		–4 to 60	V
Pin GH Voltage	V_{GH}		–4 to 75	V
Pin BOOT Voltage	V_{BOOT}		–0.6 to 75	V
Pin DT Voltage	V_{DT}		V_{REF}	V
Pin VREG Voltage	V_{REG}		–0.6 to 15	V
Operating Ambient Temperature	T_A	Range K	–40 to 135	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC
ESD Rating, Human Body Model		AEC-Q100-002, all pins	2000	V
ESD Rating, Charged Device Model		AEC-Q100-011, all pins	1050	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LB, 2-layer PCB with 3.57 in². 2-oz copper both sides	48	ºC/W
		Package LB, 4-layer PCB based on JEDEC standard	38	ºC/W
		Package LP, 2-layer PCB with 3.8 in². 2-oz copper both sides	43	ºC/W
		Package LP, 4-layer PCB based on JEDEC standard	34	ºC/W

*Additional thermal information available on Allegro Web site.

Functional Block Diagram



Control Logic Table

IN1	IN2	DT Pin	RESET	GH	GL	Function
X	X	X	0	Z	Z	Sleep mode
0	0	R_{DEAD} - LGND	1	L	H	Low-side FET ON following dead time
0	1	R_{DEAD} - LGND	1	L	L	All OFF
1	0	R_{DEAD} - LGND	1	L	L	All OFF
1	1	R_{DEAD} - LGND	1	H	L	High-side FET ON following dead time
0	0	VREF	1	L	L	All OFF
0	1	VREF	1	L	H	Low-side FET ON
1	0	VREF	1	H	L	High-side FET ON
1	1	VREF	1	H	H	CAUTION: High-side and low-side FETs ON

ELECTRICAL CHARACTERISTICS at T_A = –40 to +135°C, V_{BB} = 7 to 60 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
V_{BB} Quiescent Current	I_{VBB}	RESET = High, Outputs Low	—	3	6	mA
		RESET = Low	—	—	10	µA
VREG Output Voltage	V_{REG}	V_{BB} > 7.75 V, I_{reg} = 0 mA to 15 mA	12.0	13	13.5	V
		V_{BB} = 7 V to 7.75 V, I_{reg} = 0 mA to 15 mA	11.0	—	13.5	V
Charge Pump Frequency	F_{CP}	CP1, CP2	—	62.5	—	kHz
VREF Output Voltage	V_{REF}	I_{REF} ≤ 4 mA, C_{REF} = 0.1 µF	4.5	—	5.5	V
Top-Off Charge Pump Current	I_{TO}	$V_{BOOT} – V_S$ = 8.5 V	20	—	—	µA
Gate Output Drive						
Turn On Time	t_{rise}	C_{LOAD} = 3300 pF, 20% to 80%	—	60	100	ns
Turn Off Time	t_{fall}	C_{LOAD} = 3300 pF, 80% to 20%	—	40	80	ns
Pullup On Resistance	R_{DSUP}	T_j = 25°C	—	4	—	Ω
		T_j = 135°C	—	6	8	Ω
Pulldown On Resistance	R_{DSDOWN}	T_j = 25°C	—	2	—	Ω
		T_j = 135°C	—	3	4	Ω
GH Output Voltage	V_{GH}	t_{pw} < 10 µs, Bootstrap Capacitor fully charged	V_{REG} – 1.5	—	—	V
GL Output Voltage	V_{GL}	—	V_{REG} – 0.2	—	—	V
Timing						
Dead Time (Delay from Turn Off to Turn On)	t_{DEAD}	R_{dead} = 5 kΩ	200	350	500	ns
		R_{dead} = 100 kΩ	5	6	7	µs
Propagation Delay	t_{PD}	Logic input to unloaded GH, GL. DT = VREF	—	—	150	ns

ELECTRICAL CHARACTERISTICS at T_A = –40 to +135°C, V_{BB} = 7 to 60 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Protection						
VREG Undervoltage	V_{REGOFF}	V_{REG} decreasing	7.8	8.3	8.8	V
	V_{REGON}	V_{REG} increasing	8.6	9.1	9.6	V
BOOT Undervoltage	V_{BSOFF}	V_{BOOT} decreasing	7.25	7.8	8.3	V
	V_{BSON}	V_{BOOT} increasing	8	8.75	9.5	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	—	170	—	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	—	15	—	°C
Logic						
Input Current	$I_{IN(1)}$	IN1 V_{IN} / IN2 V_{IN} = 2.0 V	—	40	100	µA
	$I_{IN(0)}$	IN1 V_{IN} / IN2 V_{IN} = 0.8 V	—	16	40	µA
		RESET pin only	—	—	1	µA
Logic Input Voltage	$V_{IN(1)}$	IN1 / IN2 logic high	2.0	—	—	V
		RESET logic high	2.2	—	—	V
	$V_{IN(0)}$	Logic low	—	—	0.8	V
Logic Input Hysteresis	—	All digital inputs	100	—	300	mV
Fault Output	V_{ol}	I = 1 mA, fault asserted	—	—	400	mV
	V_{oh}	V = 5 V	—	—	1	µA

Functional Description

VREG. A 13 V output from the on-chip charge pump, used to power the low-side gate drive circuit directly, provides the current to charge the bootstrap capacitors for the high-side gate drive.

The VREG capacitor, C_{REG}, must supply the instantaneous current to the gate of the low-side MOSFET. A 10 µF, 25 V capacitor should be adequate. This capacitor can be either electrolytic or ceramic (X7R).

Diagnostics and Protection. The fault output pin, ~FAULT, goes low (i.e., FAULT = 1) when the RESET line is high and any of the following conditions are present:

- Undervoltage on VREG (UVREG). Note that the outputs become active as soon as VREG comes out of undervoltage, even though the ~FAULT pin is latched until reset.
- Undervoltage on VREF (UVREF). Note that this condition does NOT latch a fault.
- A junction temperature > 170°C (OVERTEMP). This condition sets a latched fault.
- An undervoltage on the stored charge of the BOOT capacitor (UVBOOT). This condition does NOT set a latched fault.

An overtemperature event signals a latched fault, but does not disable any output drivers, regulators, or logic inputs. The user must turn off the A3946 (e.g., force the RESET line low) to prevent damage.

The power FETs are protected from inadequate gate drive voltage by undervoltage detectors. Either of the regulator undervoltage faults (UVREG or UVREF) disable both output drivers until both voltages have been restored. The high-side driver is also disabled during a UVBOOT fault condition.

Under many operating conditions, both the high-side (GH) and low-side (GL) drivers may be off, allowing the BOOT capacitor to discharge (or never become charged) and create a UVBOOT fault condition, which in turn inhibits the high-side driver and creates a FAULT = 1. This fault is NOT latched. To remove this fault, momentarily turn on GL to charge the BOOT capacitor.

Latched faults may be cleared by a low pulse, 1 to 10 µs wide, on the RESET line. Throughout that pulse (despite a possible UVBOOT), FAULT = 0; also the fault latch is cleared immediately, and remains cleared. If the power is restored (no UVREG or UVREF), and if no OVERTEMP fault exists, then the latched fault remains cleared when the RESET line returns to high. However, FAULT = 1 may still occur because a UVBOOT fault condition may still exist.

Charge Pump. The A3946 is designed to accommodate a wide range of power supply voltages. The charge pump output, VREG, is regulated to 13 V nominal.

In all modes, this regulator is current-limited. When V_{BB} < 8 V, the charge pump operates as a voltage doubler. When 8 V < V_{BB}< 15 V, the charge pump operates as a voltage doubler/PWM, current-controlled, voltage regulator. When V_{BB}>15 V, the charge pump operates as a PWM, current-controlled, voltage regulator. Efficiency shifts, from 80% at V_{BB}= 7 V, to 20% at V_{BB} = 50 V.

CAUTION. Although simple paralleling of VREG supplies from several A3946s may appear to work correctly, such a configuration is NOT recommended. There is no assurance that one of the regulators will not dominate, taking on all of the load and back-biasing the other regulators. (For example, this could occur if a particular regulator has an internal reference voltage that is higher that those of the other regulators, which would force it to regulate at the highest voltage.)

Sleep Mode/Power Up. In Sleep Mode, all circuits are disabled in order to draw minimum current from VBB. When powering up and leaving Sleep Mode (the RESET line is high), the gate drive outputs stay disabled and a fault remains asserted until VREF and VREG pass their undervoltage thresholds. When powering up, before starting the first bootstrap charge cycle, wait until $t = C_{REG}/4$ (where C_{REG} is in µF, and t is in ns) to allow the charge pump to stabilize.

When powered-up (not in Sleep Mode), if the RESET line is low for > 10 µs, the A3946 may start to enter Sleep Mode (V_{REF} < 4 V). In that case, ~FAULT = 1 as long as the RESET line remains low.

If the RESET line is open, the A3946 should go into Sleep Mode. However, to ensure that this occurs, the RESET line must be grounded.

Dead Time. The analog input pin DT sets the delay to turn on the high- or low-side gate outputs. When instructed to turn off, the gate outputs change after an short internal propagation delay (90 ns typical). The dead time controls the time between this turn-off and the turn-on of the appropriate gate. The duration, t_{DEAD}, can be adjusted within the range 350 ns to 6000 ns using the following formula:

$$t_{DEAD} = 50 + (R_{DEAD} / 16.7)$$

where t_{DEAD} is in ns, and R_{DEAD} is in Ω, and should be in the range 5 kΩ < R_{DEAD} < 100 kΩ.

Do not ground the DT pin. If the DT pin is left open, dead time defaults to 12 µs.

Control Logic. Two different methods of control are possible with the A3946. When a resistor is connected from DT to ground, a single-pin PWM scheme is utilized by shorting IN1 with IN2. If a very slow turn-on is required (greater than 6 µs), the two input pins can be hooked-up individually to allow the dead times to be as long as needed.

The dead time circuit can be disabled by tying the DT pin to VREF. This disables the turn-on delay and allows direct control of each MOSFET gate via two control lines. This is shown in the Control Logic table, on page 2.

Top-Off Charge Pump. An internal charge pump allows 100% duty cycle operation of the high-side MOSFET. This is a low-current trickle charge pump, and is only operated after a high-side has been signaled to turn on. A small amount of bias current is drawn from the BOOT pin to operate the floating high-side circuit. The top-off charge pump simply provides enough drive to ensure that the gate voltage does not droop due to this bias supply current. The charge required for initial turn-on of the high-side gate must be supplied by bootstrap capacitor charge cycles. This is described in the section Application Information.

VREF. VREF is used for the internal logic circuitry and is not intended as an external power supply. However, the VREF pin can source up to 4 mA of current. A 0.1 µF capacitor is needed for decoupling.

Fault Response Table

Fault Mode	RESET	~FAULT	VREG	VREF	GH[1]	GL[1]
No Fault	1	1	ON	ON	(IL)	(IL)
BOOT Capacitor Undervoltage[2]	1	0	ON	ON	0	(IL)
VREG Undervoltage[3]	1	0	ON	ON	0	0
VREF Undervoltage[4]	1	0	OFF	ON	0	0
Thermal Shutdown[3]	1	0	ON	ON	(IL)	(IL)
Sleep[5]	0	1	OFF	OFF	High Z	High Z

[1](IL) indicates that the state is determined by the input logic.
[2]This fault occurs whenever there is an undervoltage on the BOOT capacitor. This fault is not latched.
[3]These faults are latched. Clear by pulsing RESET = 0. Note that outputs become active as soon as VREG comes out of undervoltage, even though ~FAULT = 0.
[4]Unspecified VREF undervoltage threshold < 4 V.
[5]During power supply undervoltage conditions, GH and GL are instructed to be 0 (low). However, with VREG < 4 V, the outputs start to become high impedance (High Z). Refer to the section *Sleep Mode/Power Up*.

Application Information

Bootstrap Capacitor Selection. C_{BOOT} must be correctly selected to ensure proper operation of the device. If too large, time is wasted charging the capacitor, with the result being a limit on the maximum duty cycle and PWM frequency. If the capacitor is too small, the voltage drop can be too large at the time the charge is transferred from the C_{BOOT} to the MOSFET gate.

To keep the voltage drop small:

$$Q_{BOOT} >> Q_{GATE}$$

where a factor in the range of 10 to 20 is reasonable. Using 20 as the factor:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

and

$$C_{BOOT} = Q_{GATE} \times 20 / V_{BOOT}$$

The voltage drop on the BOOT pin, as the MOSFET is being turned on, can be approximated by:

$$Delta\_v = Q_{GATE} / C_{BOOT}$$

For example, given a gate charge, Q_{GATE}, of 160 nC, and the typical BOOT pin voltage of 12 V, the value of the Boot capacitor, C_{BOOT}, can be determined by:

$$C_{BOOT} = (160\ nC \times 20) / 12\ V \approx 0.266\ \mu F$$

Therefore, a 0.22 µF ceramic (X7R) capacitor can be chosen for the Boot capacitor.

In that case, the voltage drop on the BOOT pin, when the high-side MOSFET is turned on, is:

$$Delta\_v = 160\ nC / 0.22\ \mu F = 0.73\ V$$

Bootstrap Charging. It is good practice to ensure that the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested.

The time required to charge the capacitor can be approximated by:

$$t_{CHARGE} = C_{BOOT} (Delta\_v / 100\ mA)$$

At power-up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, Delta_v can be considered to be the full high-side drive voltage, 12 V. Otherwise, Delta_v is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S pin is pulled low, via a GL PWM cycle, and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

Power Dissipation. For high ambient temperature applications, there may be little margin for on-chip power consumption. Careful attention should be paid to ensure that the operating conditions allow the A3946 to remain in a safe range of junction temperature.

The power consumed by the A3946 can be estimated as:

$$P\_total = Pd\_bias + Pd\_cpump + Pd\_switching\_loss$$

where:

$Pd\_bias = V_{BB} \times I_{VBB}$, typically 3 mA,

and

$Pd\_cpump = (2V_{BB} - V_{REG})\ I_{AVE}$, for $V_{BB} < 15$ V, or

$Pd\_cpump = (V_{BB} - V_{REG})\ I_{AVE}$, for $V_{BB} > 15$ V,

in either case, where

$$I_{AVE} = Q_{GATE} \times 2 \times f_{PWM}$$

and

$Pd\_switching\_loss = Q_{GATE} \times V_{REG} \times 2 \times f_{PWM}$ Ratio,

where

$$Ratio = 10\ \Omega / (R_{GATE} + 10\ \Omega).$$

Application Block Diagrams

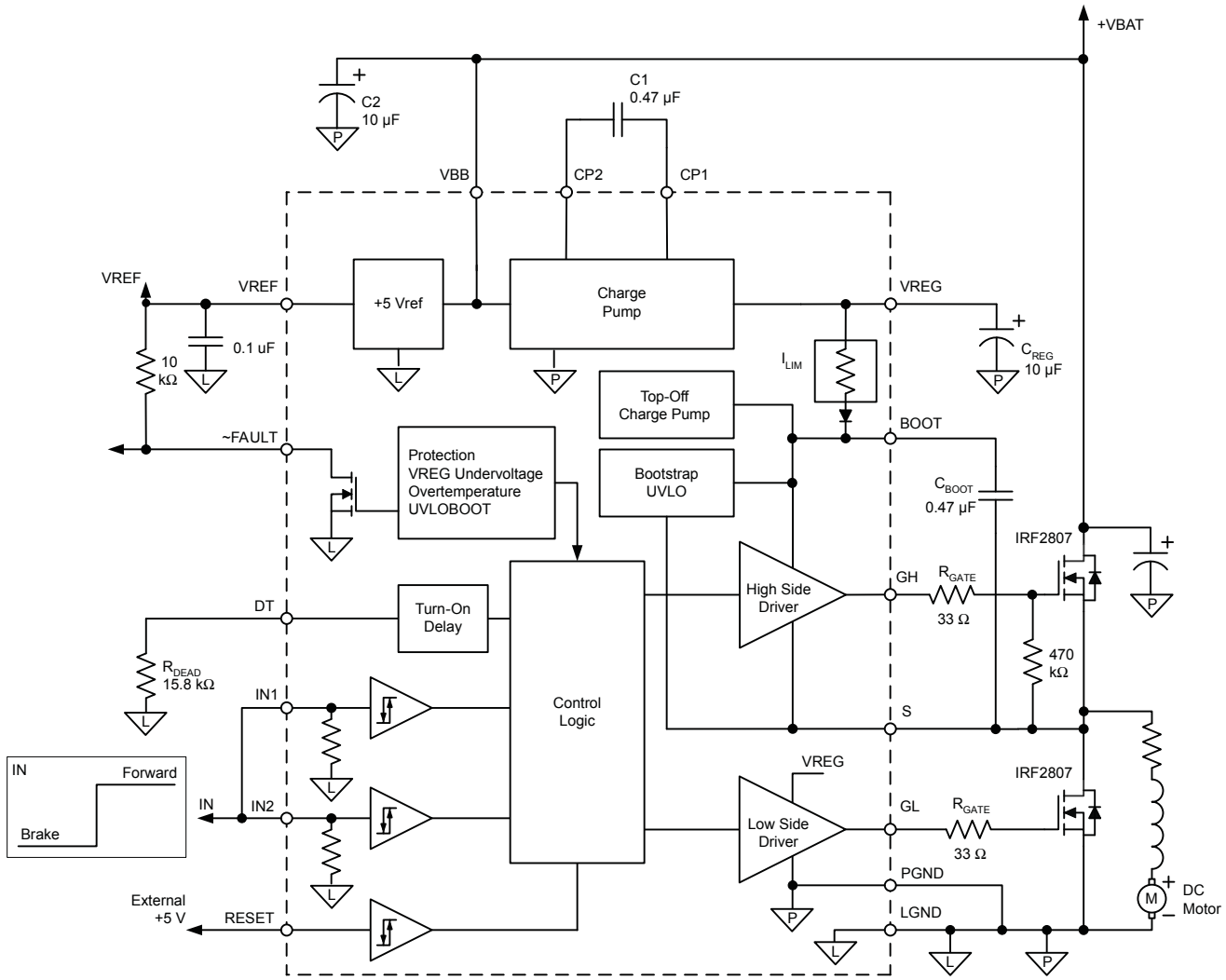


Diagram A. Dependent drivers. Unidirectional motor control with braking and dead time. T_{DEAD} = 1 µs; Q_{TOTAL} = 160 nC.

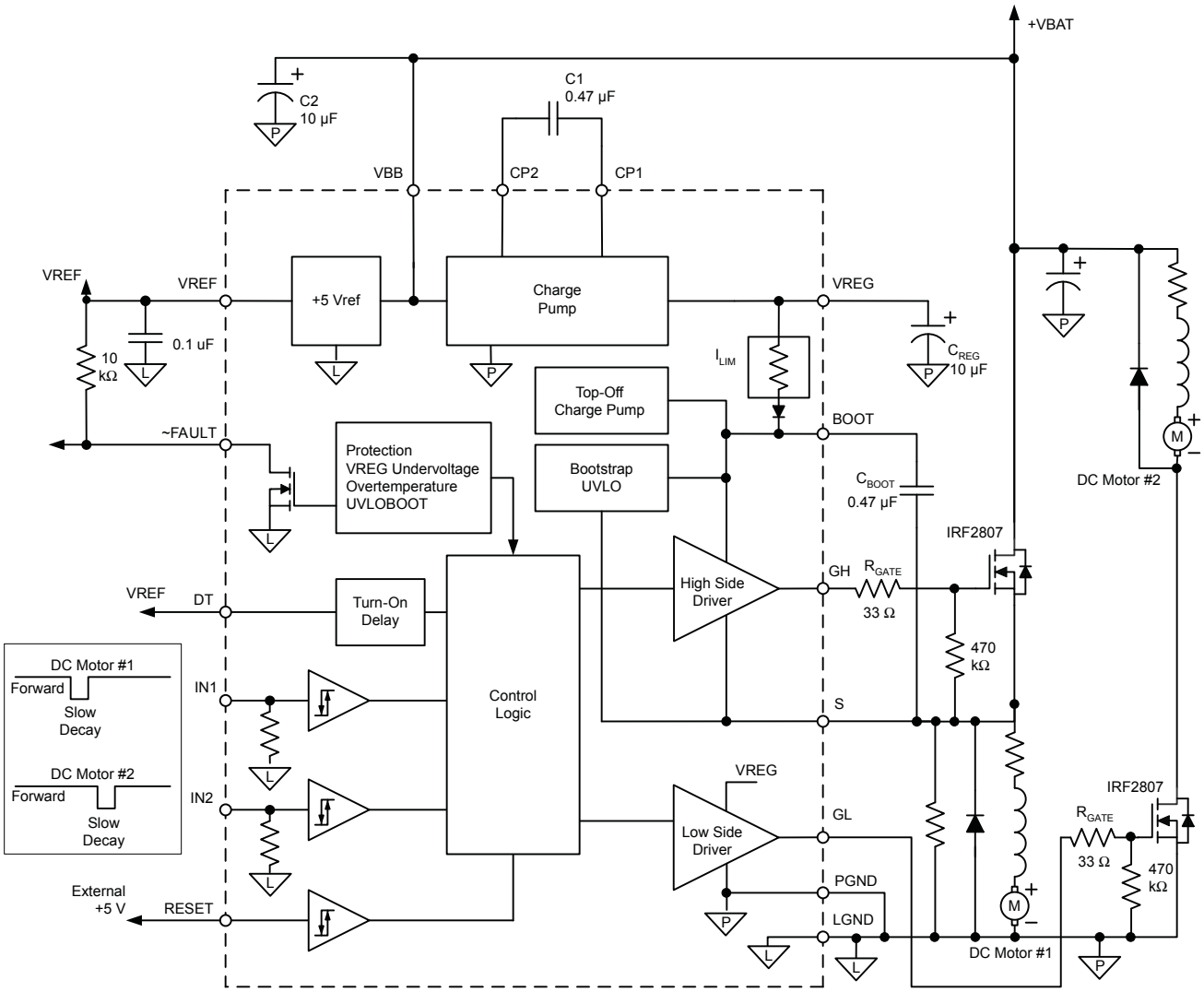


Diagram B. Independent drivers. One high-side drive and one low-side drive.

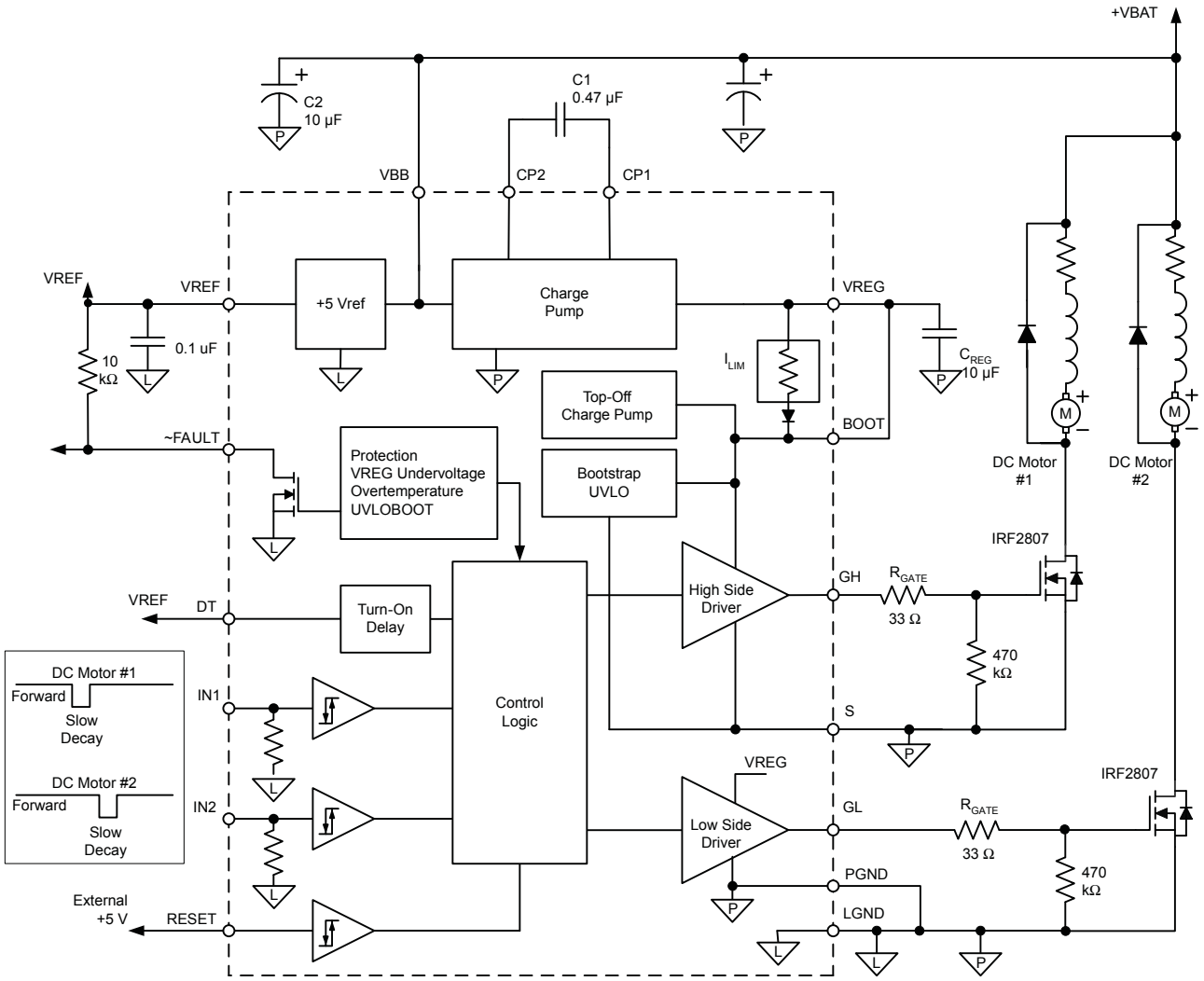
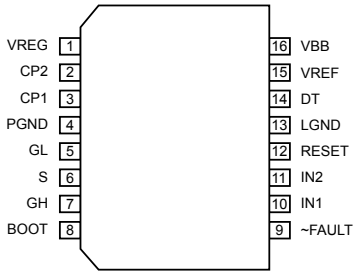


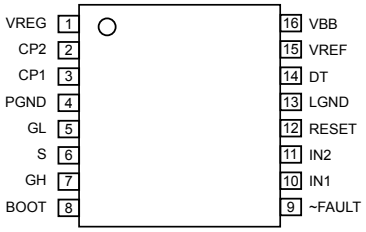
Diagram C. Independent drivers. Two low-side drives.

Pin-out Diagrams

LB package



LP package



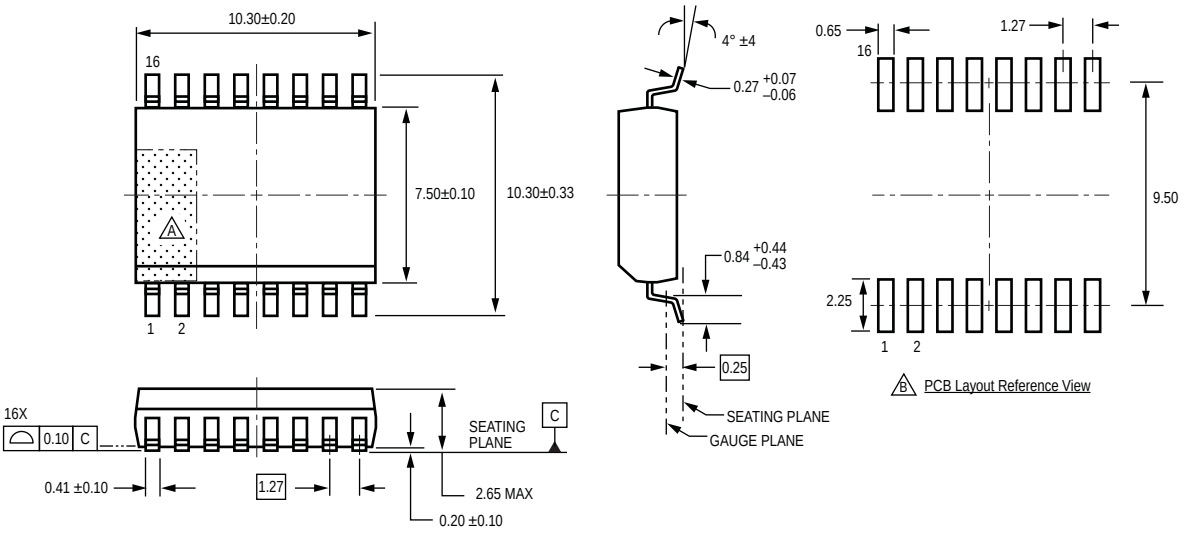
Terminal List Table

Name	Number	Description
VREG	1	Gate drive supply.
CP2	2	Charge pump capacitor, positive side. When not using the charge pump, leave this pin open.
CP1	3	Charge pump capacitor, negative side. When not using the charge pump, leave this pin open.
PGND*	4	External ground. Internally connected to the power ground.
GL	5	Low-side gate drive output for external MOSFET driver. External series gate resistor can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of the S pin output.
S	6	Directly connected to the load terminal. The pin is also connected to the negative side of the bootstrap capacitor and negative supply connection for the floating high-side drive.
GH	7	High-side gate drive output for N-channel MOSFET driver. External series gate resistor can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of the S pin output.
BOOT	8	High-side connection for bootstrap capacitor, positive supply for the high-side gate drive.
~FAULT	9	Diagnostic output, open drain. Low during a fault condition.
IN1	10	Logic control.
IN2	11	Logic control.
RESET	12	Logic control input. When RESET = 0, the chip is in a very low power sleep mode.
LGND*	13	External ground. Internally connected to the logic ground.
DT	14	Dead Time. Connecting a resistor to GND sets the turn-on delay to prevent shoot-through. Forcing this input high disables the dead time circuit and changes the logic truth table.
VREF	15	5 V internal reference decoupling terminal.
VBB	16	Supply Input.

*In the LB package, the PGND pin (4) and LGND pin (13) grounds are internally connected by the leadframe. In the LP package, however, the PGND pin (4) and LGND pin (13) grounds are NOT internally connected, and both must be connected to ground externally.

In the LP package, the exposed thermal pad is not connected to any pin, but should be externally connected to ground, to reduce noise pickup by the pad.

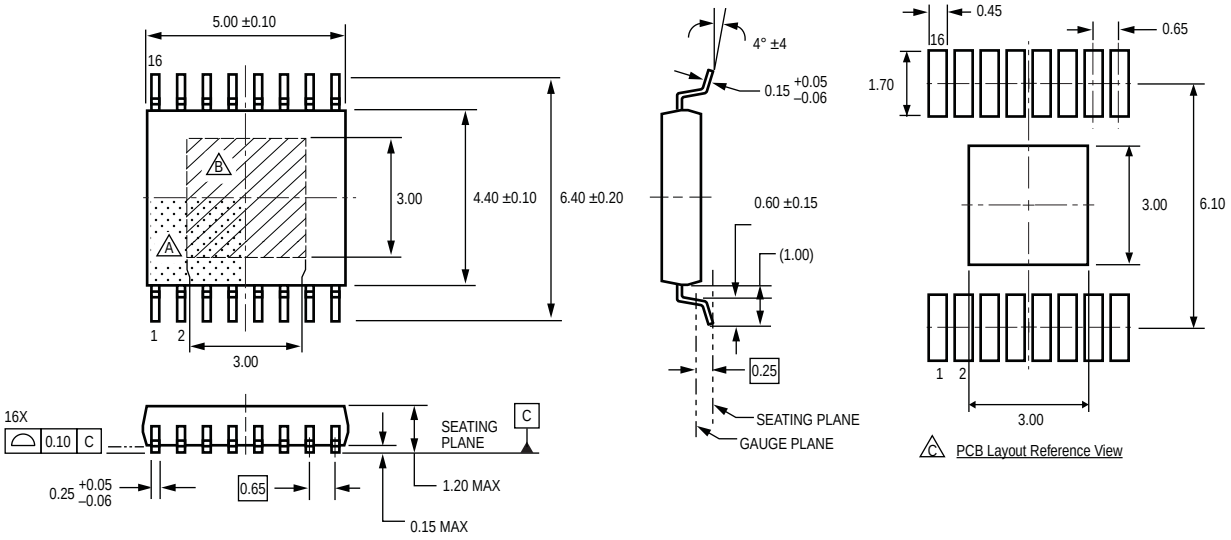
LB Package SOICW



For Reference Only
Dimensions in millimeters
(reference JEDEC MS-013 AA)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Reference pad layout (reference IPC SOIC127P1030X265-16M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

LP Package TSSOP with Exposed Thermal Pad



For Reference Only
(reference JEDEC MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Exposed thermal pad (bottom surface)
C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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