1.0 Functional Description

The ZL38012 is a hardware platform designed to support advanced acoustic echo canceller (with noise reduction) firmware applications available from Zarlink Semiconductor. These applications are resident in external memory and are down-loaded by the ZL38012 resident boot code during initialization.

The firmware products and manuals available at the release of this data sheet are: ZLS385xx: Acoustic Echo Canceller with Noise Reduction for Hands-Free Car Kits. If these applications do not meet your requirements, please contact your local Zarlink Sales Office for the latest firmware releases.

The ZL38012 Advanced Acoustic Echo Canceller with Noise Reduction platform integrates Zarlink's Voice Processor (ZVP) DSP Core with a number of internal peripherals. These peripherals include the following:

- Two independent ΔΣ CODECs
- PCM ports - ST BUS, GCI, McBSP or SSI operation/^{2}S interface port
- A 2048 tap Filter Co-processor (LMS, FIR and FAP realizations)
- Two Auxiliary Timers and a Watchdog Timer
- 5 GPIO pins
- A UART interface
- A Slave SPI port and a Master SPI port
- A timing block that supports master and slave operation
- An IEEE - 1149.1 compatible JTAG port

The DSP Core can process up to two 8-bit audio channels or two 16-bit audio channels. These audio channels may originate and terminate with the ΣΔ CODECs, or be communicated to and from the DSP Core through the PCM/ the I^2S port.

2.0 Core DSP Functional Block

The ZL38012 DSP Core functional block, illustrated in Figure 1, is made up of a DSP Core, Interrupt Controller, Data RAM, Instruction RAM, BOOT ROM and a ButterFly Hardware Accelerator. This block controls the timing (APLL and Timing Generator), peripheral interfaces and Filter Co-processor through a peripheral address/data/control bus.

The ZL38012 implementation of DSP core and Filter Co-processor have been optimized to efficiently support voice processing applications. These applications are described in detail in the Firmware Manuals associated with this hardware platform.

3.0 Codec[1:0]

The ZL38012 has two 16-bit fully differential ΔΣ CODECs (CODEC 0/1) that meet G.712 requirements at 8 kHz sampling, see Figure 2. The ADC path consists of input signal pins C0/1_ADCi+ and C0/1_ADCi- (buffer output pins C0/1_BF0+ and C0/1_BFo-), which feed selectable Microphone Amplifier or Line Amplifier options. Once past the buffer the analog signal goes through a low pass antialiasing filter and to a 4th order feed-forward ΔΣ Modulator that produces a Pulse Density Modulated (PDM) signal. Next the PDM signal goes through a Low Pass Decimation Filter and then is converted into a 16-bit parallel word that can be read by the ZL38012 DSP (ADCout[15:0], Figure 2).

The ZL38012 DSP will send 16-bit parallel word samples (DACin[15:0], Figure 2) to the DAC where they are converted to serial data and passed through an interpolation filter followed by a digital ΔΣ Modulator. The ΔΣ Modulator generates PDM data, which then passes through a 32-tap FIR reconstruction filter. The reconstructed analog signal is then passed to a unity voltage gain differential output driver and to pins C0/1_DACo+ and C0/1_DACo-.

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The CODEC bias voltages are generated by an internal bandgap circuit (BIAS_VCM, BIAS_RF+ and BIAS_RF-).

Each ZL38012 CODEC has two loopbacks. When activated, the input analog signal on pins C0/1_ADC+/- is looped around to C0/1_DAC+/-. Pulse Density Modulated (PDM) serial data from the ADC Analog ΔΣ Modulator output is looped around to the input of the DAC Reconstruction Filter. At the same time 16-bit parallel data is looped around from DACin[15:0] to ADCout[15:0]. PDM serial data from the DAC Digital ΔΣ Modulator is looped around to the input of the ADC Digital Low Pass Decimation Filter.

When the Parallel Loopback is activated the input analog signal on pins C0/1_ADC+/- is looped around to the C0/1_DAC+/- output. 16-bit parallel data from the ADC Digital Low Pass Decimation Filter is looped around to the DAC Digital Low Pass Interpolation Filter. This data may be read by the DSP, but parallel data written to the DAC by the DSP will be lost.

CODEC0 and CODCE1 of the ZL38012 may be powered down if they are not required. See firmware manual.

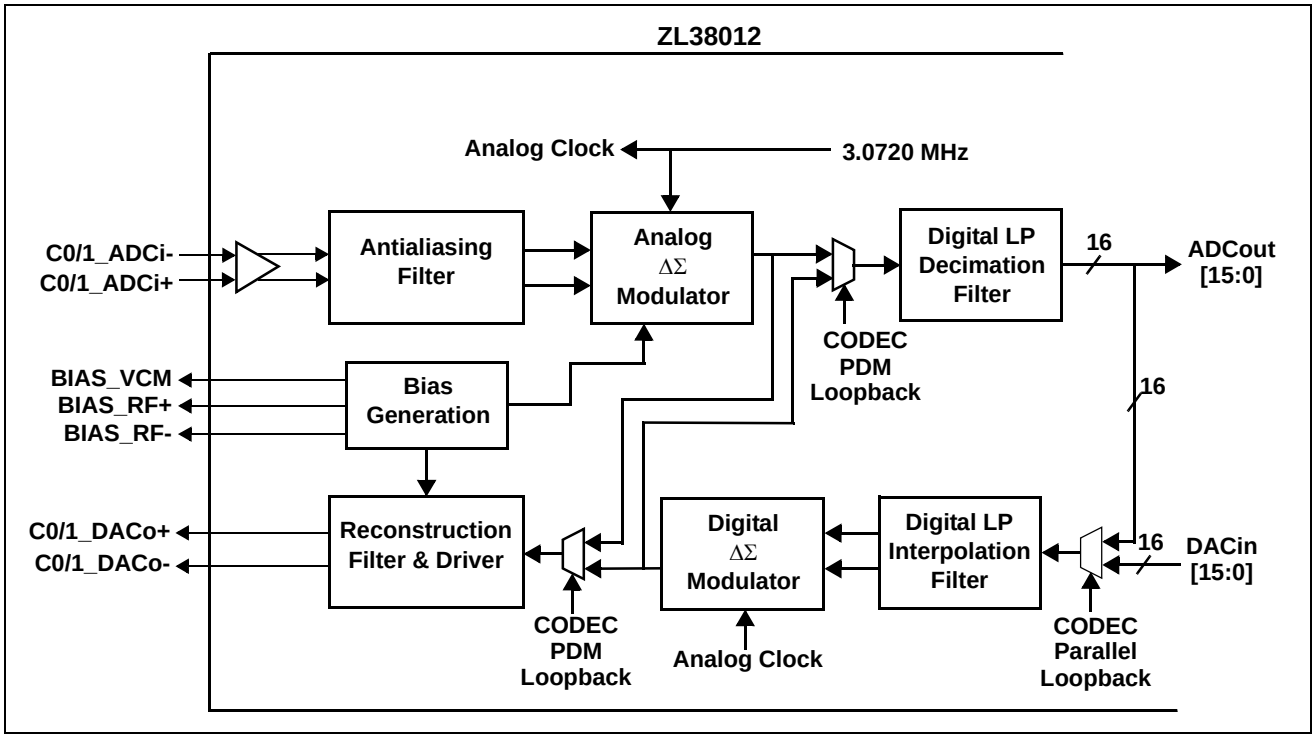

Figure 2 - CODEC Block Diagram

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4.0 PCM / I²S Ports

The PCM port supports data communication between an external peripheral device and the ZL38012 DSP Core using separate input (PCMi) and output (PCMo) serial streams with TDM (i.e., ST-BUS, GCI or McBSP) or SSI interface timing in both master or slave timing modes.

PCM Port pin functions are shared with the I²S Port pin functions. The I²S (Inter-IC Sound) port and PCM Port share the same physical pins of the ZL38012. Selection of either I²S port operation or PCM Port operation is done through the Port PCM/I²S Select Register. See firmware manual.

The I²S port can be used to connect external Analog-to-Digital Converters or CODECs to the internal DSP. This port can operate in master mode, where the ZL38012 is the source of the port clocks, or slave mode, where the bit and sampling clocks (I²S_SCK and I²S_ LRCK) are inputs to the ZL38012. In I²S port master mode the clock signal at output pin I²S_LRCK is the sampling frequency (f_S), the clock signal at output I²S_SCK is 32 x f_S, and the clock signal at output I²S_MCLK is 256 x f_S. In I²S port slave mode the relationship between the clock signal at input pin I²S_LRCK and the clock signal at input I²S_SCK must be 32 x f_S. In slave mode the 256 x f_S relationship between f_S and the I²S_MCLK is not mandatory, and the I²S_MCLK output pin will be in a high impedance state.

Access to the control and status registers associated with these ports is through the Slave SPI port or UART.

5.0 Host Microprocessor and Peripheral Interfaces

The ZL38012 provides 1 master SPI port (with 2 chip selects), 1 slave SPI ports and an UART. The master SPI port's primary function is to access and external FLASH memory to download firmware to the ZL38012.

The control/status registers and memory of the ZL38012 can be accessed (R/W) by an external host through the Slave SPI and the UART ports. Register/Memory read and write accesses are carried out through a series of port read and write accesses as follows:

5.1 Master SPI (FLASH Port)

The Master SPI port is used by the ZL38012 to access one or two peripheral devices (chip select signals SPIM_CS[1:0]). It supports both SPI and MICROWIRE modes of operation and can write up to 40 bits or read up to 32 bits in a single access. The Chip Select output signals may be programmed for a single access or burst access. All communication is MSB first and all pins of the master SPI port are outputs controlled by the ZL38012, except SPIM_MISO.

5.2 Slave SPI (Host Port)

The slave SPI port may be used by an external host microprocessor to access (Read/Write) the ZL38012 internal control/status registers and memory. Access is initiated when the external host makes signal SPIS_CS low and is ended when this signal goes high. The host will then apply a clock (maximum 25 MHz) to signal SPIS_CLK to clock data out of SPIS_MISO and in on SPIS_MOSI.

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5.3 UART

The UART (Universal Asynchronous Receiver Transmitter) port may be used by an external host microprocessor to access (Read/Write) the ZL38012 internal control/status registers and memory. The ZL38012 DSP will set up the initial parameters of this port (i.e., master/slave, baud rate, stop bits, parity bit...) during the Boot process. After the device has been booted these port options can be changed as per the firmware manual.

The UART port will support 8-bit data only with any combination of 1 start bit, 0 or 1 parity bit(s) and 1, 1.5 or 2 stop bit(s).

The ZL38012 has 5 GPIO (General Purpose Input/Output) pins that can be individually configured as either input or output. These pins are intended for low frequency signalling.

When a GPIO pin is defined as an input the state of that input pin is sampled with the internal master clock (Mclk = 100 MHz) and latched into the GPIO Read Register. This sampling can be stopped (Freeze) on an individual GPIO pin. Individual pins of GPIO[2:0] may have an internal pull-down resistor activated/deactivated and individual pins of GPIO[3:4] may have an internal pull-up activated/deactivated.

Immediately after a power-on reset ($\overline{\text{RST}}$ pin) the GPIO pins are defined as inputs and their state is captured in the GPIO Start-Up Status Register. The state of this register is used by the Boot program to determine the base functionality and programming options of the device.

Individual GPIO pins may also be defined as outputs with associated enable/disable (active/high impedance) control.

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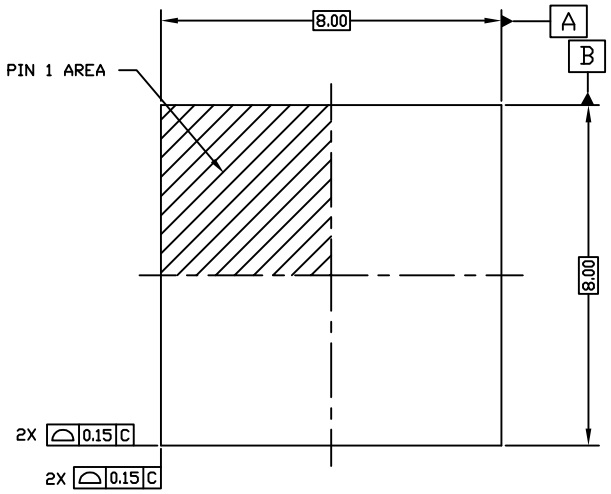
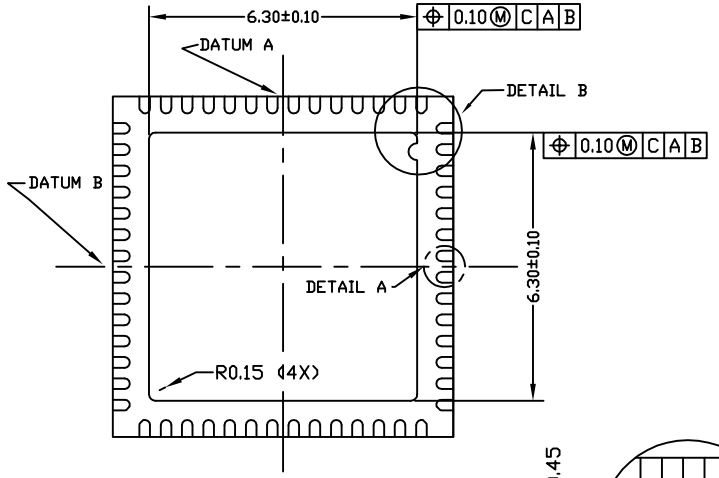
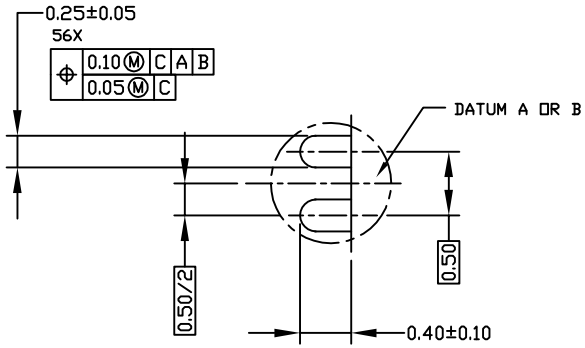
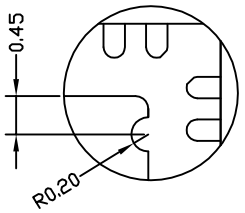


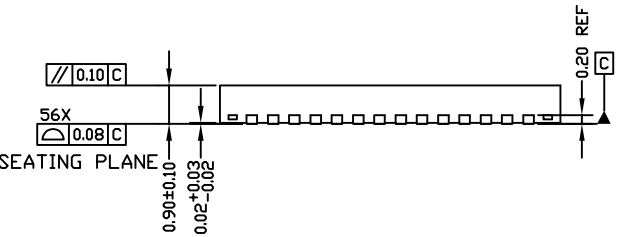




DETAIL A (SCALE 3:1)



DETAIL B (SCALE 2:1)



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E LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

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TITLE 56 QFN PACKAGE OUTLINE BODY SIZE : 8X8X0.90 mm PITCH : 0.50mm				SHEET 1 OF 1	SIZE A4
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