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1 Block diagram and pin description

Figure 1. Block diagram

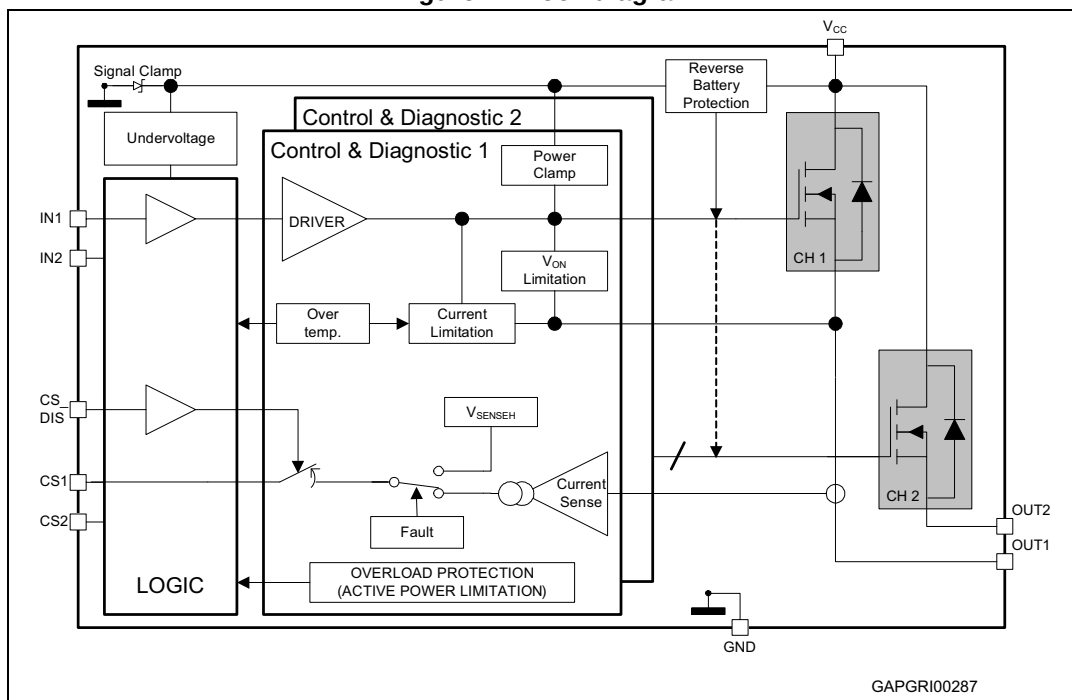


Table 1. Pin function

Name	Function
V _{CC}	Battery connection
OUT _{1,2}	Power output
GND	Ground connection
IN _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CS _{1,2}	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

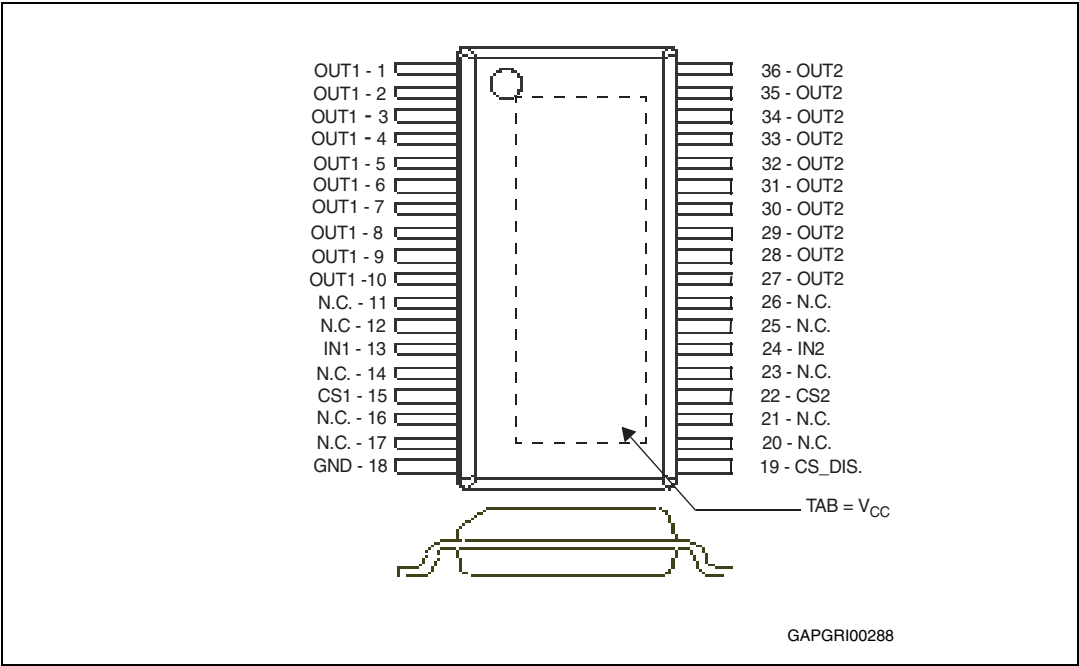
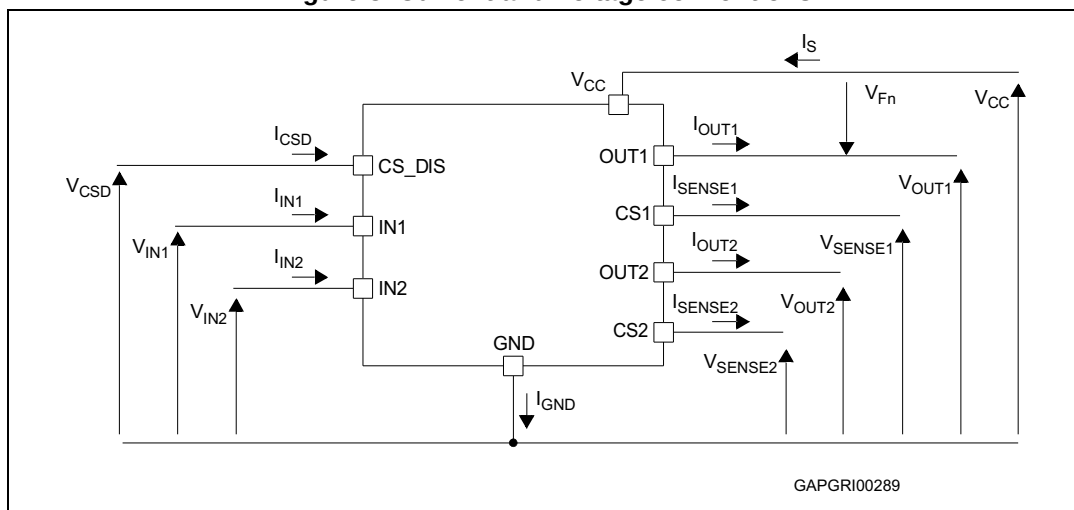


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 K Ω resistor	X	Not allowed	Through 10 K Ω resistor	Through 10 K Ω resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Applying stress which exceeds the ratings listed in the [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage ($T < 400\text{ms}$, $R_{LOAD} > 0.5\Omega$)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
V_{CC_LSC}	Maximum supply voltage for full protection to short-circuit (acc. AEC-Q100-012)	18	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	50	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 0.47\text{ mH}$; $R_L = 0\ \Omega$; $V_{bat} = 13.5\text{ V}$; $T_{jstart} = 150\text{ }^\circ\text{C}$; $I_{OUT} = I_{limL}(\text{Typ.})$)	110	mJ

Table 3. Absolute maximum rating (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: $R=1.5K\Omega$; $C=100pF$)		
	– V_{CC} , OUTPUT	5000	V
	– INPUT, CS_DIS	4000	
	– CURRENT SENSE	2000	
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX) (with one channel ON)	2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	See Figure 33 in the thermal section	°C/W

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 28V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	$I_{OUT} = 5A$; $T_j = 25^{\circ}C$		11		m Ω
		$I_{OUT} = 5A$; $T_j = 150^{\circ}C$			24	m Ω
		$I_{OUT} = 5A$; $V_{CC} = 5V$; $T_j = 25^{\circ}C$			16	m Ω
$R_{ON REV}$	Reverse battery on-state resistance	$V_{CC} = -13V$; $I_{OUT} = -5A$; $T_j = 25^{\circ}C$			12	m Ω
V_{clamp}	Clamp voltage	$I_S = 20 mA$	41	46	52	V
I_S	Supply current	Off-state; $V_{CC} = 13V$; $T_j = 25^{\circ}C$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0V$		2 ⁽¹⁾	5 ⁽¹⁾	μA
		On-state; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$		3.5	6.5	mA
$I_{L(off)}$	Off-state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$	0	0.01	3	
		$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$	0		5	μA

1. PowerMOS leakage included.

2. For each channel.

Table 6. Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 2.6\Omega$ (see Figure 5)	-	30	-	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 2.6\Omega$ (see Figure 5)	-	20	-	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 2.6\Omega$	-	See Figure 24	-	V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 2.6\Omega$	-	See Figure 25	-	V/ μs
W_{ON}	Switching energy losses during t_{WON}	$R_L = 2.6\Omega$ (see Figure 5)	-	1	-	mJ
W_{OFF}	Switching energy losses during t_{WOFF}	$R_L = 2.6\Omega$ (see Figure 5)	-	0.5	-	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9V$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	5.5	-0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9V$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1V$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1mA$ $I_{CSD} = -1mA$	5.5	-0.7	7	V V

Table 8. Protections and diagnostics ⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{CC} = 13V$ $5V < V_{CC} < 18V$	52	74	104 104	A A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13V$; $T_R < T_J < T_{TSD}$		18.5		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}C$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
T_{RS}	Thermal reset of status		135			$^{\circ}C$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}C$
V_{DEMG}	Turn-off output voltage clamp	$I_{OUT} = 2A$; $V_{IN} = 0$; $L = 6mH$	$V_{CC} - 28$	$V_{CC} - 31$	$V_{CC} - 35$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.4A$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ (see Figure 7)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} =0.25A; V _{SENSE} =0.5V T _J = -40°C...150°C	2615	5130	7770	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} =5A; V _{SENSE} =0.5V T _J =-40°C...150°C T _J =25°C...150°C	4155 4530	5330 5330	6650 6130	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} =5A; V _{SENSE} = 0.5V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-8		8	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} =10A; V _{SENSE} =4V T _J =-40°C...150°C T _J =25°C...150°C	4705 4865	5290 5290	5950 5715	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-5		5	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} =25A; V _{SENSE} =4V T _J =-40°C...150°C T _J =25°C...150°C	4935 4985	5250 5250	5565 5515	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 25 A; V _{SENSE} = 4 V; V _{CSD} = 0V; T _J = -40 °C to 150 °C	-4		4	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _J =-40°C...150°C	0		1	μA
		V _{CSD} =0V; V _{IN} =5V; T _J =-40°C...150°C	0		2	μA
		I _{OUT} =5A; V _{SENSE} =0V; V _{CSD} =V _{IN} =5V;	0		1	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} =15A; V _{CSD} =0V	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	V _{CC} =13V; R _{SENSE} =10KΩ		8		V
I _{SENSEH}	Analog sense output current in fault condition ⁽²⁾	V _{CC} =13V; V _{SENSE} =5V		9		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		5	20	μs

Table 9. Current sense (8V<V_{CC}<18V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} <4V, 1.5A<I _{out} <25A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		70	300	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} = 5A (see Figure 6)			300	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} <4V, 1.5A<I _{out} <25A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		100	250	μs

- 1. Parameter guaranteed by design; it is not tested.
- 2. Fault condition includes: power limitation and overtemperature.

Figure 4. Current sense delay characteristics

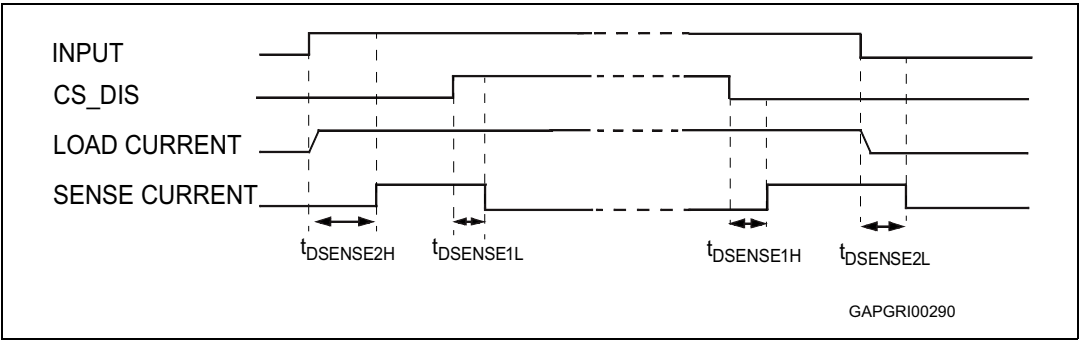


Figure 5. Switching characteristics

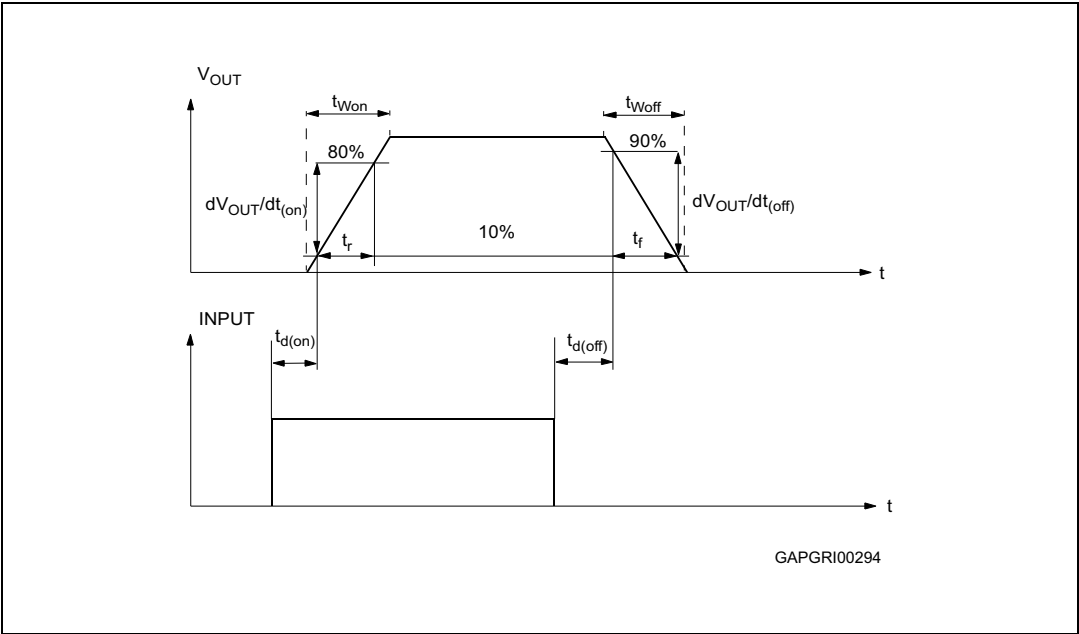


Figure 6. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

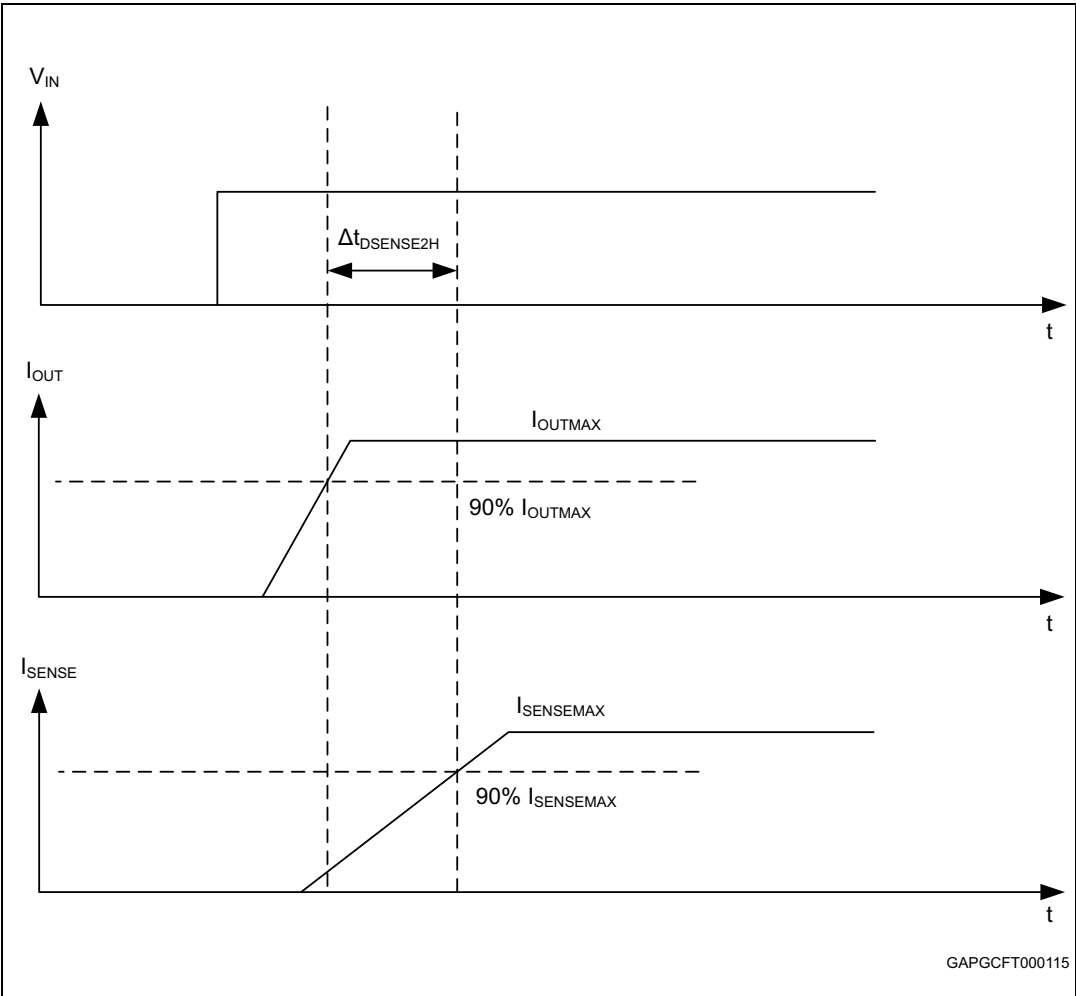


Figure 7. Output voltage drop limitation

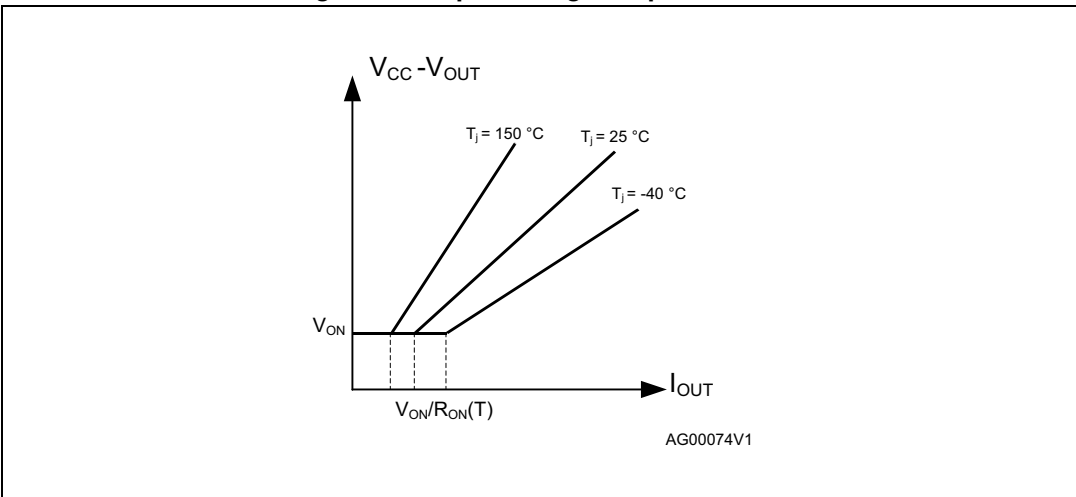


Figure 8. I_{OUT}/I_{SENSE} vs I_{OUT}

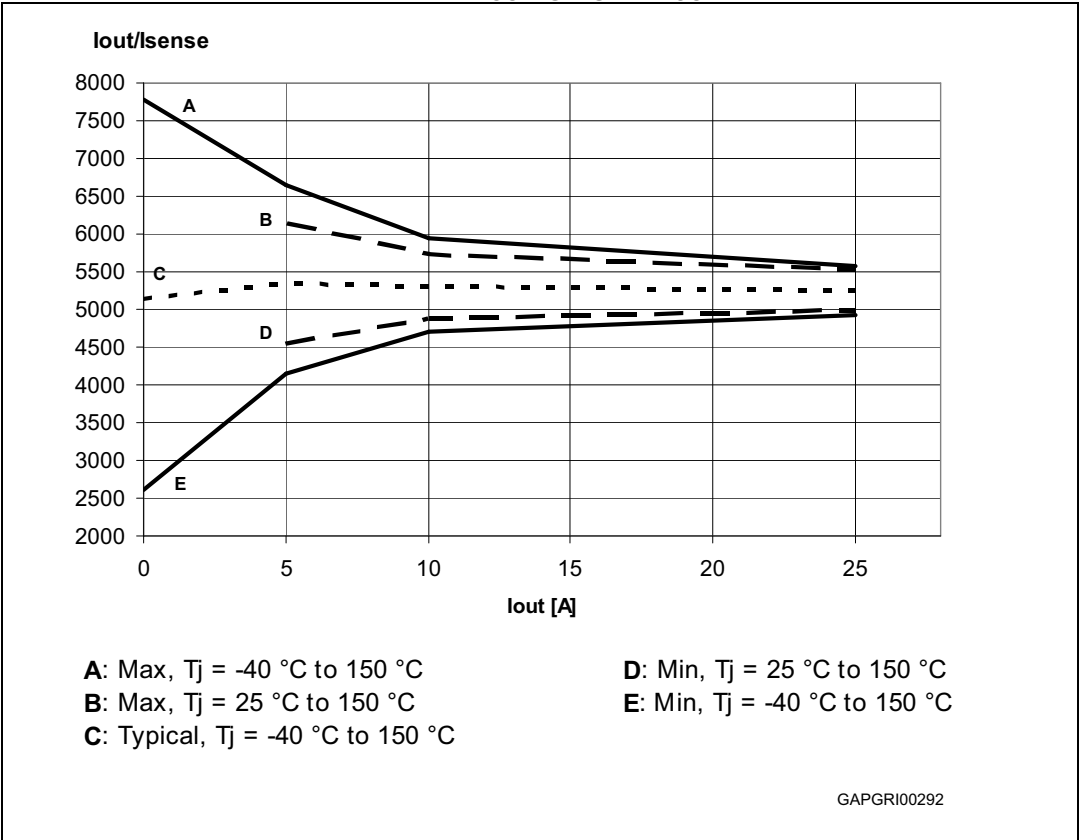
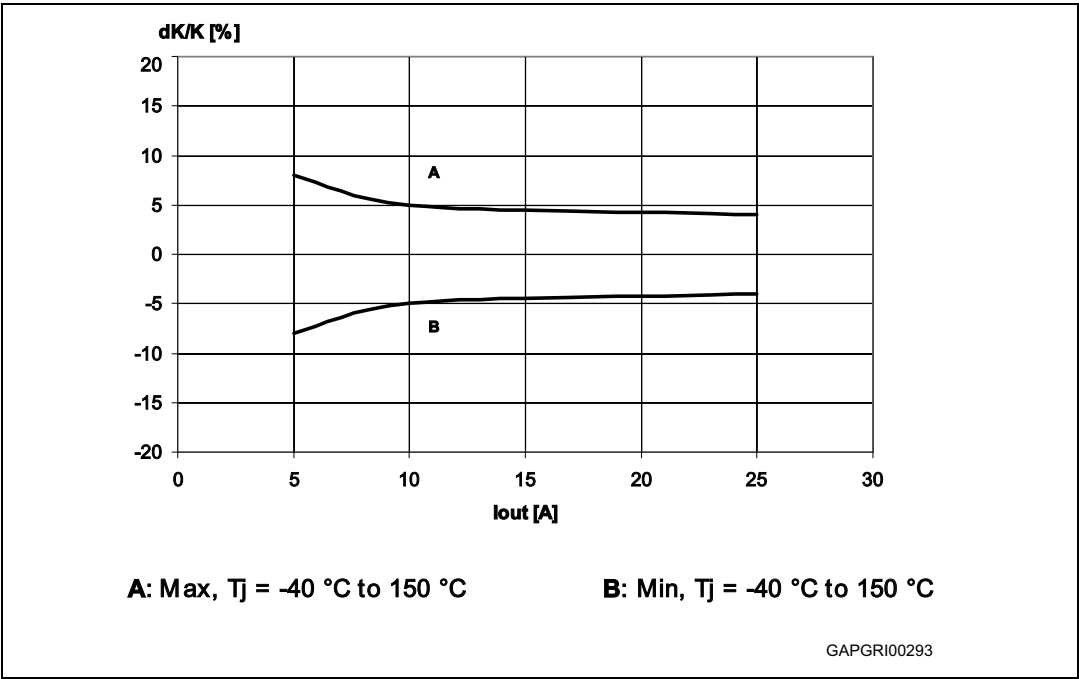


Figure 9. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense ($V_{CSD}=0V$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (Power limitation)	L	L	0
	H	L	V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾⁽³⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 3: Absolute maximum rating](#).

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 10. Normal operation

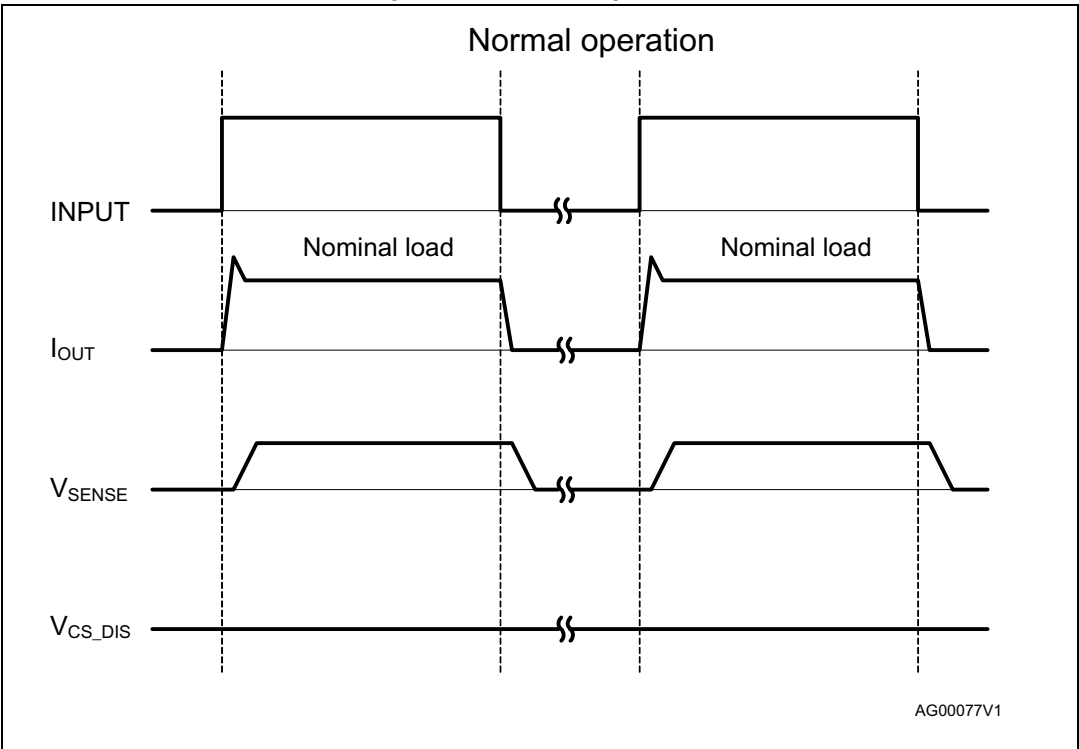


Figure 11. Overload or short to GND

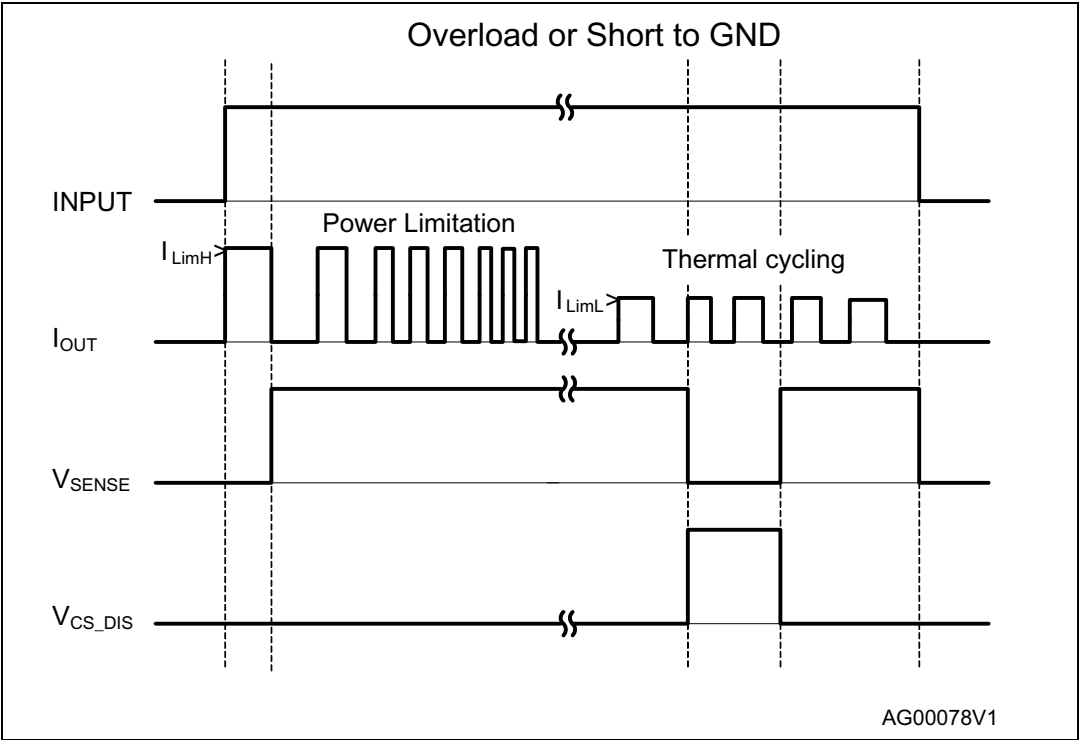


Figure 12. Intermittent overload

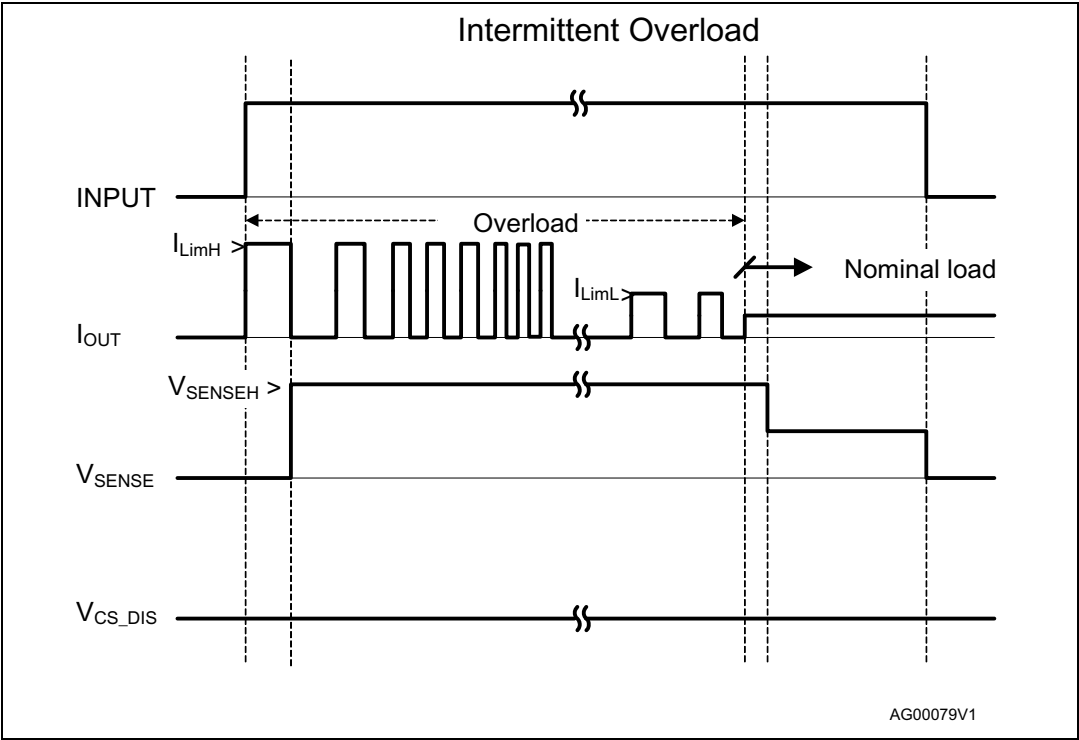
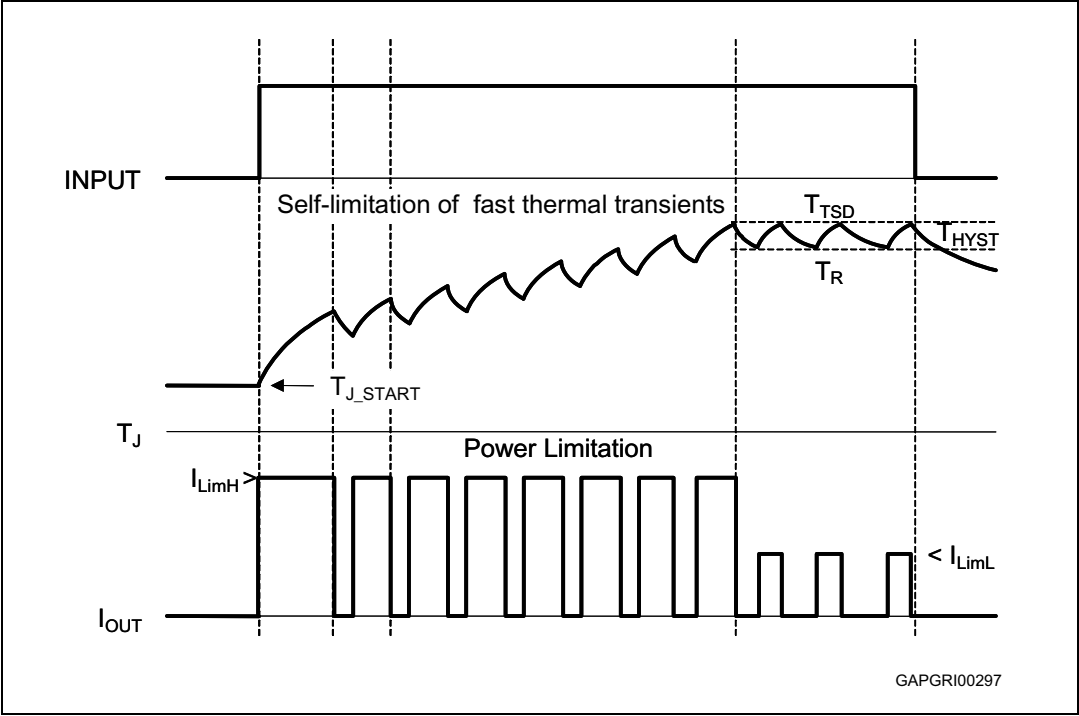


Figure 13. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 14. Off-state output current

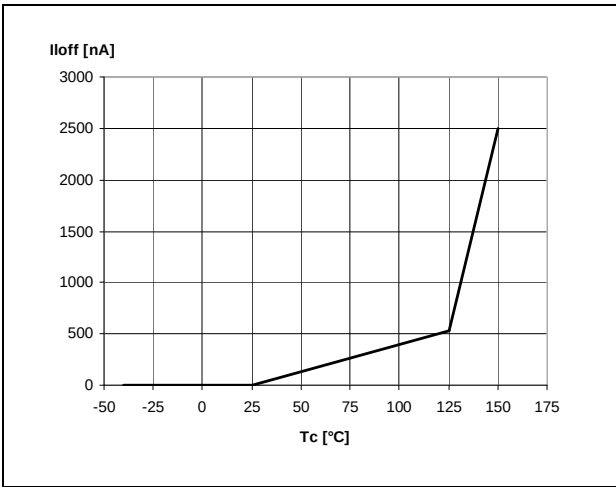


Figure 15. High level input current

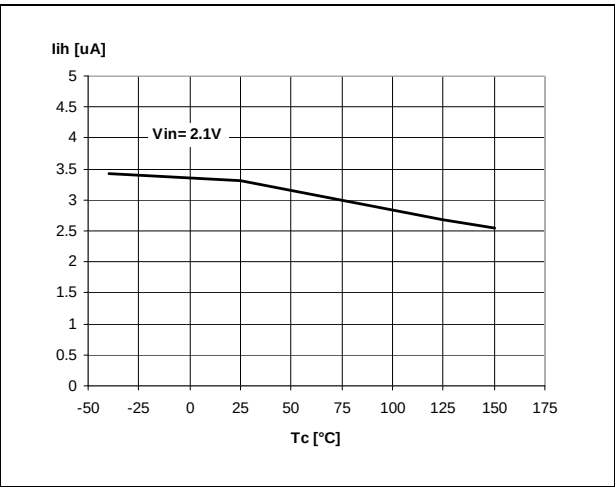


Figure 16. Input clamp voltage

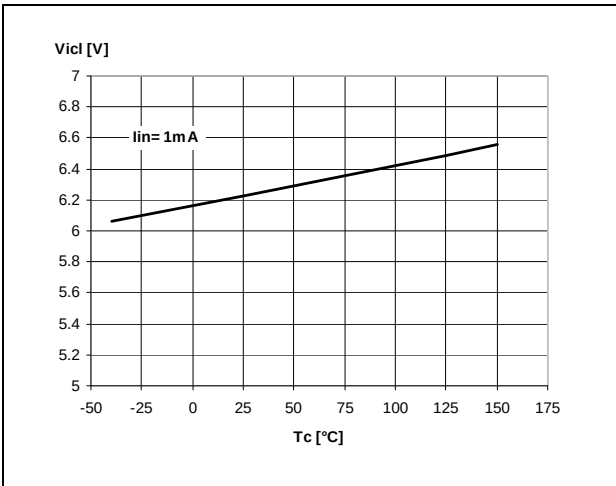


Figure 17. Input high level voltage

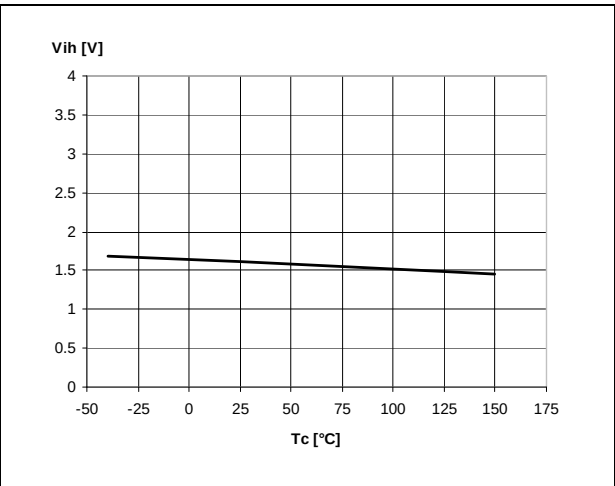


Figure 18. Input low level voltage

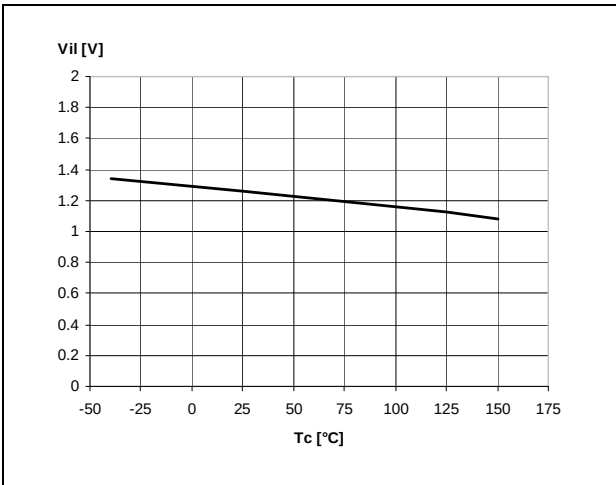


Figure 19. Input hysteresis voltage

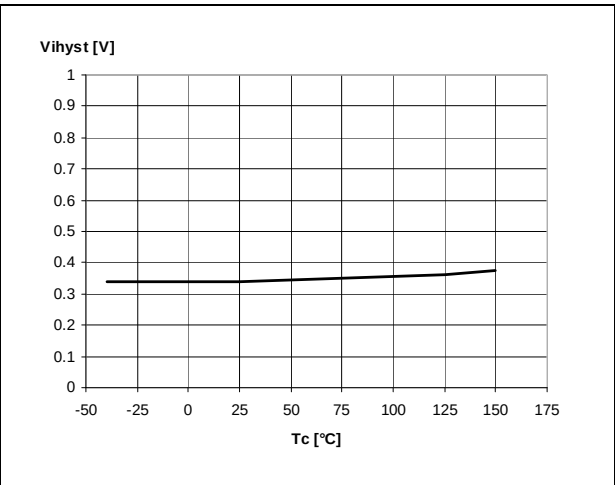


Figure 20. On-state resistance vs T_{case}

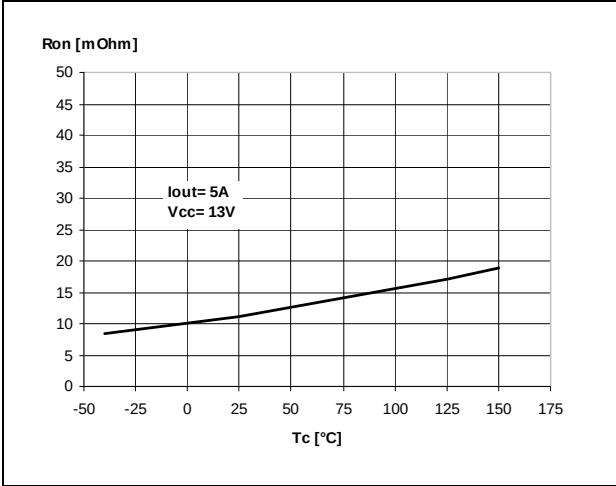


Figure 21. On-state resistance vs V_{CC}

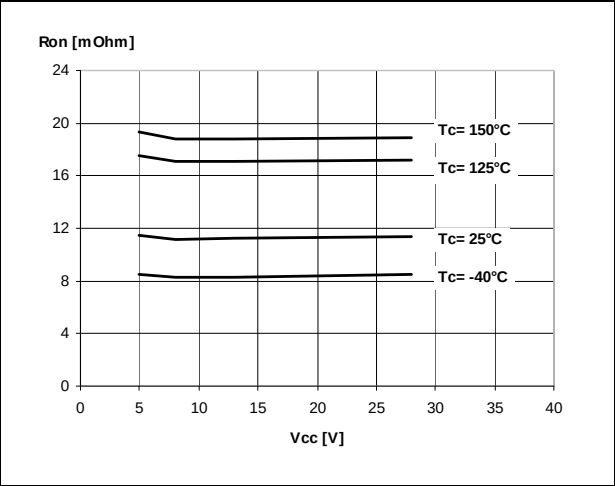


Figure 22. Undervoltage shutdown

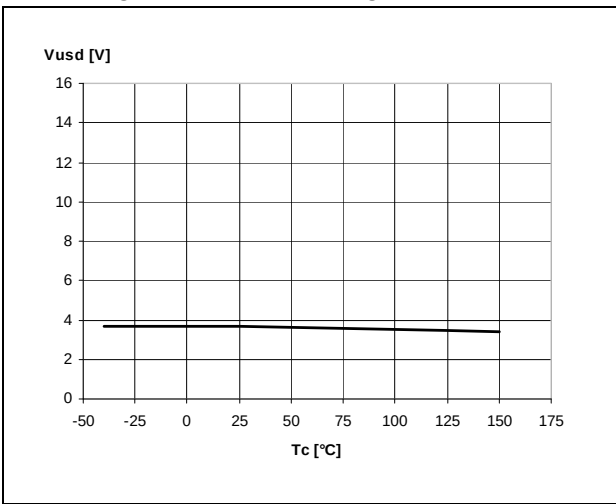


Figure 23. I_{LIMH} vs T_{case}

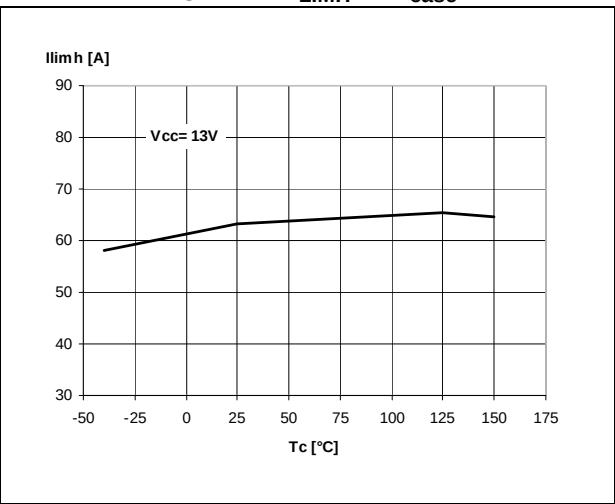


Figure 24. Turn-on voltage slope

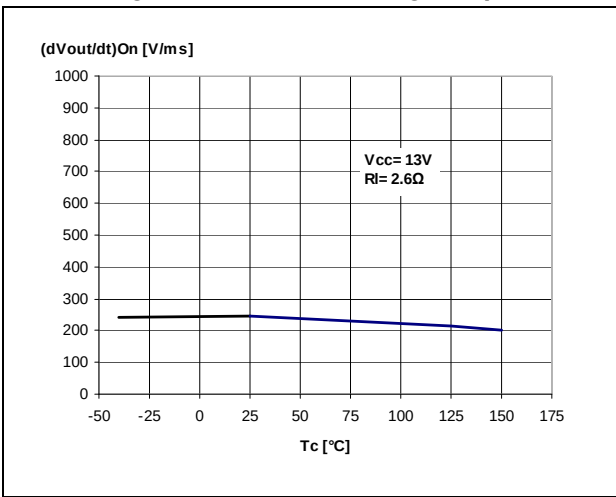


Figure 25. Turn-off voltage slope

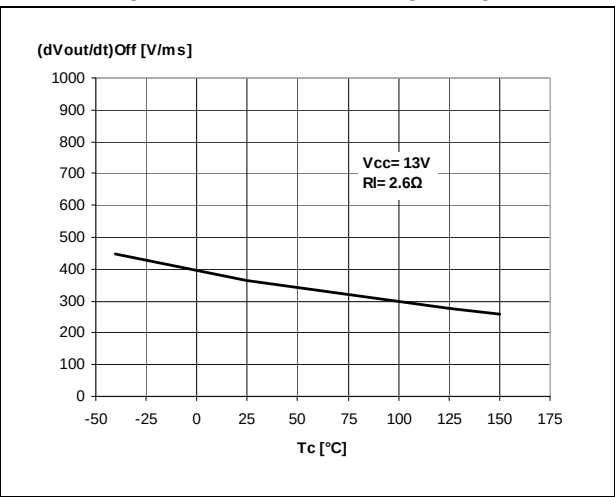


Figure 26. CS_DIS clamp voltage

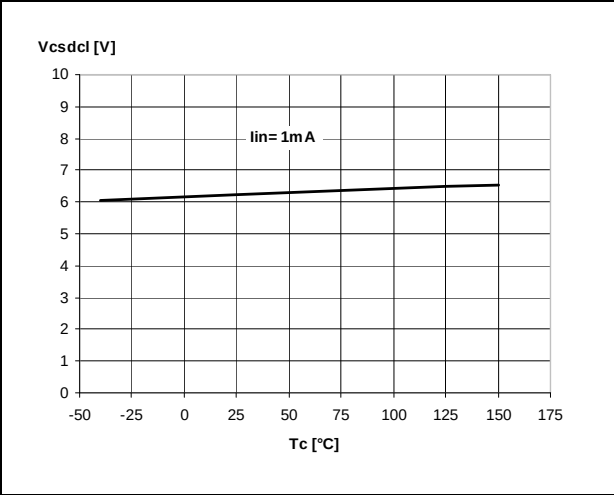


Figure 27. Low level CS_DIS voltage

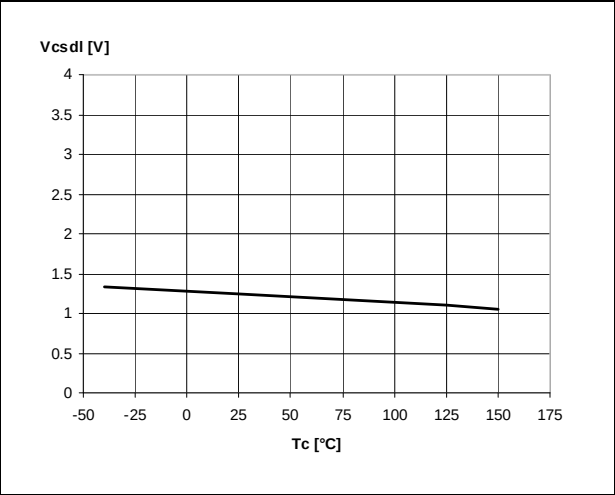
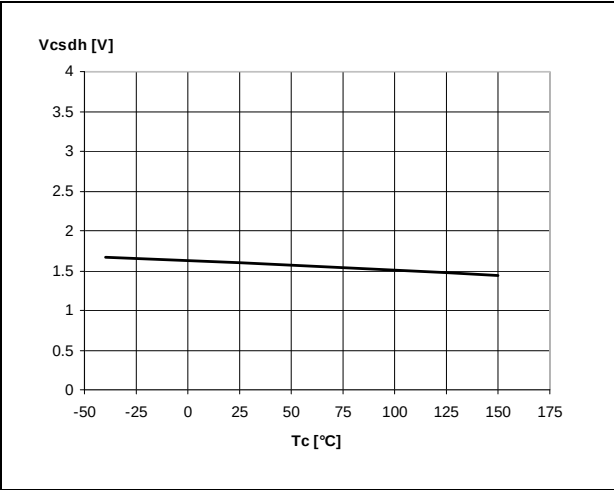
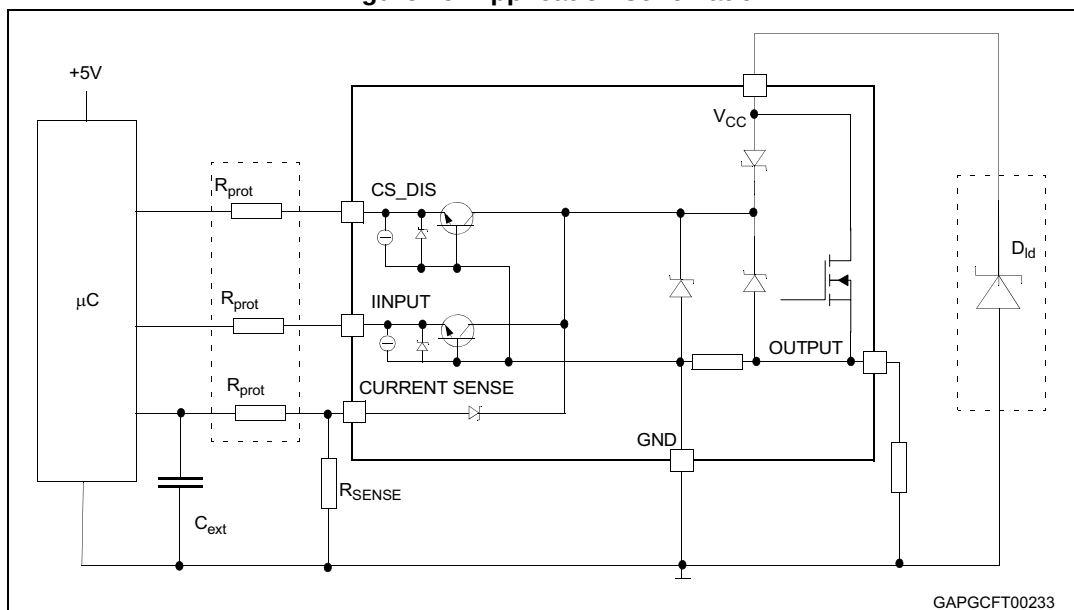


Figure 28. High level CS_DIS voltage



3 Application information

Figure 29. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pin is pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH})/I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -1.5$ V; $I_{latchup} \geq 20$ mA; $V_{OH\mu C} \geq 4.5$ V

$$75 \Omega \leq R_{prot} \leq 240 \text{ k}\Omega.$$

Recommended values: $R_{\text{prot}} = 10 \text{ k}\Omega$, $C_{\text{EXT}} = 10 \text{ nF}$.

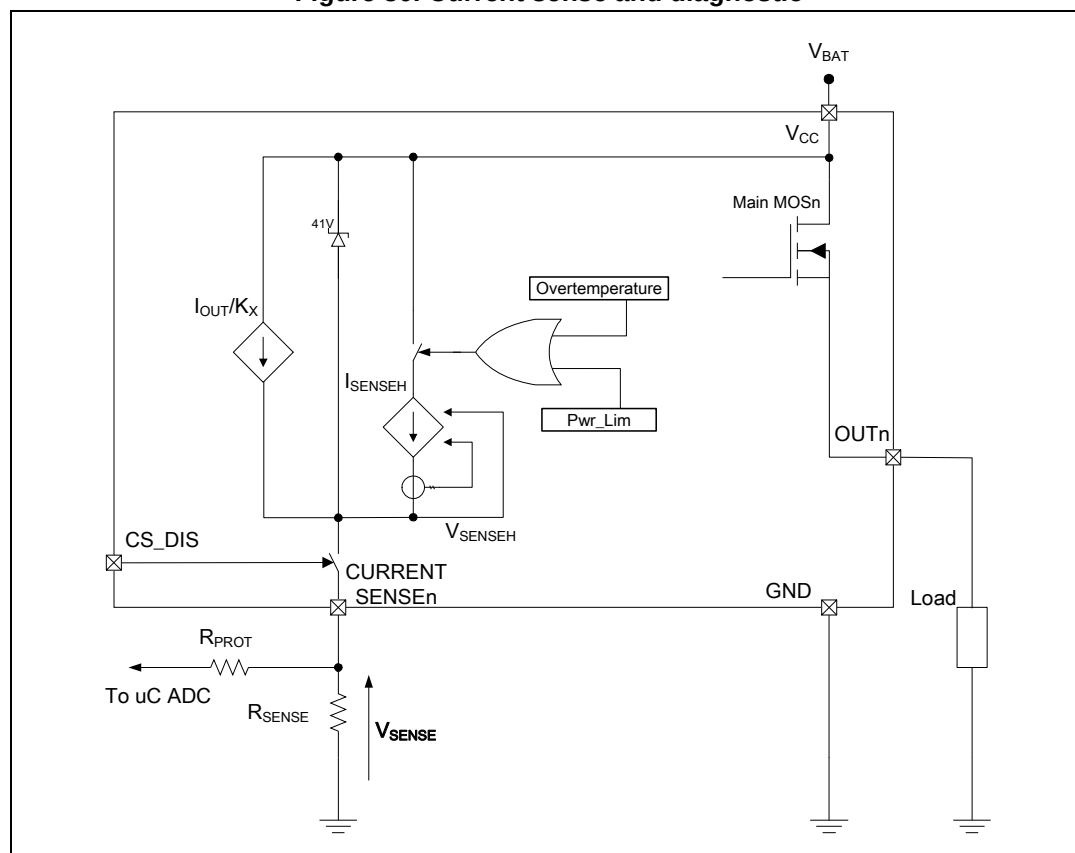
3.3 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 30: Current sense and diagnostic](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_X .
The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in [Table 9: Current sense \(\$8V < V_{\text{CC}} < 18V\$ \)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 9: Current sense \(\$8V < V_{\text{CC}} < 18V\$ \)](#)).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to [Truth table](#)):
 - Power limitation activation
 - Overtemperature

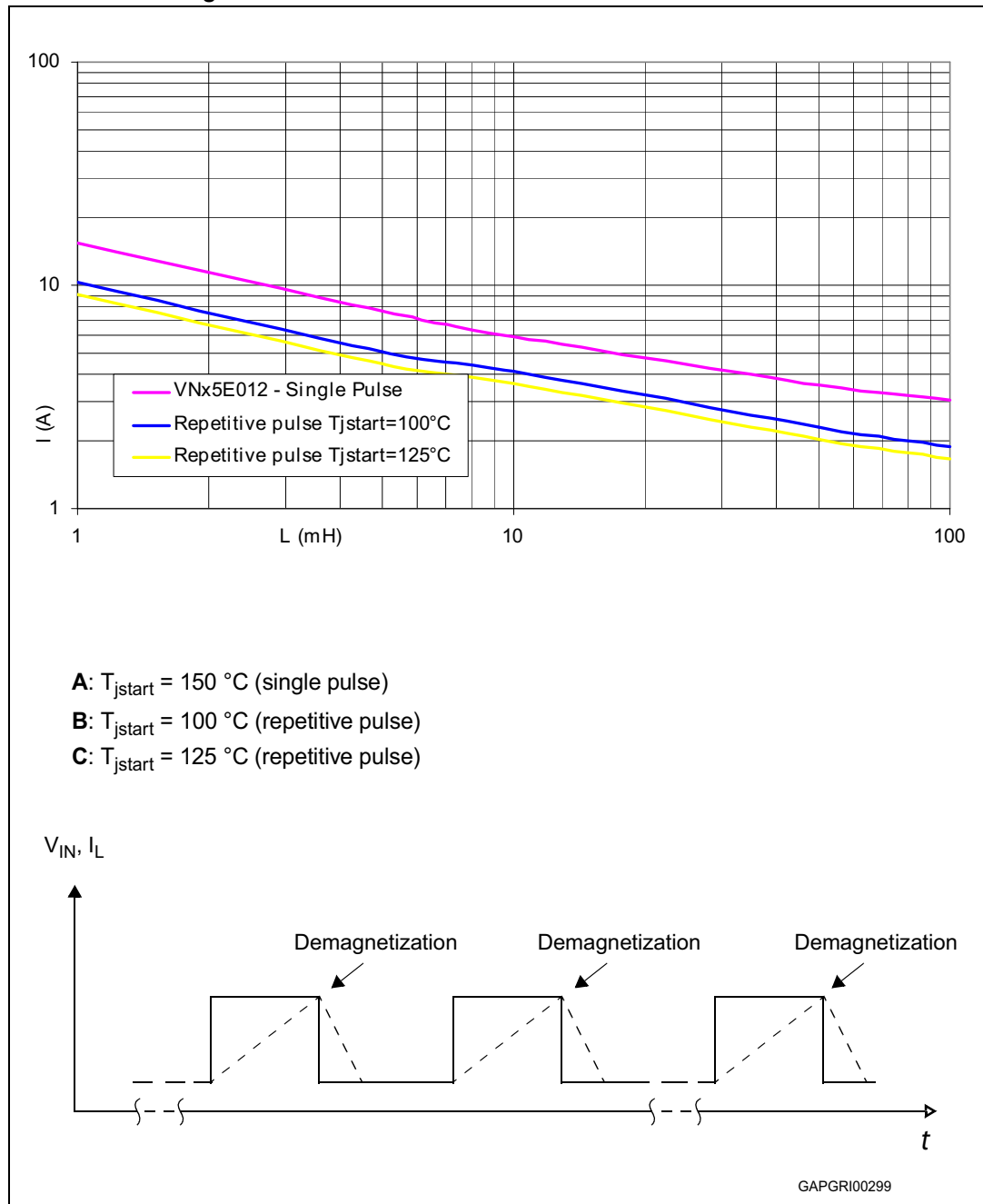
A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 30. Current sense and diagnostic



3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 31. Maximum turn-off current versus inductance



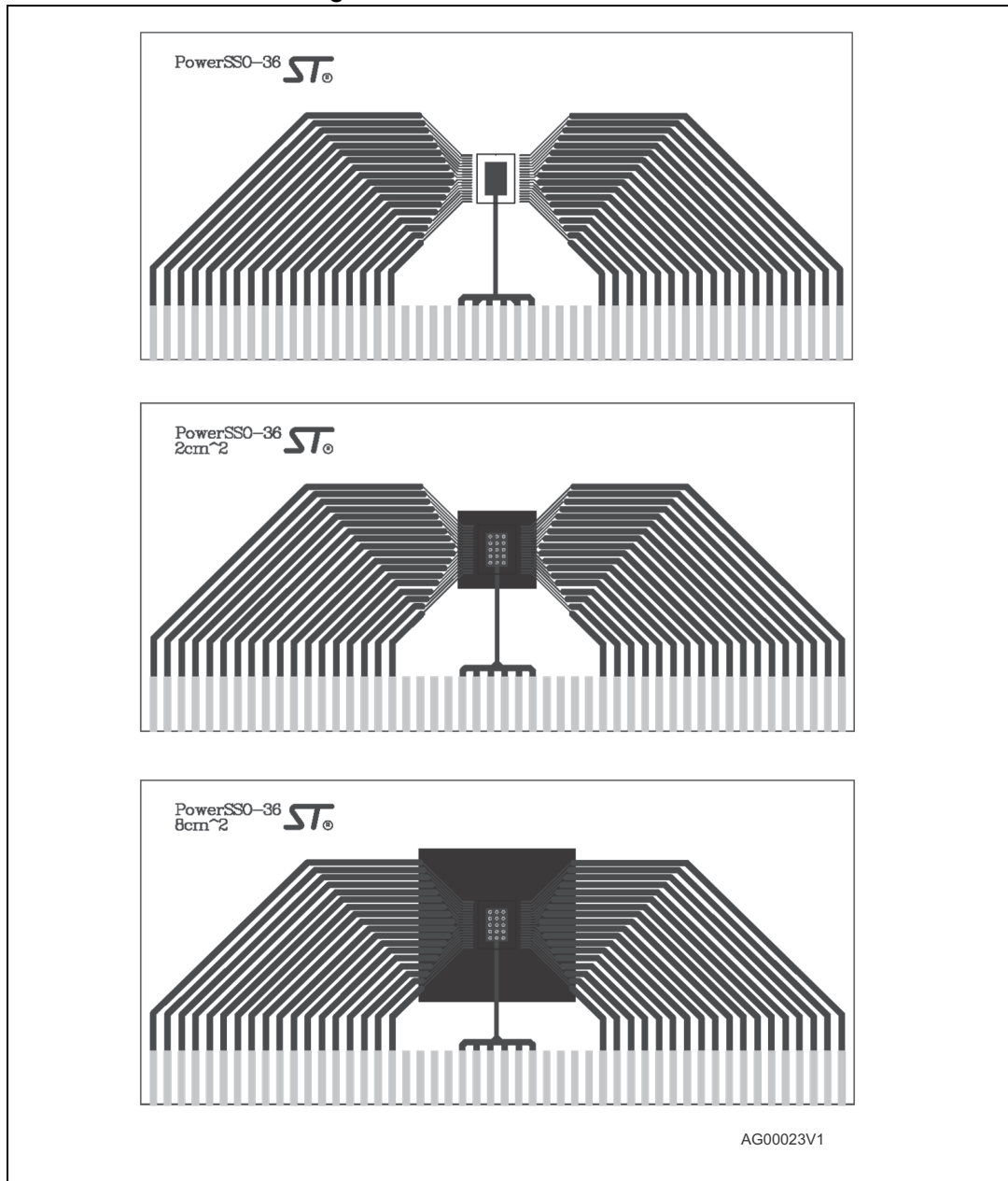
Note: Values are generated with $R_L = 0 \Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-36 thermal data

Figure 32. PowerSSO-36 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 129mm x 60mm, PCB thickness=1.6mm, Cu thickness=70μm (front and back side), Copper areas: from minimum pad lay-out to 8 cm²).

Figure 33. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

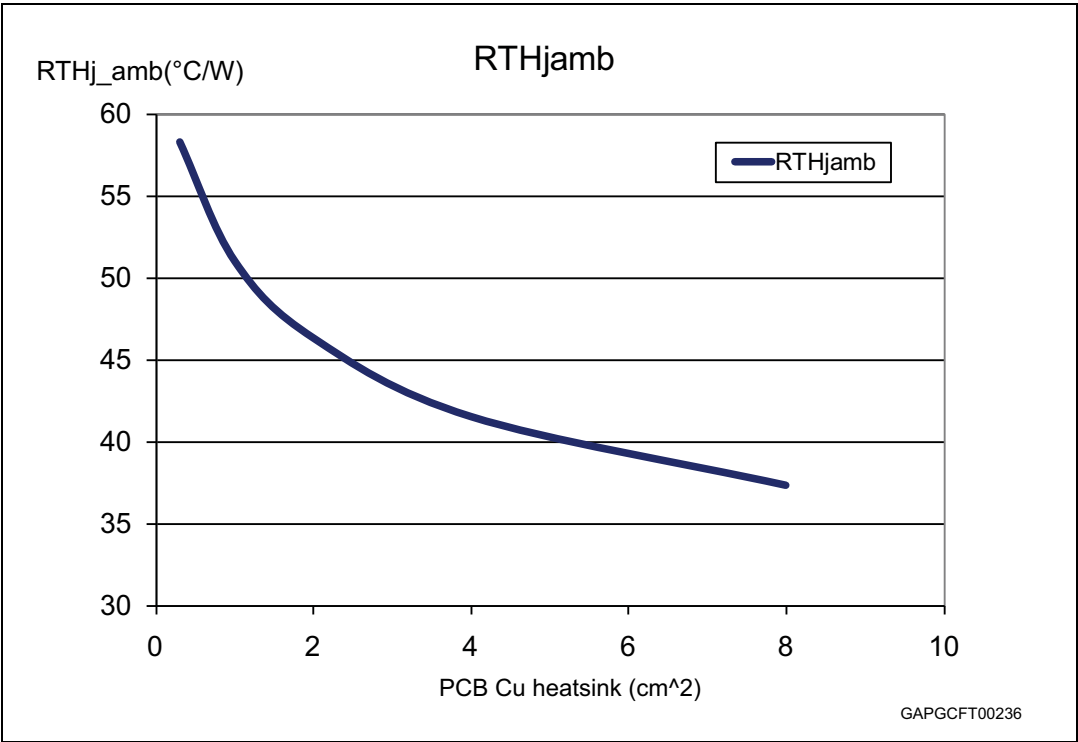


Figure 34. PowerSSO-36 thermal impedance junction ambient single pulse (one channel ON)

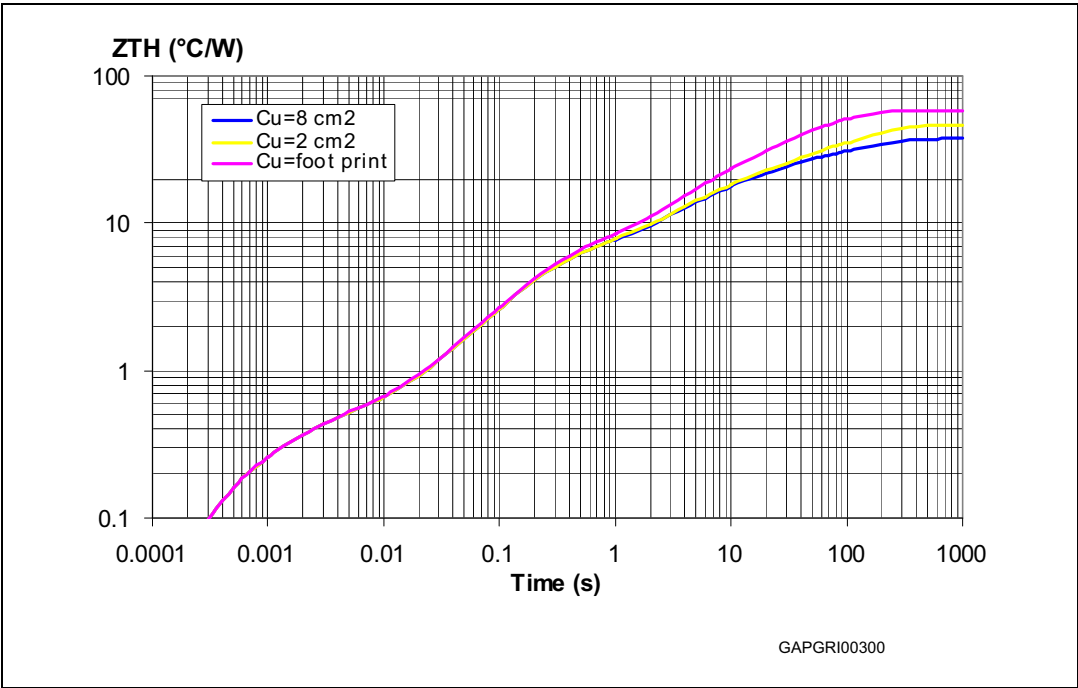
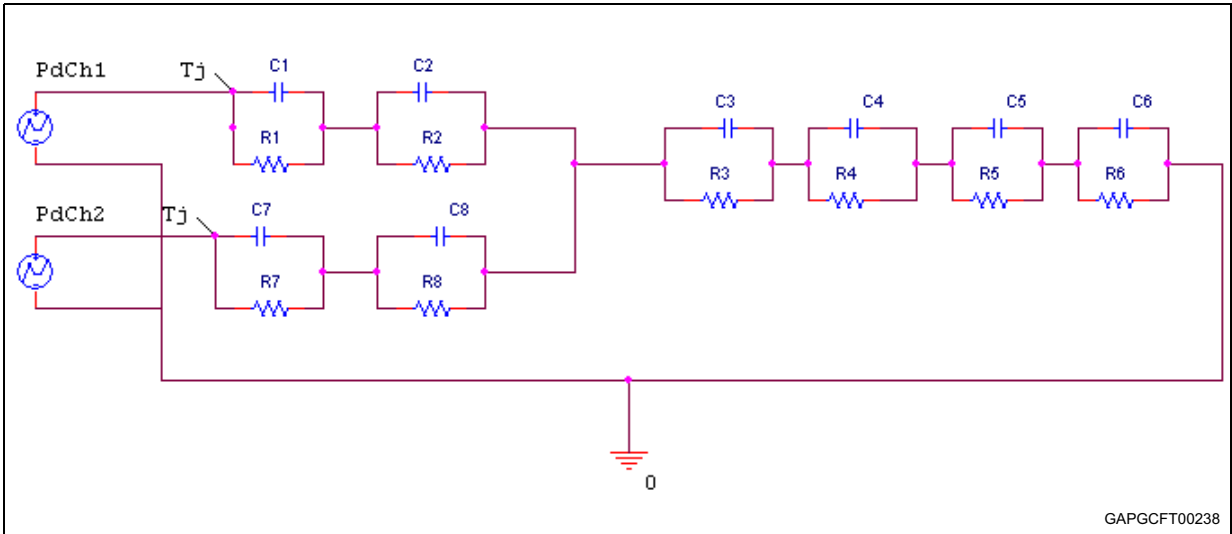


Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-36⁽¹⁾



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 14. Thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.1		
R2 (°C/W)	0.3		
R3 (°C/W)	5		
R4 (°C/W)	8		
R5 (°C/W)	18	10	10
R6 (°C/W)	27	23	14
R7 (°C/W)	0.1		
R8 (°C/W)	0.3		
C1 (W.s/°C)	0.0025		
C2 (W.s/°C)	0.005		
C3 (W.s/°C)	0.04		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	2	2
C6 (W.s/°C)	3	6	9

Table 14. Thermal parameter

Area/island (cm ²)	Footprint	2	8
C7 (W.s/°C)	0.0025		
C8 (W.s/°C)	0.005		

5 Package information

5.1 ECOPACK[®] package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.2 PowerSSO-36 mechanical data

Figure 36. PowerSSO-36 package dimensions

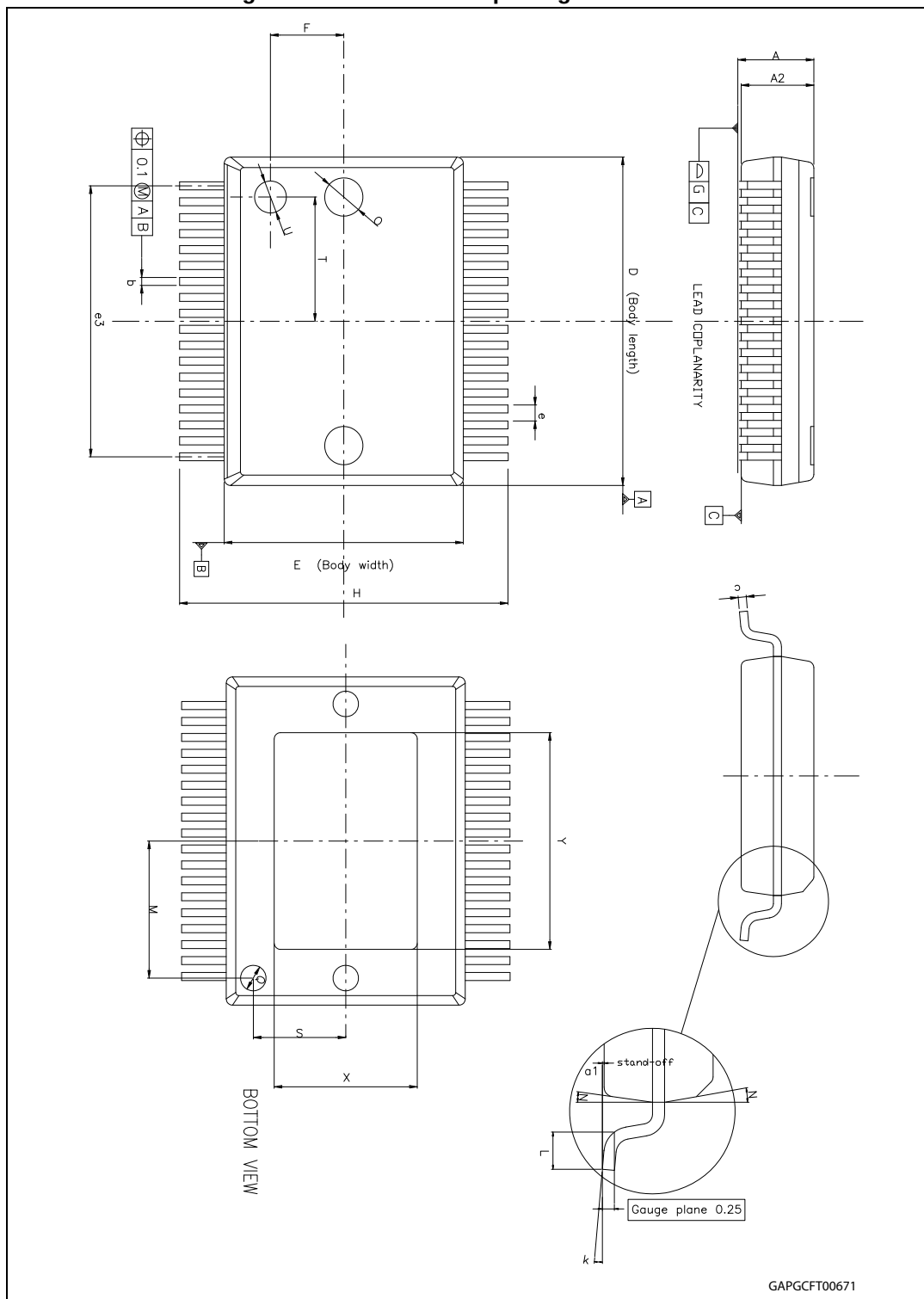


Table 15. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.47
A2	2.15	-	2.40
a1	0	-	0.075
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
L	0.55	-	0.85
N	-	-	10 deg
X	4.1	-	4.7
Y	6.5	-	7.1

5.3 Packing information

Figure 37. PowerSSO-36 tube shipment (no suffix)

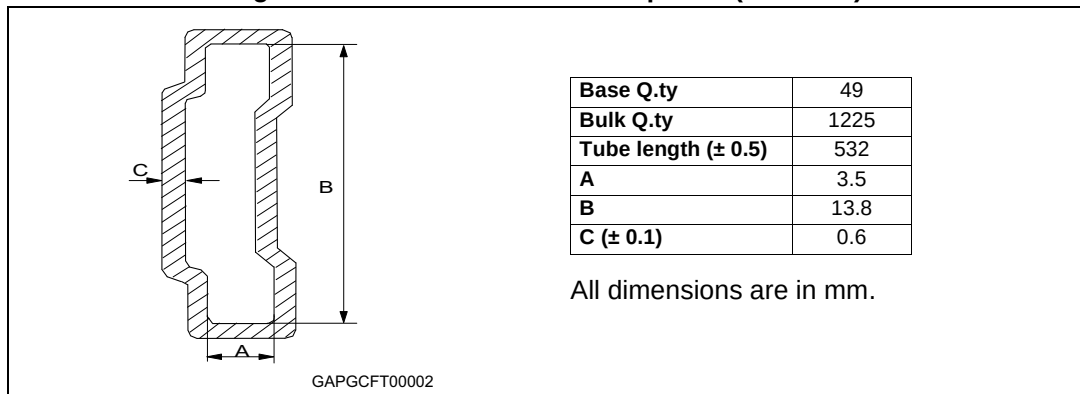
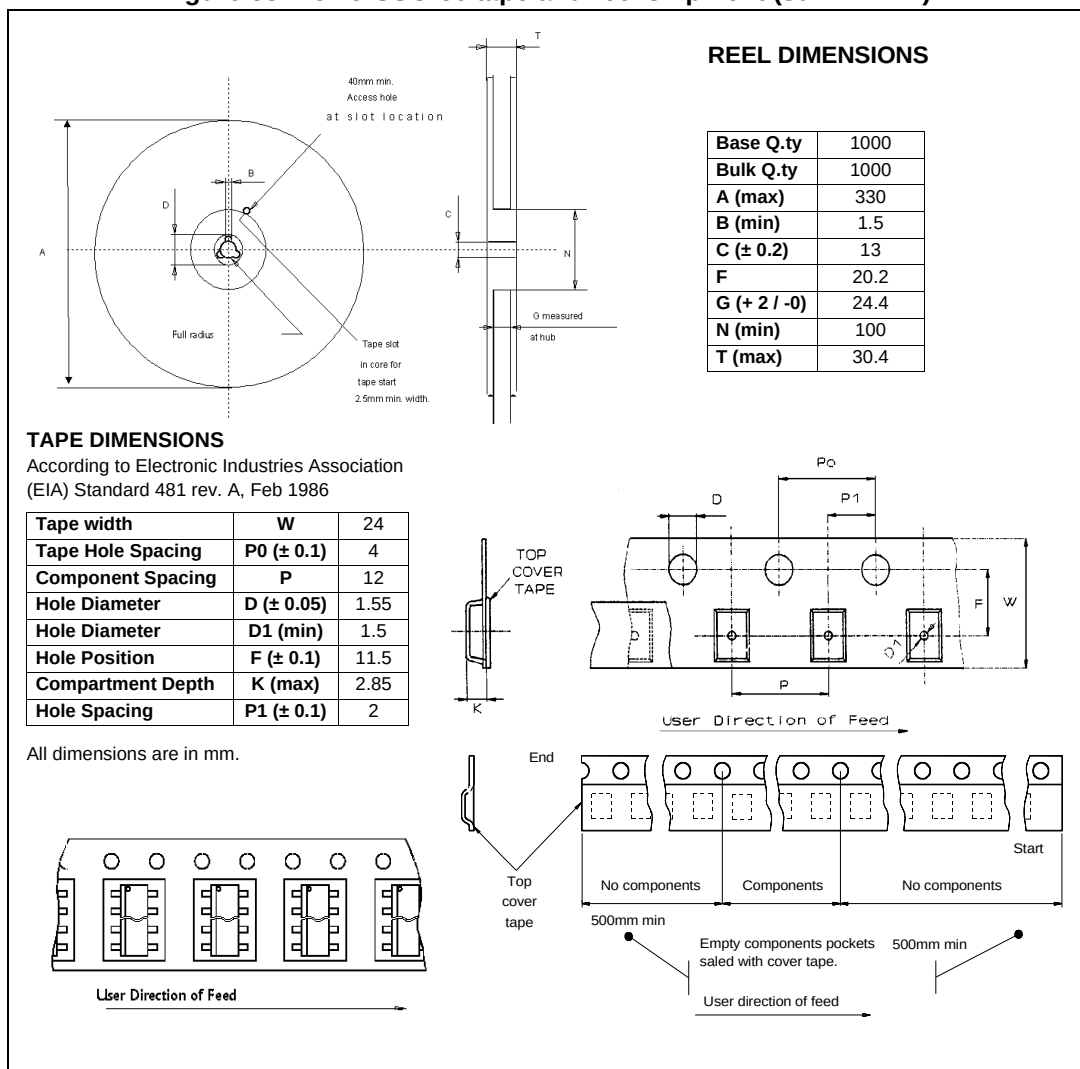


Figure 38. PowerSSO-36 tape and reel shipment (suffix "TR")



6 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VND5E012MY-E	VND5E012MYTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
21-Oct-2009	1	Initial release.
04-Dec-2009	2	Updated Section 4.1: PowerSSO-36 thermal data
11-July-2012	3	Updated Figure 36: PowerSSO-36 package dimensions
19-Sep-2013	4	Updated Disclaimer.
24-Oct-2013	5	Updated footnote 2 into the Table 11: Electrical transient requirements (part 1) and Table 12: Electrical transient requirements (part 2) .

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