designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

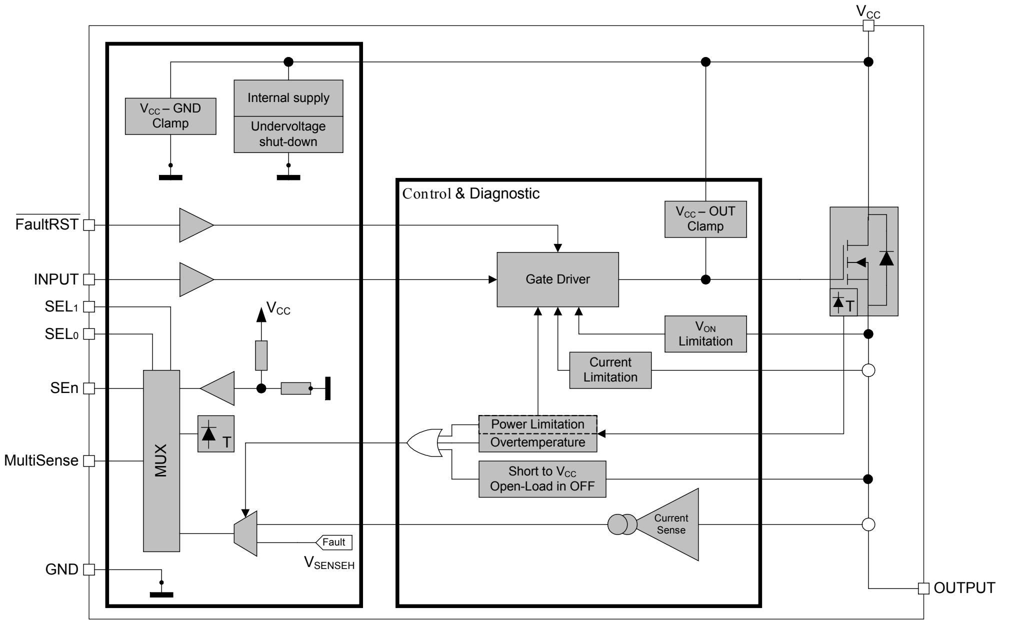
A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

1 Block diagram and pin description

Figure 1. Block diagram



GAPGCFT00328

Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power outputs. All the pins must be connected together.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

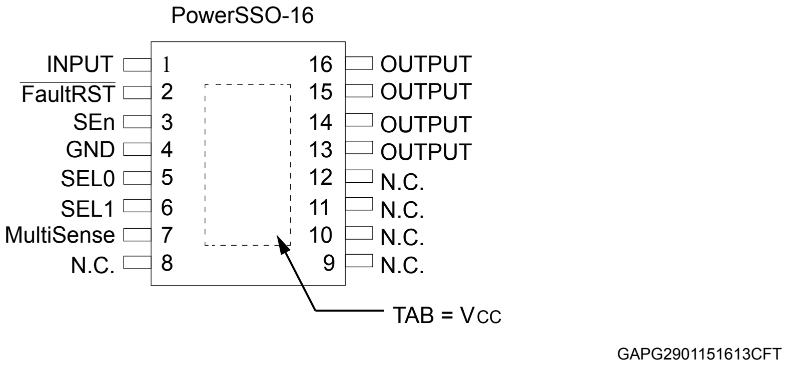


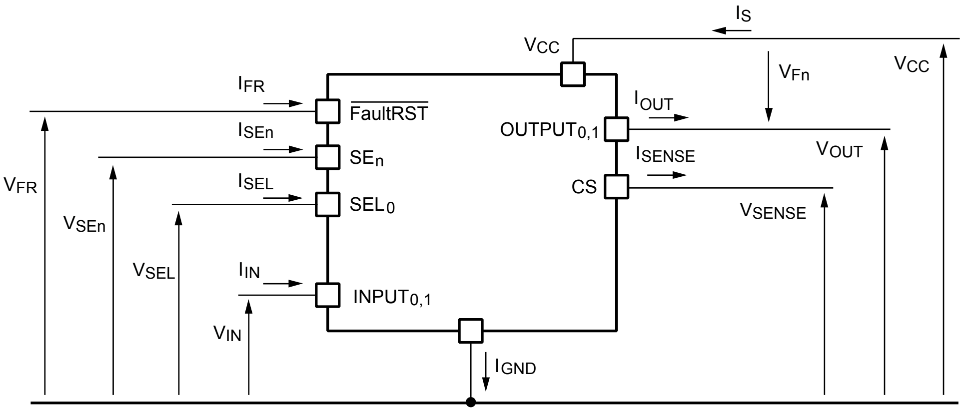
Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, FaultRST
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. *X: do not care.*

2 Electrical specification

Figure 3. **Current and voltage conventions**



GADG2203170950PS

Note: *$V_F = V_{OUT} - V_{CC}$ during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4\ \Omega$)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	17	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	MultiSense pin DC output current in reverse ($V_{CC} < 0$ V)	-20	
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4$ ms; $T_{jstart} = 150$ °C)	64	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) • INPUT • MultiSense • SEn, $SEL_{0,1}$, FaultRST • OUTPUT • V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. **Thermal data**

Symbol	Parameter	Typ. value	Unit
$R_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8)(1)	5.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(2)	57	
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)	23	

1. *Device mounted on four-layers 2s2p PCB*
2. *Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace*

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. **Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	V
$V_{USDReset}$	Undervoltage shutdown reset				5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
R_{ON}	On-state resistance	I_{OUT} = 3 A; T_j = 25°C		20		mΩ
		I_{OUT} = 3 A; T_j = 150°C			40	
		I_{OUT} = 3 A; V_{CC} = 4 V; T_j = 25°C			30	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	V
		I_S = 20 mA; T_j = -40°C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V(1)	V_{CC} = 13 V; $V_{IN} = V_{OUT} = V_{FR} = V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; $V_{IN} = V_{OUT} = V_{FR} = V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C(2)			0.5	
		V_{CC} = 13 V; $V_{IN} = V_{OUT} = V_{FR} = V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; $V_{IN} = V_{OUT}$ = $V_{FR} = V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; $V_{SEn} = V_{FR} = V_{SEL0,1}$ = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A		3	5	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; $V_{FR} = V_{SEL0,1}$ = 0 V; V_{IN} = 5 V; I_{OUT} = 3 A			6	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V	$V_{IN} = V_{OUT}$ = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		$V_{IN} = V_{OUT}$ = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -3 A; T_j = 150°C			0.7	V

1. *PowerMOS leakage included.*
2. *Parameter specified by design; not subject to production test.*

Table 6. Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 4.3 Ω	10	60	120	µs
$t_{d(off)}$ (1)	Turn-off delay time at T_j = 25 °C		10	40	100	
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope at T_j = 25 °C	R_L = 4.3 Ω	0.1	0.28	0.7	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope at T_j = 25 °C		0.1	0.32	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 4.3 Ω	—	0.36	0.54 (2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 4.3 Ω	—	0.37	0.54(2)	mJ
t_{SKEW} (1)	Differential pulse skew (t_{PHL} - t_{PLH})	R_L = 4.3 Ω	-75	-25	25	µs

1. *See Figure 6. Switching time and pulse skew.*

2. *Parameter guaranteed by design and characterization; not subject to production test.*

Table 7. **Logic inputs**

$7\ V < V_{CC} < 28\ V; -40°C < T_j < 150°C$						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
INPUT characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics ($7\ V < V_{CC} < 18\ V$)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics ($7\ V < V_{CC} < 18\ V$)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8. Protections

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	45	63	90	A
		4 V < V_{CC} < 18 V (1)				
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		23		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(1)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	3	10	20	μs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40°C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.5 A		20		mV

1. *Parameter guaranteed by design and characterization; not subject to production test.*

Table 9. MultiSense

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
CurrentSense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	550			
dK_{cal}/K_{cal} (1) (2)	Current sense ratio drift at calibration point	I_{OUT} = 0.01 A to 0.05 A; I_{cal} = 30 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.1 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	1800	3630	5100	
dK_{LED}/K_{LED} (1) (2)	Current sense ratio drift	I_{OUT} = 0.1 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	2230	3200	4120	
dK_0/K_0 (1) (2)	Current sense ratio drift	I_{OUT} = 0.5 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	2180	2970	3900	
dK_1/K_1 (1) (2)	Current sense ratio drift	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	2450	2880	3320	

$7\ V < V_{CC} < 18\ V$; $-40°C < T_j < 150°C$						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
dK_2/K_2 (1) (2)	Current sense ratio drift	$I_{OUT} = 3\ A$; $V_{SENSE} = 4\ V$; $V_{SEn} = 5\ V$	-10		10	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT} = 9\ A$; $V_{SENSE} = 4\ V$; $V_{SEn} = 5\ V$	2650	2860	3070	
dK_3/K_3 (1) (2)	Current sense ratio drift	$I_{OUT} = 9\ A$; $V_{SENSE} = 4\ V$; $V_{SEn} = 5\ V$	-5		5	%
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: $V_{SEn} = 0\ V$	0		0.5	µA
		MultiSense disabled: $-1\ V < V_{SENSE} < 5\ V$(1)	-0.5		0.5	
		MultiSense enabled: $V_{SEn} = 5\ V$; Channel ON; $I_{OUT} = 0\ A$; Diagnostic selected; $V_{IN} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $I_{OUT} = 0\ A$	0		2	
		MultiSense enabled: $V_{SEn} = 5\ V$; Channel OFF; Diagnostic selected: $V_{IN} = 0\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$	0		2	
V_{OUT_MSD} (1)	Output Voltage for MultiSense shutdown	$V_{IN} = 5\ V$; $V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $R_{SENSE} = 2.7\ k\Omega$; $I_{OUT} = 3\ A$		5		V
V_{SENSE_SAT}	Multisense saturation voltage	$V_{CC} = 7\ V$; $R_{SENSE} = 2.7\ k\Omega$; $V_{SEn} = 5\ V$; $V_{IN} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $I_{OUT} = 9\ A$; $T_j = 150°C$	5			V
I_{SENSE_SAT} (1)	CS saturation current	$V_{CC} = 7\ V$; $V_{SENSE} = 4\ V$; $V_{IN} = 5\ V$; $V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $T_j = 150°C$	4			mA
I_{OUT_SAT} (1)	Output saturation current	$V_{CC} = 7\ V$; $V_{SENSE} = 4\ V$; $V_{IN} = 5\ V$; $V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $T_j = 150°C$	12			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	$V_{IN} = 0\ V$; $V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	$V_{IN} = 0\ V$; $V_{OUT} = V_{OL}$; $V_{SEn} = 5\ V$	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 9. T_{DSTKON})	$V_{IN} = 5\ V$ to $0\ V$; $V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $I_{OUT} = 0\ A$; $V_{OUT} = 4\ V$	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	$V_{IN} = 0\ V$; $V_{FR} = 0\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $V_{OUT} = 4\ V$; $V_{SEn} = 0\ V$ to $5\ V$			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	$V_{IN} = 0\ V$; $V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 0\ V$; $V_{OUT} = 0\ V$ to $4\ V$		5	30	µs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	$V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 5\ V$; $V_{IN} = 0\ V$; $R_{SENSE} = 1\ k\Omega$; $T_j = -40°C$	2.325	2.41	2.495	V
		$V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 5\ V$; $V_{IN} = 0\ V$; $R_{SENSE} = 1\ k\Omega$; $T_j = 25°C$	1.985	2.07	2.155	V
		$V_{SEn} = 5\ V$; $V_{SEL0} = 0\ V$; $V_{SEL1} = 5\ V$; $V_{IN} = 0\ V$; $R_{SENSE} = 1\ k\Omega$; $T_j = 125°C$	1.435	1.52	1.605	V

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
dV_{SENSE_TC}/dT	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function[3]		$V_{SENSE\_VCC} = V_{CC} / 4$				
Fault diagnostic feedback (see Table 10. Truth table)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V; R_{SENSE} = 1 kΩ	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see Figure 7. MultiSense timings (current sense mode)) [4]						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 4.3 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 4.3 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 4.3 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 4.3 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 4.3 Ω		50	250	µs
MultiSense timings (chip temperature sense mode - see Figure 8. Multisense timings (chip temperature and V_{CC} sense mode)) [4]						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see Figure 8. Multisense timings (chip temperature and V_{CC} sense mode)) [4]						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times)[4]						
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 1.5 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 1.5 A; R_{SENSE} = 1 kΩ			20	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 1.5 A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 1.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs

1. *Parameter specified by design; not subject to production test.*
2. *All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.*
3. *V_{CC} sensing and T_C are referred to GND potential.*
4. *Transition delays are measured up to +/- 10% of final conditions.*

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

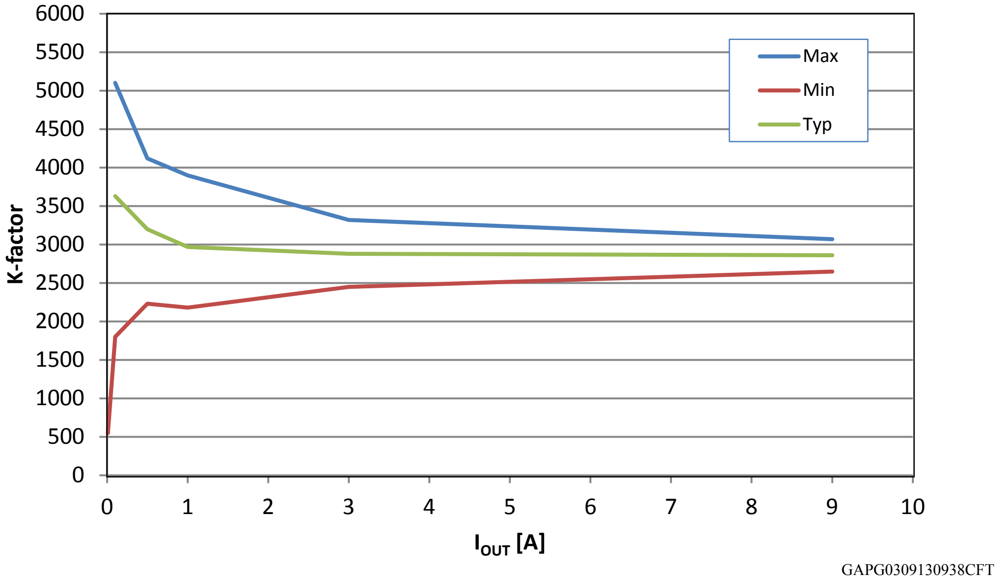


Figure 5. **Current sense accuracy versus I_{OUT}**

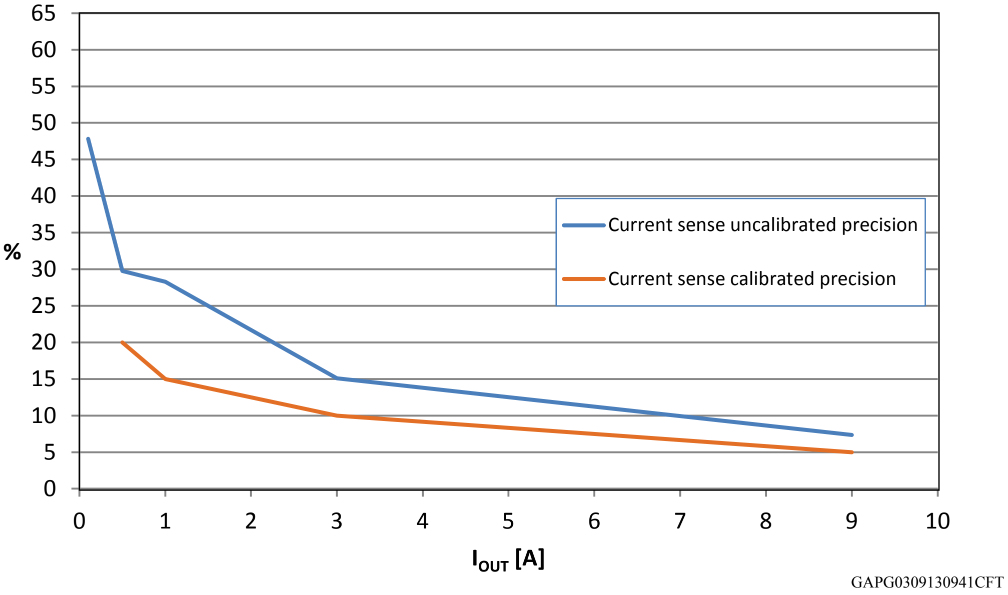
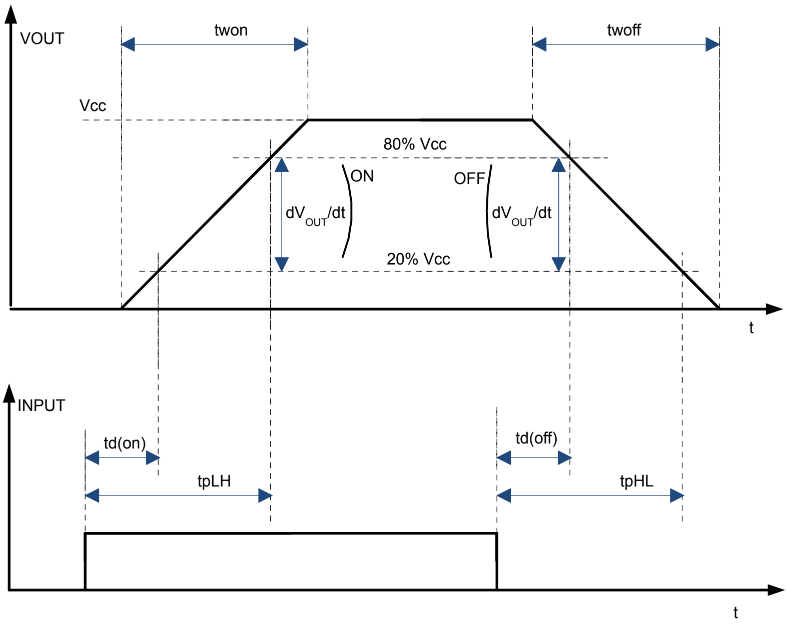


Figure 6. **Switching time and pulse skew**



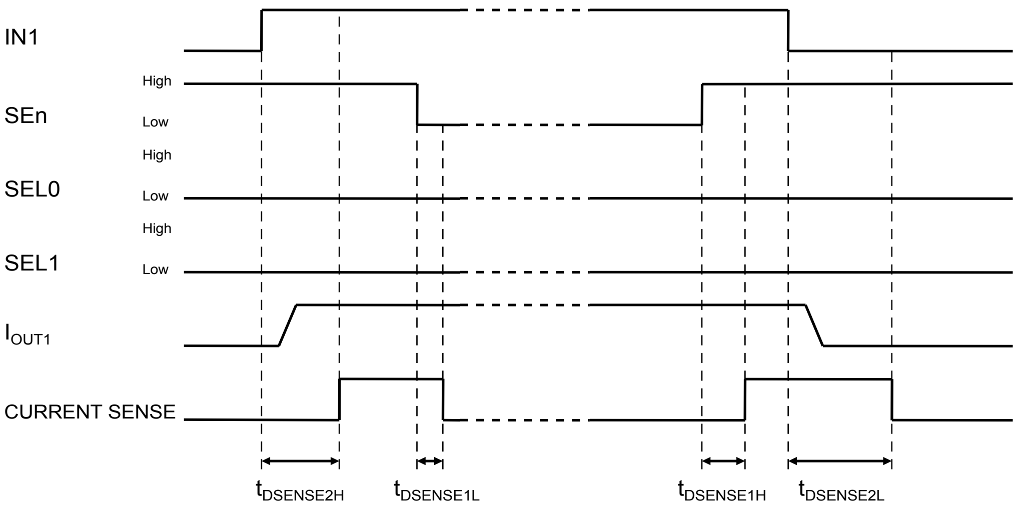


Figure 7. **MultiSense timings (current sense mode)**

Figure 8. **Multisense timings (chip temperature and V_{CC} sense mode)**

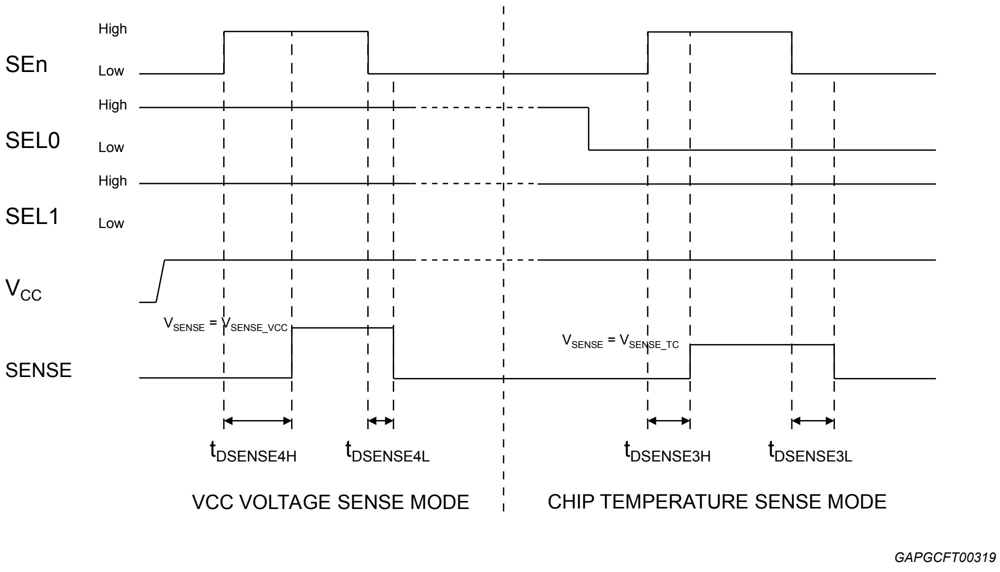


Figure 9. T_{DSTKON}

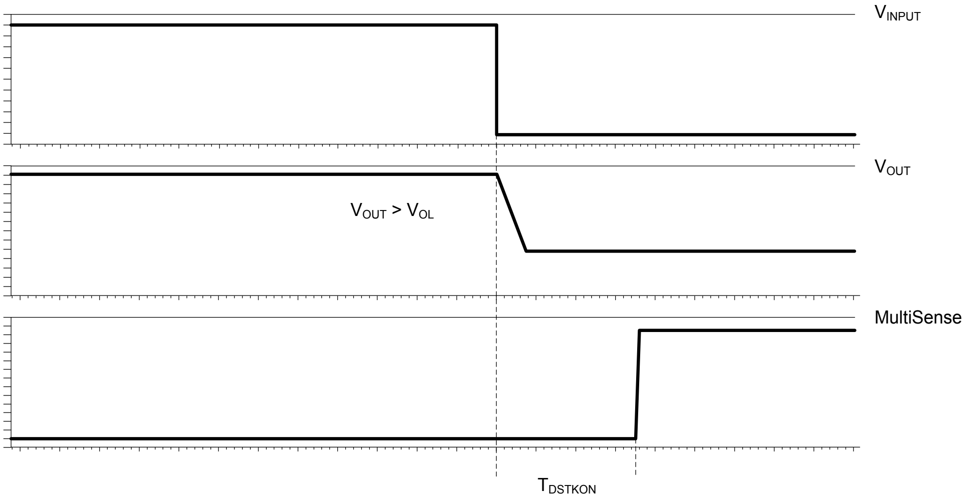


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Table 10. Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150$ °C	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Outputs configured for auto-restart
		H	H			H	See (1)	Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Output cycles with temperature hysteresis
		H	H			L	See (1)	Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} +$ $V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)		H	See (1)	
	Open-load	L	X			H	See (1)	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See (1)		< 0 V	See (1)	

1. *Refer to Table 11. MultiSense multiplexer addressing*

Table 11. MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUX channel	MultiSense output			
				Normal mode	Overload	OFF-state diag.(1)	Negative output
L	X	X		Hi-Z			

SEn	SEL_1	SEL_0	MUX channel	MultiSense output			
				Normal mode	Overload	OFF-state diag.[1]	Negative output
H	L	L	Output diagnostic	I_{SENSE} = 1/K * I_{OUT}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H					
H	H	L	T_{CHIP} Sense	V_{SENSE} = V_{SENSE_TC}			
H	H	H	V_{CC} Sense	V_{SENSE} = V_{SENSE_VCC}			

1. *In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN = 0; OUT = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN = 0; OUT = latched,* $V_{OUT} > V_{OL}$*; MUX channel = channel 0 diagnostic; Mutisense =* V_{SENSEH}

2.4 Waveforms

Figure 10. **Latch functionality - behavior in hard short-circuit condition ($T_{AMB} << T_{TSD}$)**

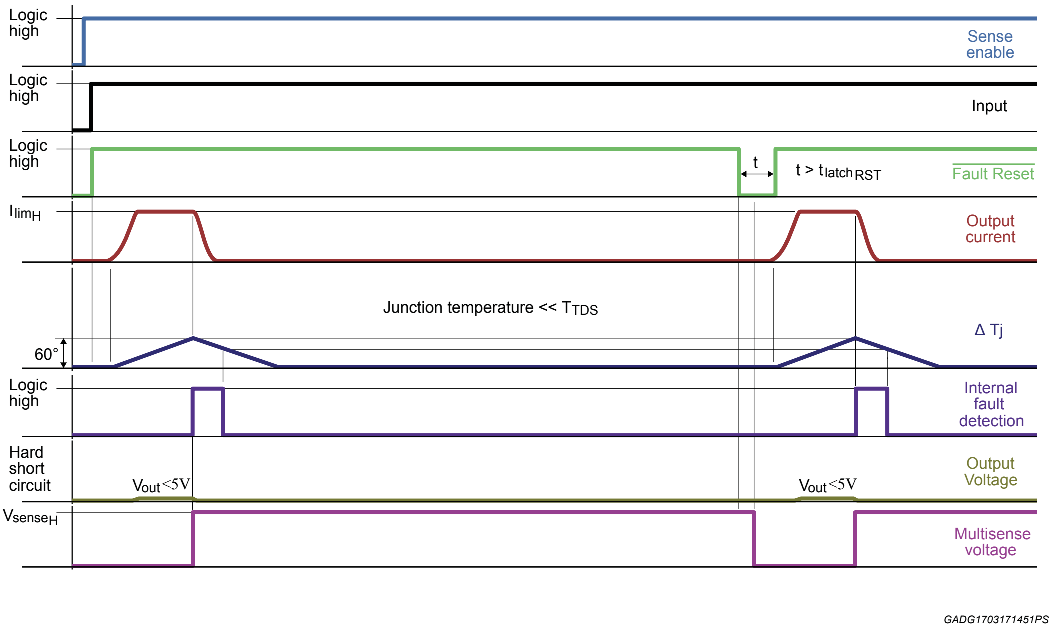

Figure 11. Latch functionality - behavior in hard short-circuit condition

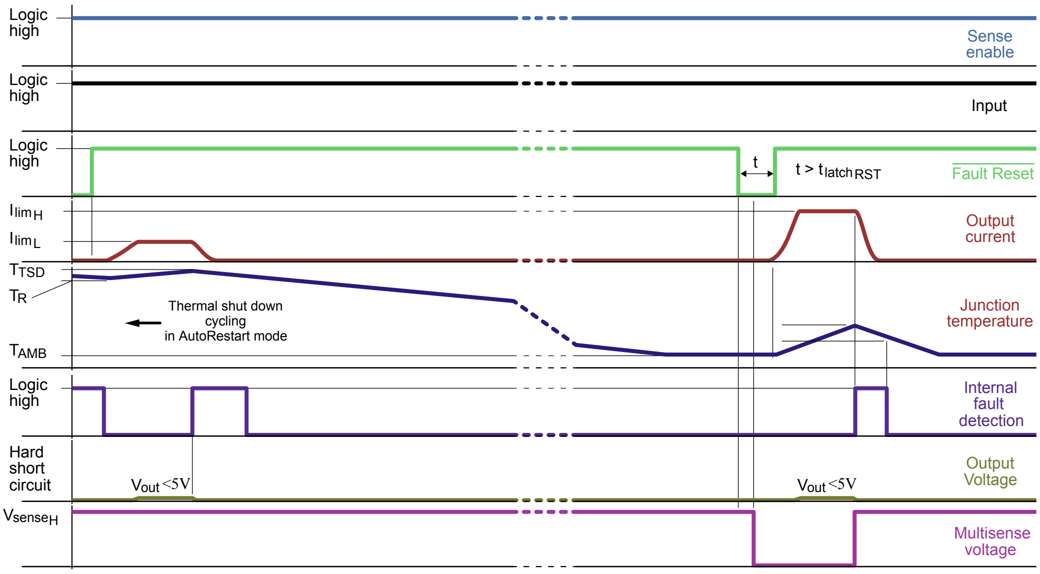

Figure 12. Latch functionality - behavior in hard short-circuit condition (autorestart mode + latch off)

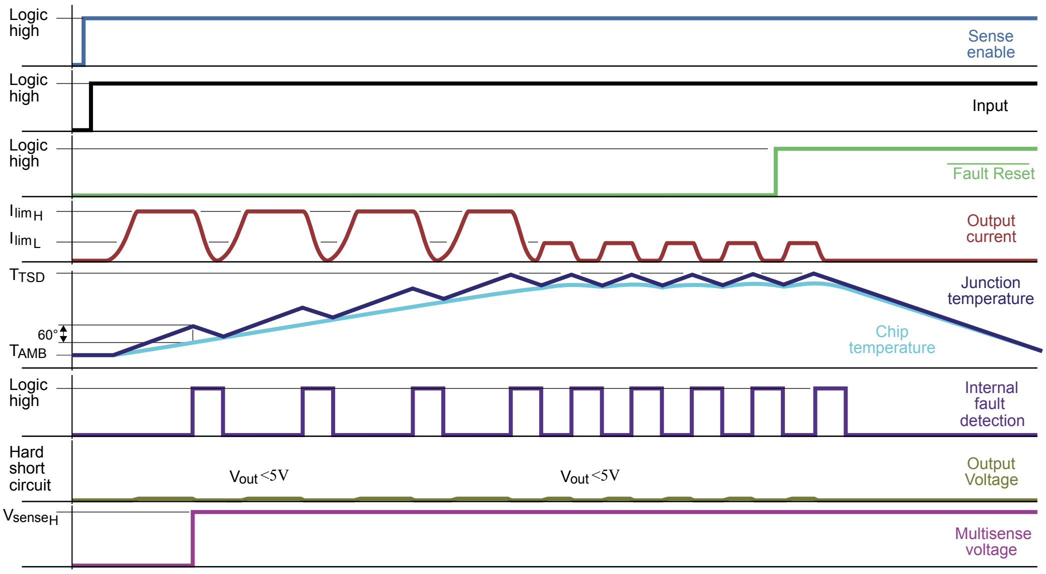

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Figure 13. Standby mode activation

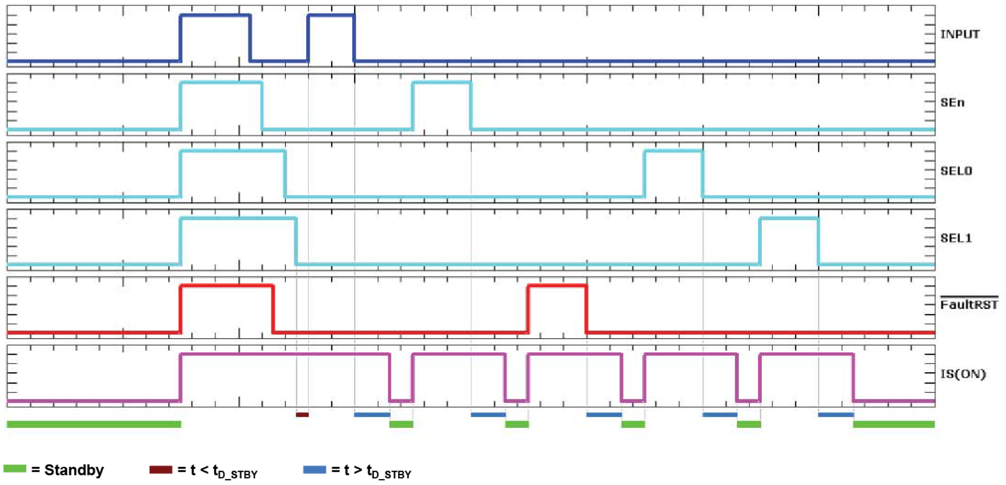

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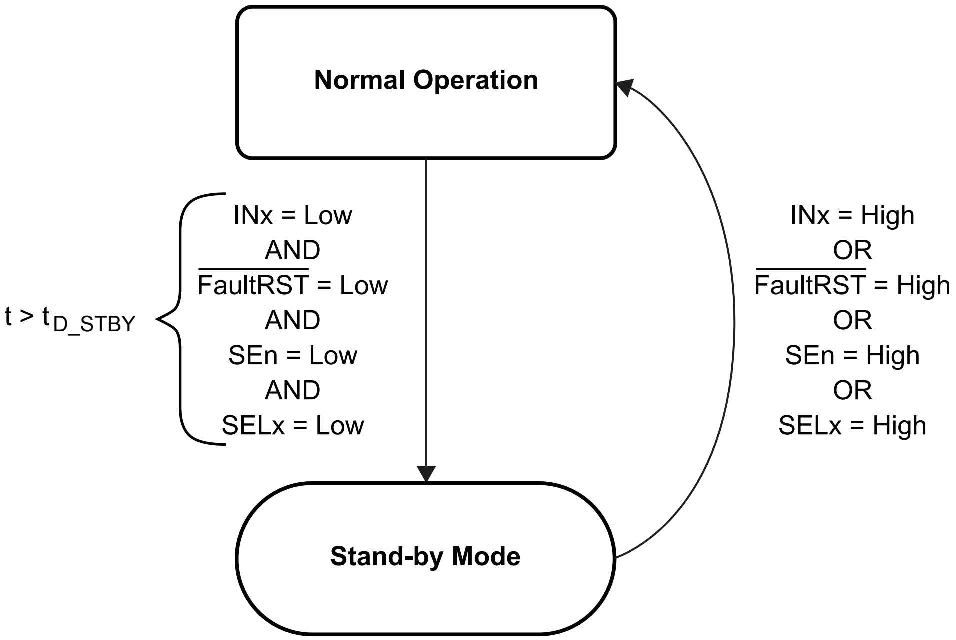
Figure 14. Standby state diagram



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2.5 Electrical characteristics curves

Figure 15. **OFF-state output current**

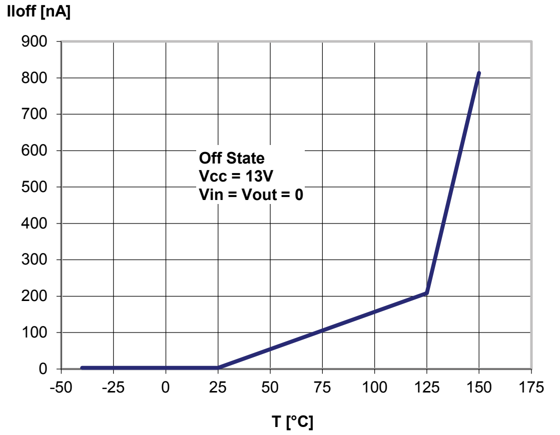

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Figure 16. **Standby current**

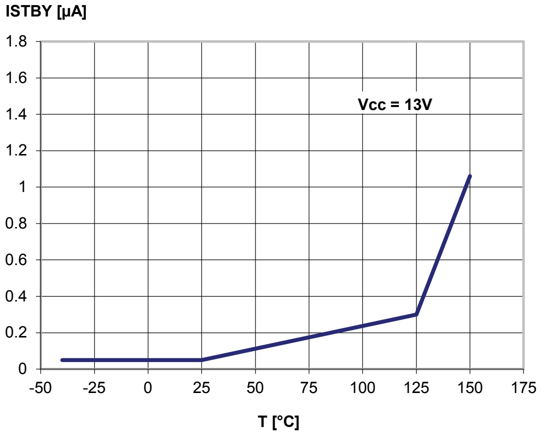

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Figure 17. **$I_{GND(ON)}$ vs. I_{out}**

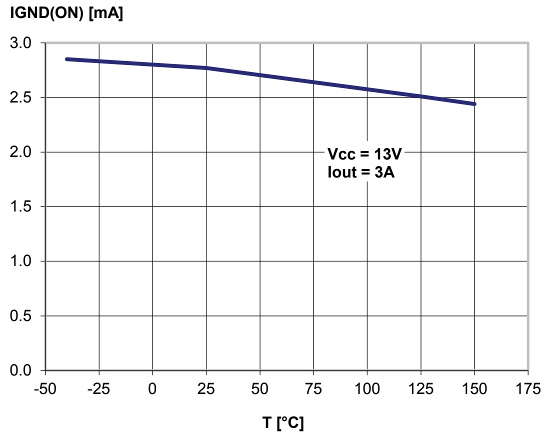

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Figure 18. **Logic Input high level voltage**

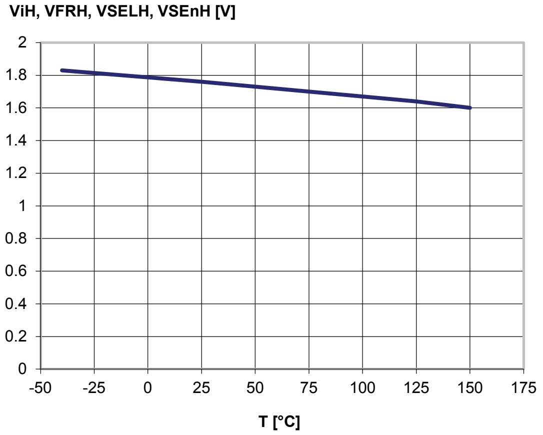

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Figure 19. **Logic Input low level voltage**

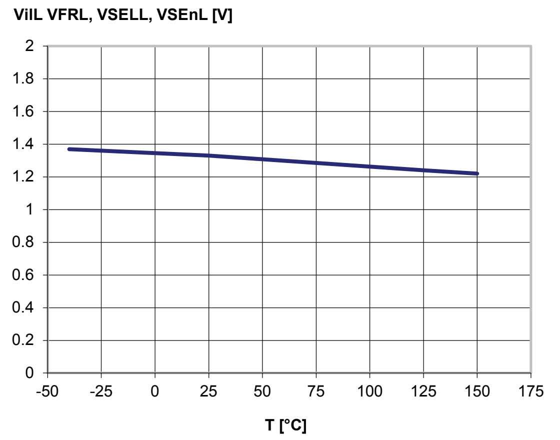

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Figure 20. **High level logic input current**

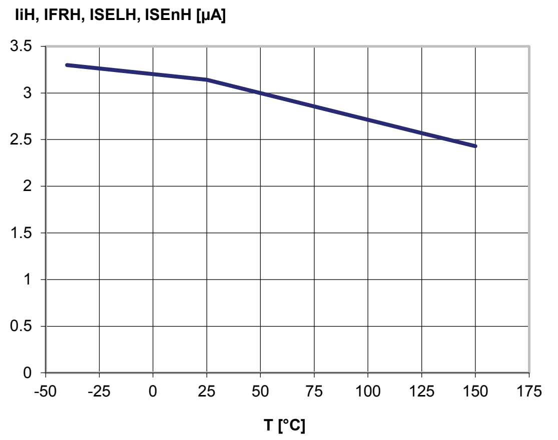

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Figure 21. **Low level logic input current**

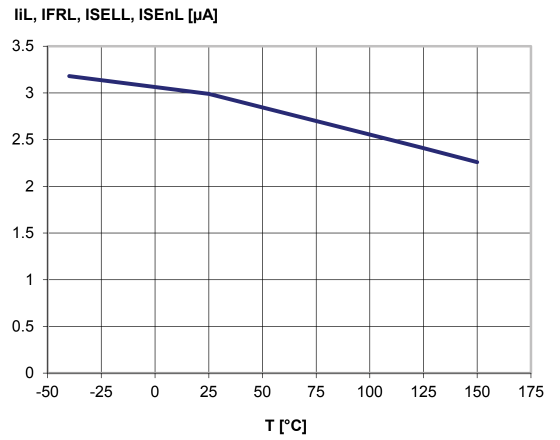

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Figure 22. **Logic Input hysteresis voltage**

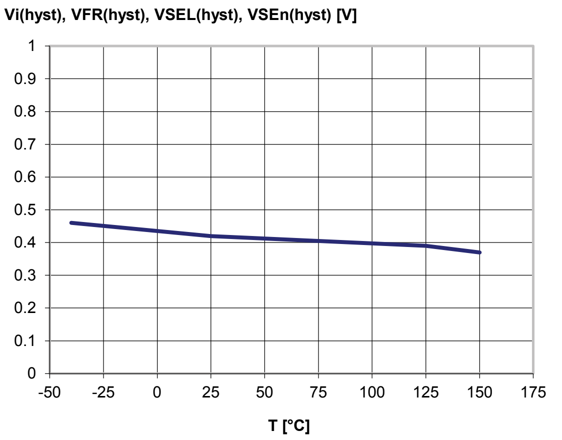

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Figure 23. **FaultRST Input clamp voltage**

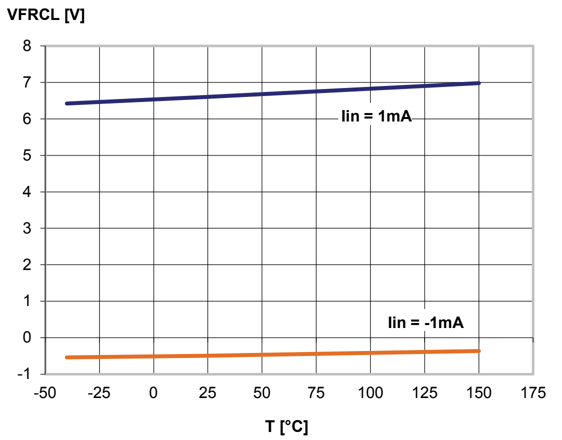

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Figure 24. **Undervoltage shutdown**

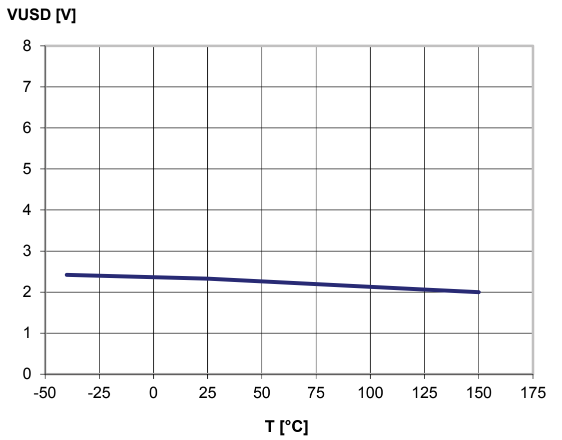

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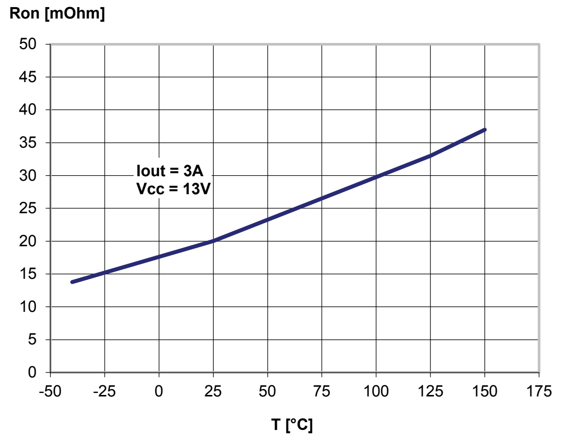
Figure 25. On-state resistance vs. T_{case}



GAPG0309131003CFT

Figure 26. On-state resistance vs. V_{CC}

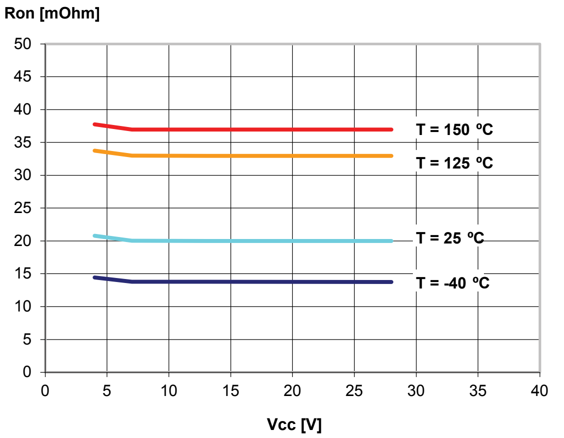


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Figure 27. Turn-on voltage slope

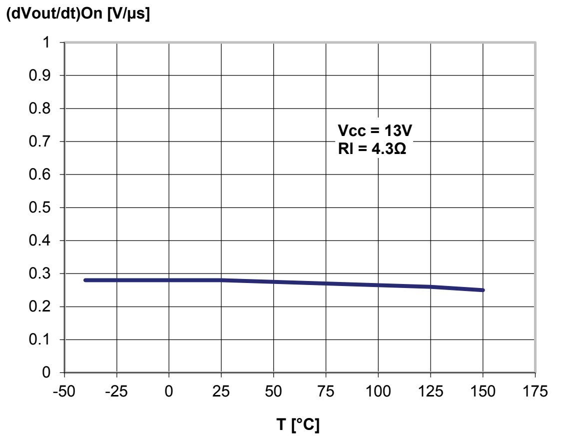

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Figure 28. Turn-off voltage slope

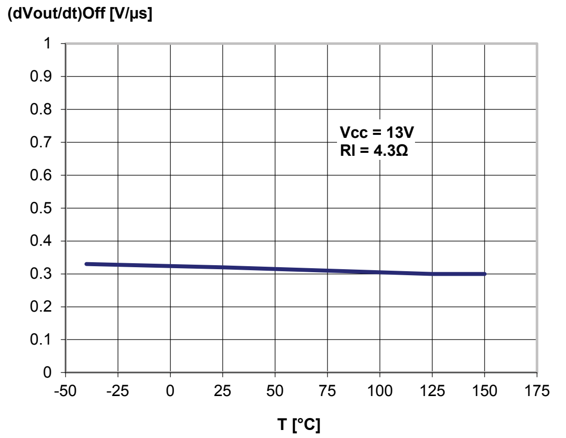

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Figure 29. Won vs. T_{case}

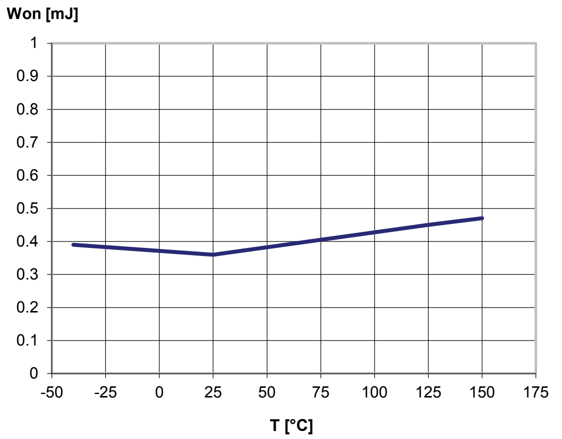

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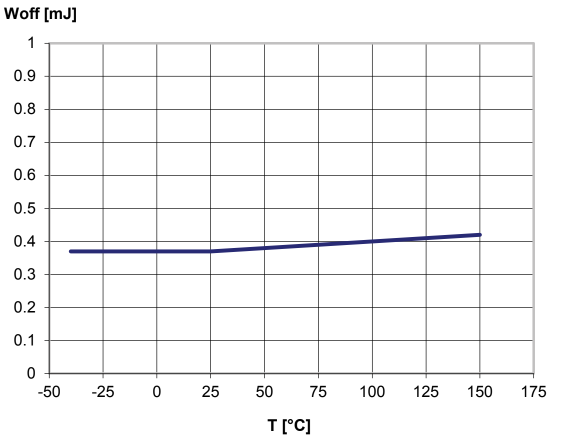
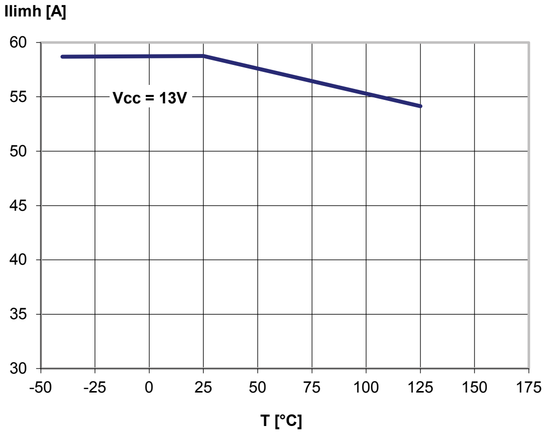
Figure 30. Woff vs. T_{case}



GAPG0309131013CFT

Figure 31. I_{LIMH} vs. T_{case}



GAPG0309131014CFT

Figure 32. OFF-state open-load voltage detection threshold

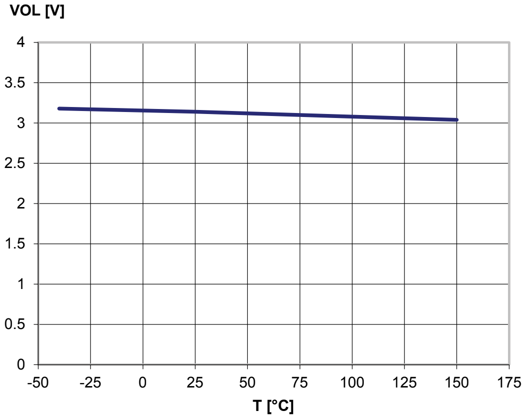


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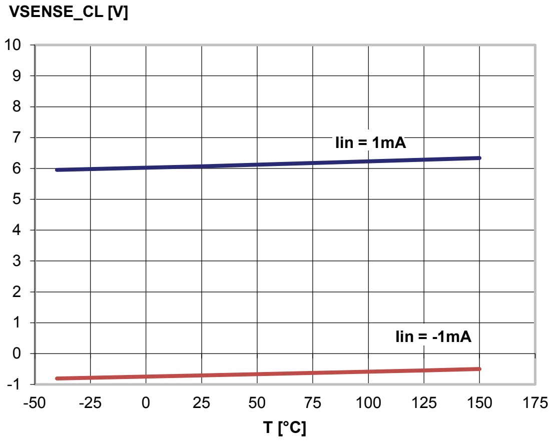
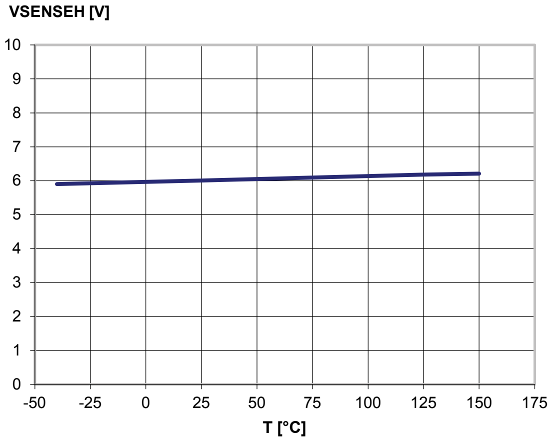
Figure 33. V_{sense} clamp vs. T_{case}



GAPG0309131017CFT

Figure 34. V_{senseh} vs. T_{case}



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3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

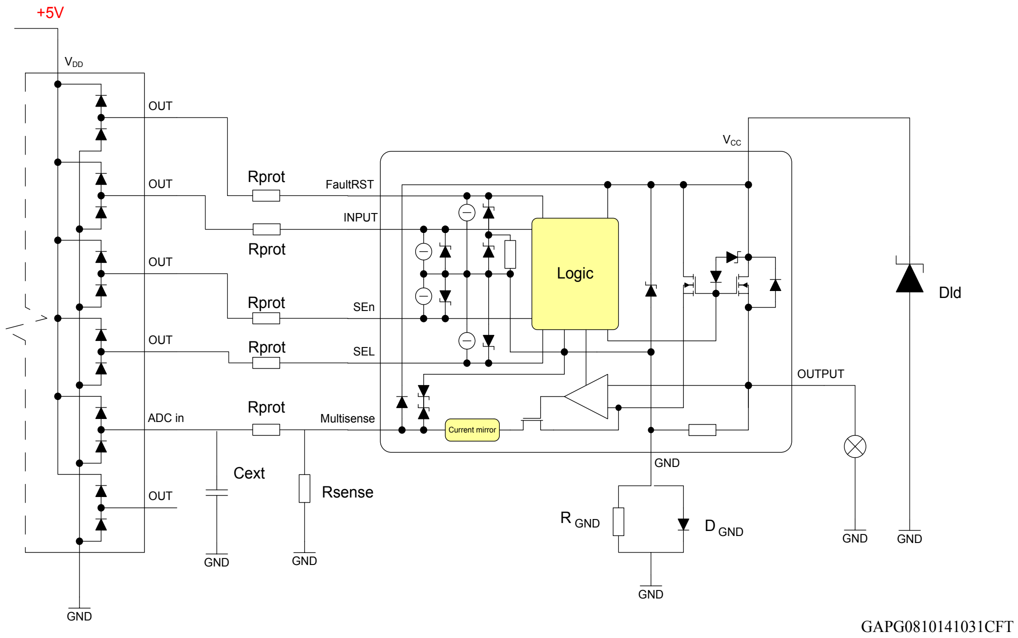
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

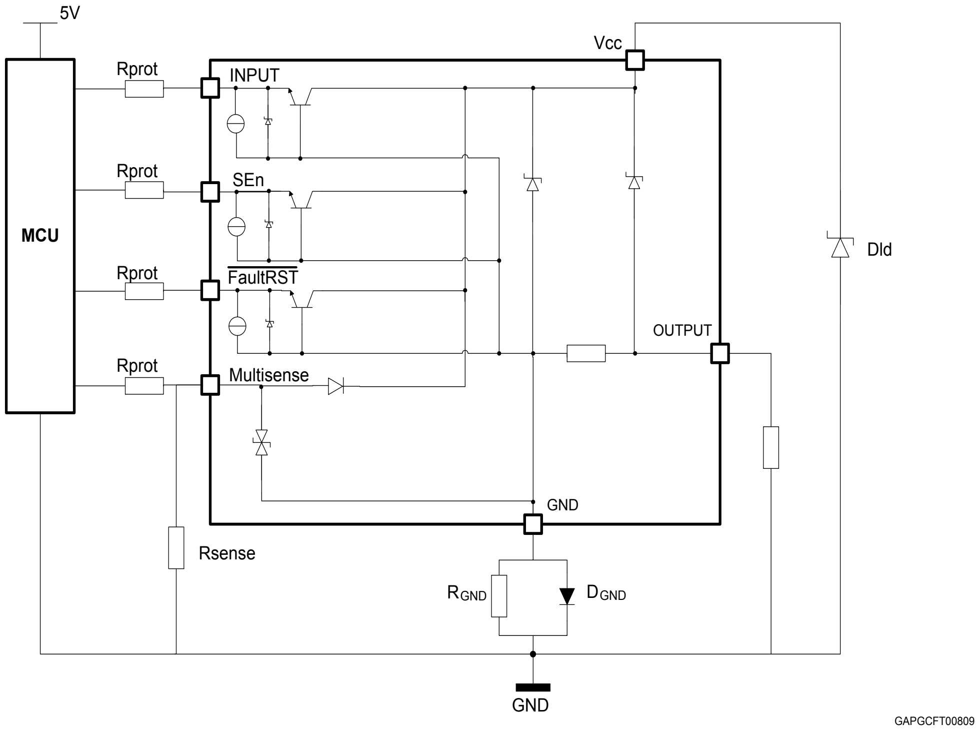
4 Application information

Figure 35. Application diagram



4.1 GND protection network against reverse battery

Figure 36. Simplified internal structure



4.1.1 Diode (DGND) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in Table 12. ISO 7637-2 - electrical transient conduction along supply line.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 12. **ISO 7637-2 - electrical transient conduction along supply line**

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S [1]		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 [2]	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B [3]		40 V	5 pulse	1 min		400 ms, 2 Ω

1. *U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *Test pulse from ISO 7637-2:2004(E).*
3. *With 40 V external suppressor referred to ground (-40°C < T_j < 150 °C).*

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$V_{CCpeak}/I_{latchup} \le R_{prot} \le (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \ge 20$ mA; $V_{OH\mu C} \ge 4.5$ V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

Recommended values: R_{prot} = 15 kΩ

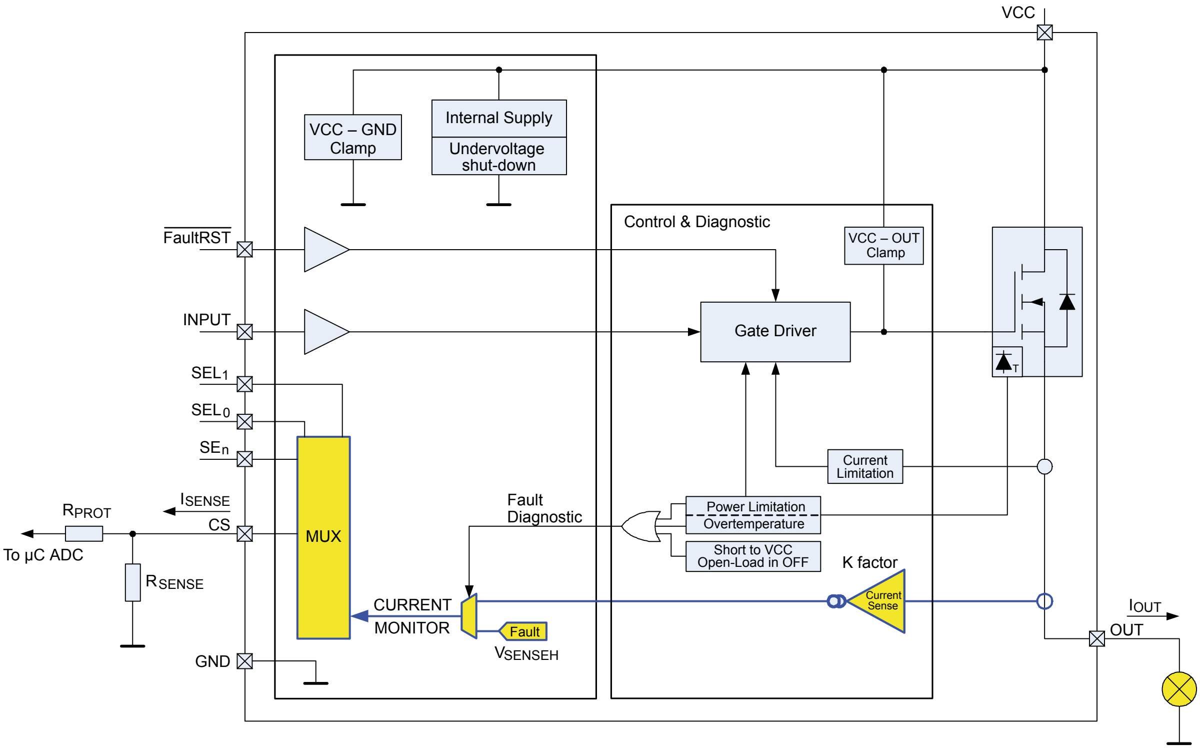
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE}: voltage propotional to chip temperature

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

Figure 37. MultiSense and diagnostic – block diagram



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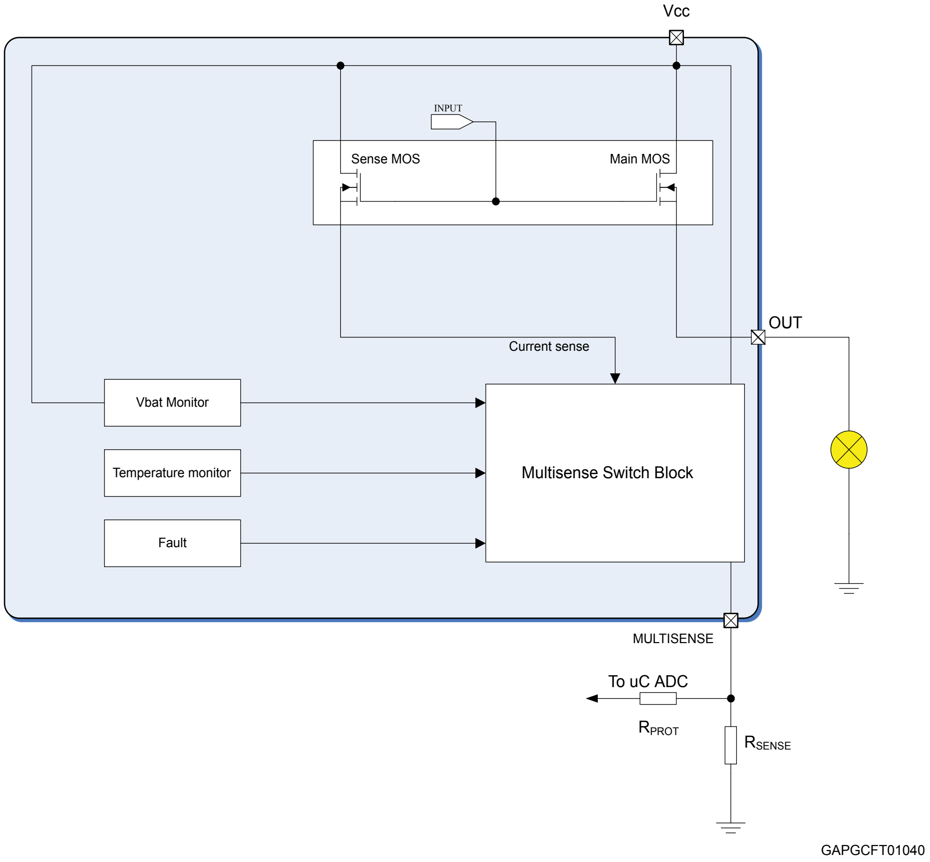
4.4.1 Principle of Multisense signal generation

Figure 38. **MultiSense block diagram**



Current monitor

When current mode is selected in the MultiSense, this output is capable to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from MultiSense pin in current output mode
- I_{OUT} is current flowing through output

- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the MultiSense pin which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the MultiSense in this condition is limited to I_{SENSEH}.

The typical behavior in case of overload or hard short circuit is shown in *Waveforms section*.

Figure 39. Analogue HSD – open-load detection in off-state

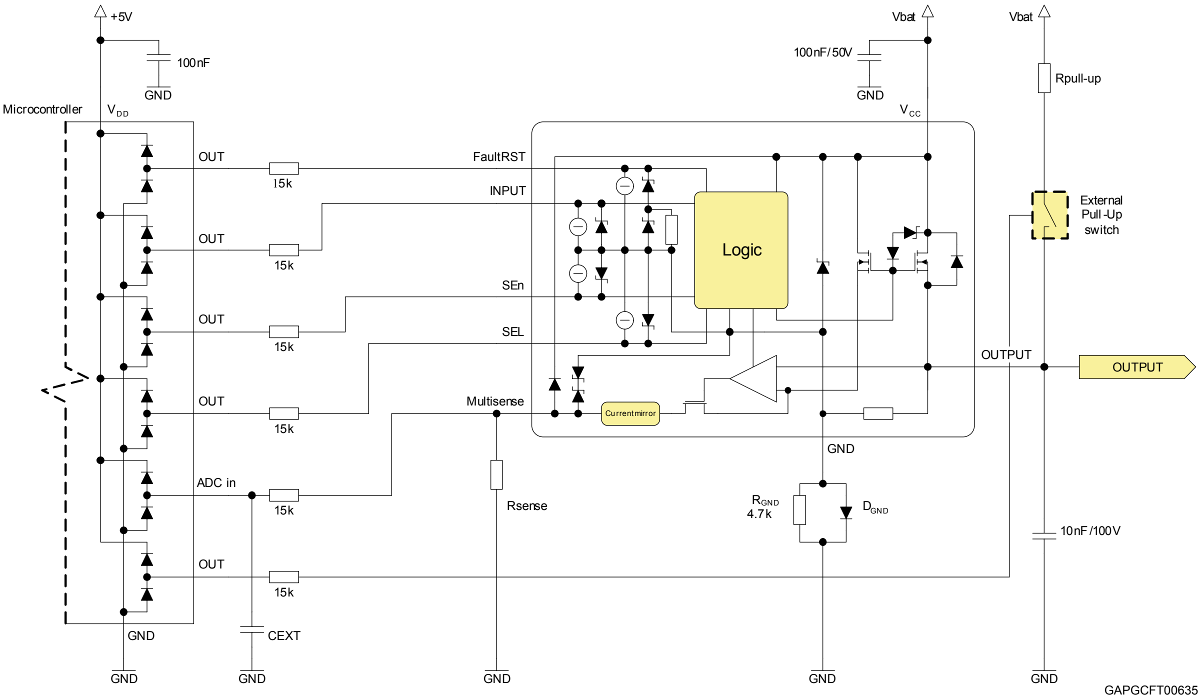


Figure 40. **Open-load / short to V_{CC} condition**

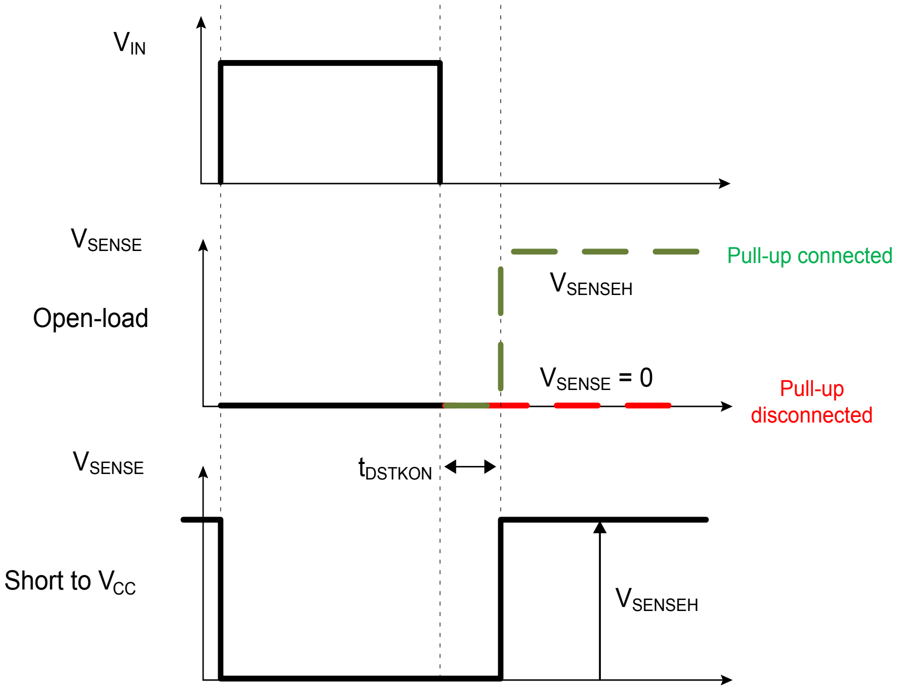


Table 13. **MultiSense pin levels in off-state**

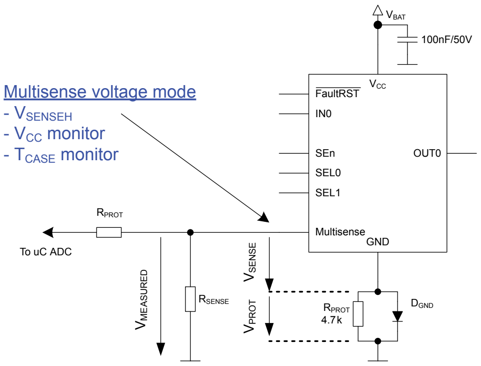
Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 TCASE and VCC monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because a voltage shift is generated between the device GND and the microcontroller input GND reference.

Figure 41. GND voltage shift shows the link between $V_{MEASURED}$ and the real V_{SENSE} signal.

Figure 41. **GND voltage shift**



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V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$.

Case temperature monitor

Case temperature monitor is capable of providing information about the actual device temperature. Since a diode is used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40 °C to 150 °C)).

4.4.3 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

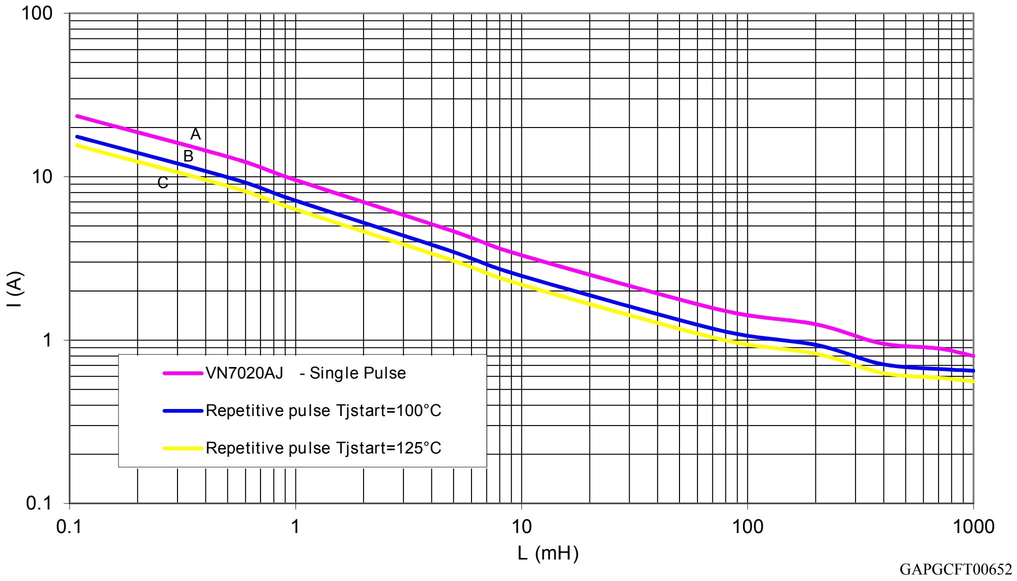
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

5 Maximum demagnetization energy (VCC = 16 V)

Figure 43. **Maximum turn off current versus inductance**



Note: *Values are generated with $R_L = 0\ \Omega$.*

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 44. **PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)**

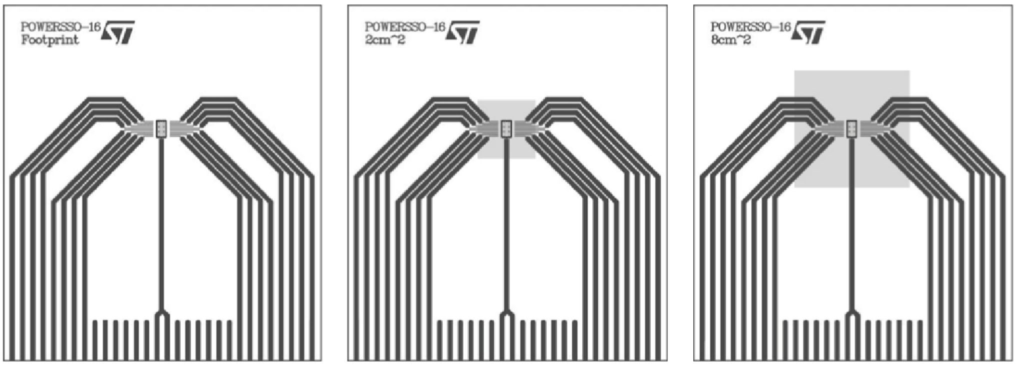


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Figure 45. **PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)**

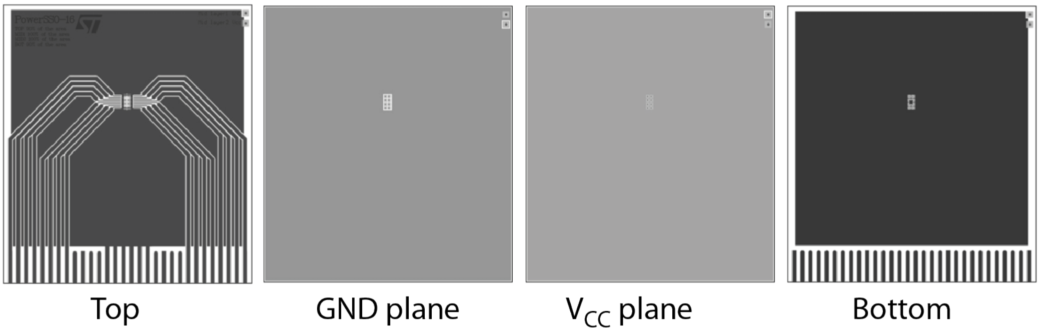

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Table 14. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 46. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

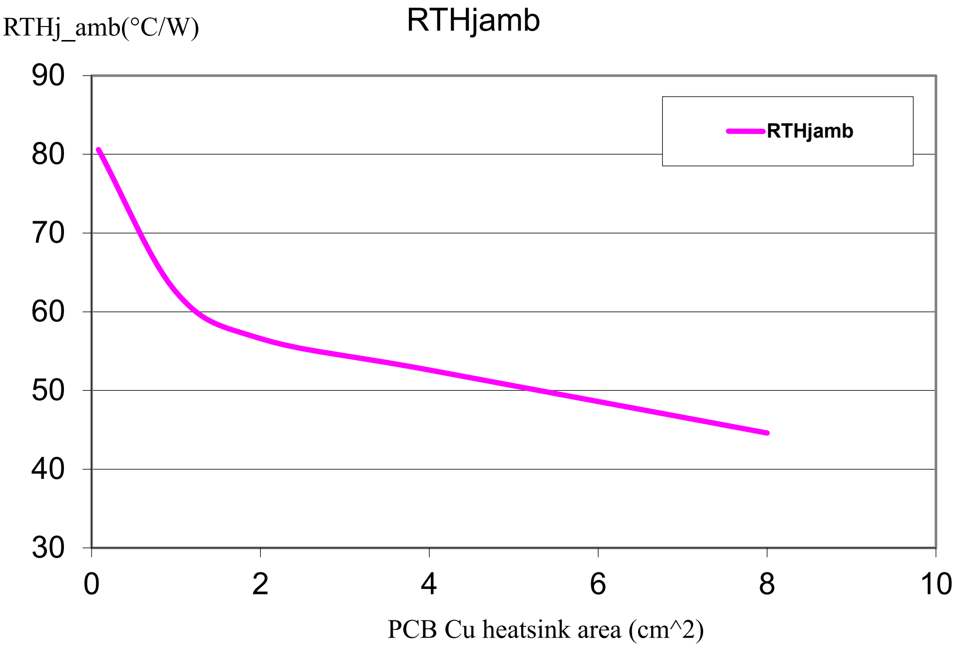

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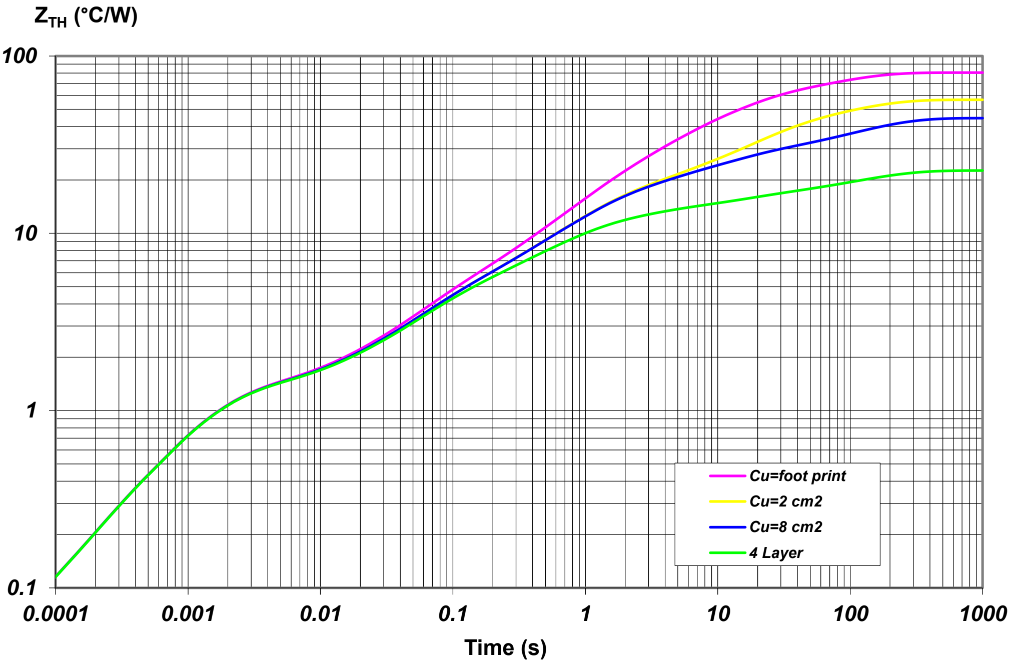
Figure 47. PowerSSO-16 thermal impedance junction ambient single pulse



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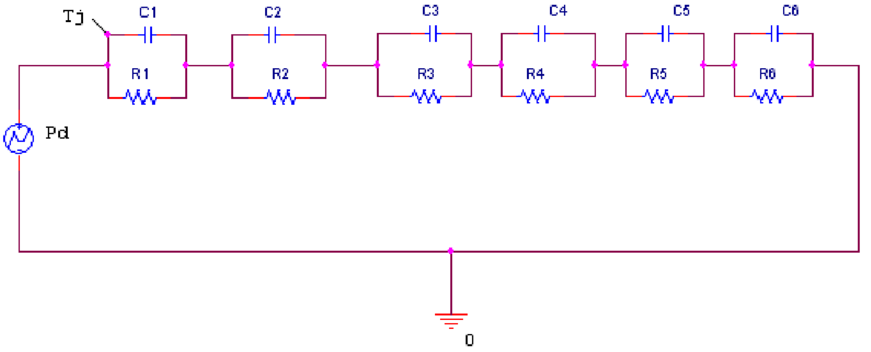
Equation: pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

Figure 48. Thermal fitting model for PowerSSO-16



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Note: *The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.*

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	1.2			
R2 (°C/W)	2.4			
R3 (°C/W)	7	7	7	5
R4 (°C/W)	14	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 (W.s/°C)	0.001			
C2 (W.s/°C)	0.025			
C3 (W.s/°C)	0.1			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 PowerSSO-16 package information

Figure 49. PowerSSO-16 package outline

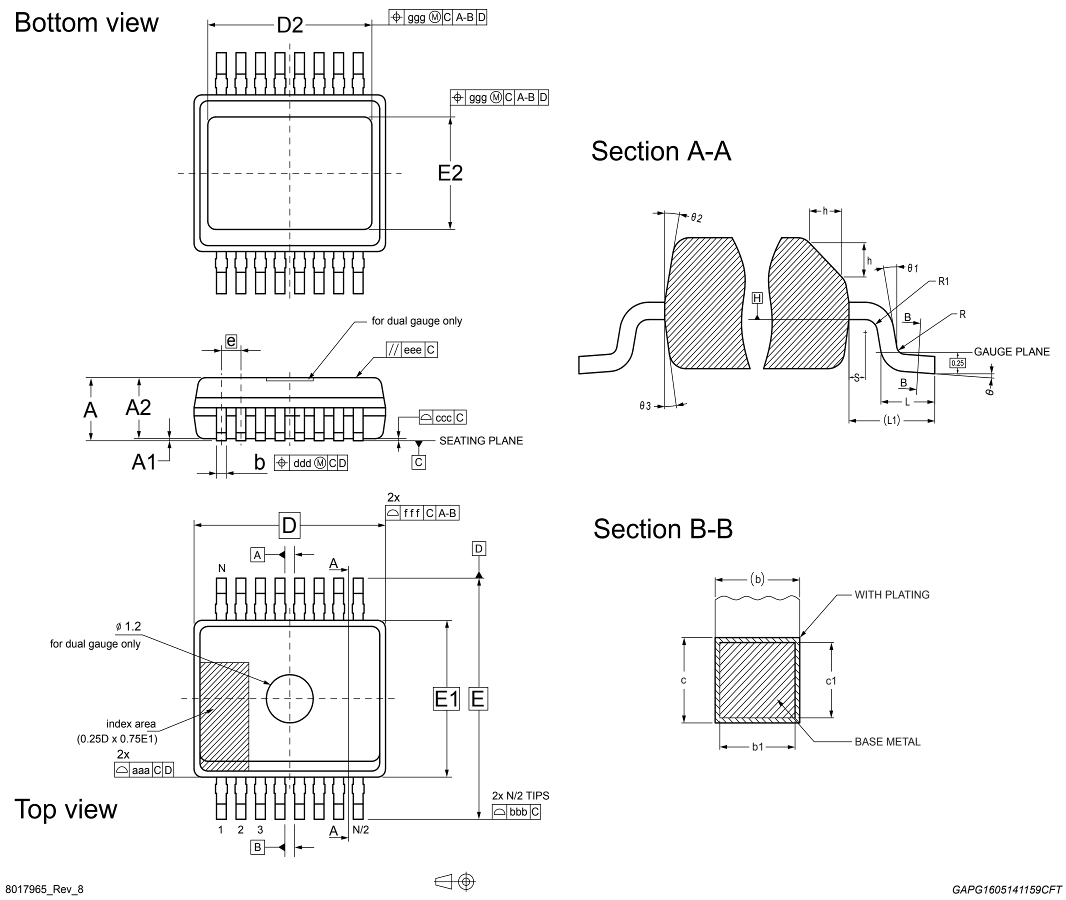


Table 16. PowerSSO-16 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.9 BSC		
D1	2.90		3.50
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.20		2.80
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

7.2 PowerSSO-16 packing information

Figure 50. **PowerSSO-16 reel 13"**

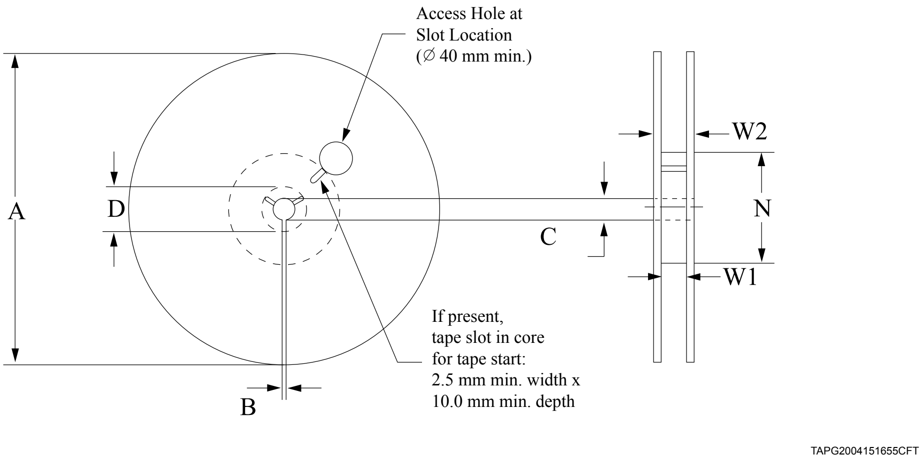


Table 17. **Reel dimensions**

Description	Value[(1)]
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. *All dimensions are in mm.*

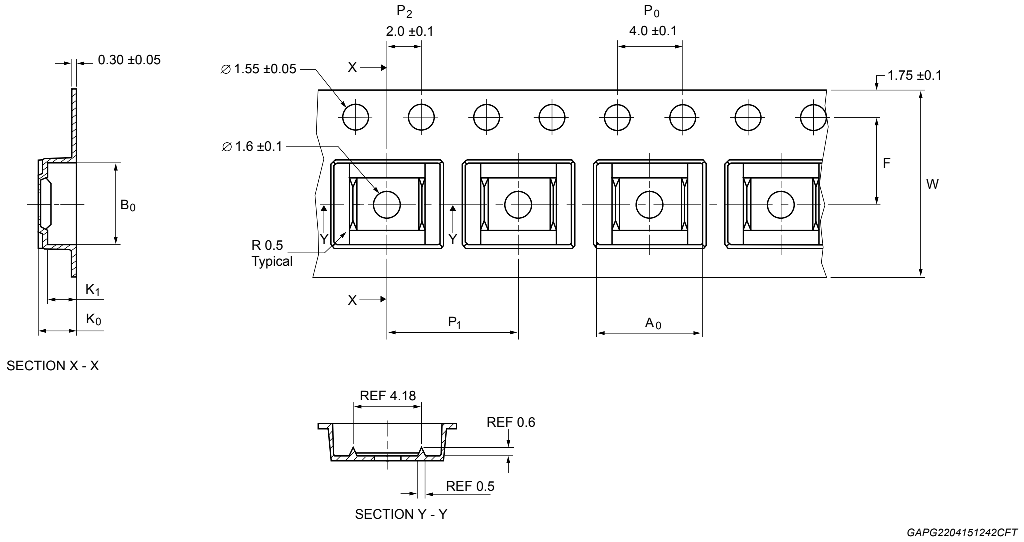


Figure 51. PowerSSO-16 carrier tape

Table 18. PowerSSO-16 carrier tape dimensions

Description	Value[1]
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3

1. *All dimensions are in mm.*

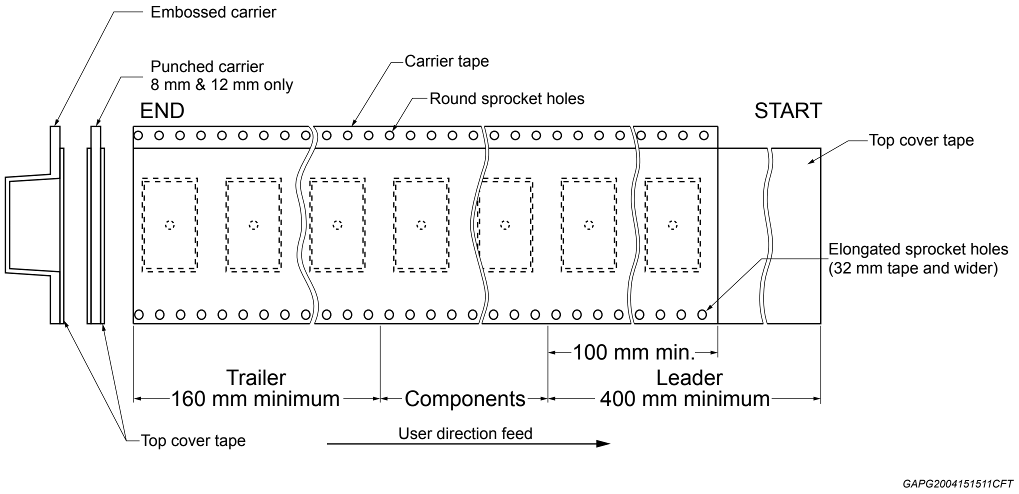
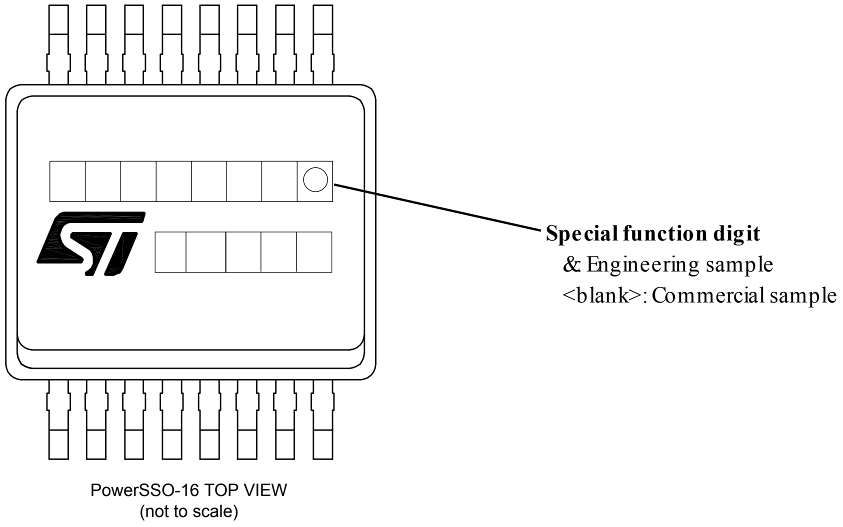


Figure 52. PowerSSO-16 schematic drawing of leader and trailer tape

7.3 PowerSSO-16 marking information

Figure 53. PowerSSO-16 marking information



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Parts marked as ‘&’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8 Order codes

Table 19. **Device summary**

Package	Order codes
	Tape and reel
PowerSSO-16	VN7020AJTR

Revision history

Table 20. **Document revision history**

Date	Revision	Changes
25-May-2015	1	Initial release.
02-Oct-2016	2	Updated the following: • Features list on the cover page • *Figure 52: "PowerSSO-16 marking information"*
02-Dec-2016	3	Updated the Current sense ratio drift I_{OUT} value in *Table 9: "MultiSense".* Modified note in *Section 7.3: "PowerSSO-16 marking information".*
29-Jun-2018	4	Minor text change in Section 4.4.2 T_{CASE} and V_{CC} monitor.

List of tables

List of figures