## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

| | |
|---|---|
| Drain-to-Source Voltage | $BV_{DSS}$ |
| Drain-to-Gate Voltage | $BV_{DGS}$ |
| Gate-to-Source Voltage | ±20V |
| Operating Ambient Temperature, $T_A$ | –55°C to +150°C |
| Storage Temperature, $T_S$ | –55°C to +150°C |

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** $T_A$ = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | –400 | — | — | V | $V_{GS}$ = 0V, $I_D$ = –2 mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | –0.8 | — | –2 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = –1 mA |
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | — | 5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = –1 mA (Note 1) |
| Gate Body Leakage Current | $I_{GSS}$ | — | — | –100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| Zero-Gate Voltage Drain Current | $I_{DSS}$ | — | — | –1 | µA | $V_{GS}$ = 0V, $V_{DS}$ = –100V |
| | | | | –10 | mA | $V_{GS}$ = 0V,<br>$V_{DS}$ = Maximum rating |
| | | | | –1 | mA | $V_{DS}$ = 0.8 Maximum rating,<br>$V_{GS}$ = 0V, $T_A$ = 125°C<br>(Note 1) |
| On-State Drain Current | $I_{D(ON)}$ | –0.7 | — | — | A | $V_{GS}$ = –10V, $V_{DS}$ = –25V |
| Static Drain-to-Source On-State Resistance | $R_{DS(ON)}$ | — | 12 | 15 | Ω | $V_{GS}$ = –2.5V, $I_D$ = –20 mA |
| | | | 11 | 15 | Ω | $V_{GS}$ = –4.5V, $I_D$ = –150 mA |
| | | | 11 | 15 | Ω | $V_{GS}$ = –10V, $I_D$ = –300 mA |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta R_{DS(ON)}$ | — | — | 0.75 | %/°C | $V_{GS}$ = –10V, $I_D$ = –300 mA (Note 1) |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** $T_A$ = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Forward Transconductance | $G_{FS}$ | 200 | — | — | mmho | $V_{DS}$ = –25V, $I_D$ = –300 mA |
| Input Capacitance | $C_{ISS}$ | — | — | 300 | pF | $V_{GS}$ = 0V,<br>$V_{DS}$ = –25V,<br>f = 1 MHz |
| Common-Source Output Capacitance | $C_{OSS}$ | — | — | 50 | pF | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | — | 12 | pF | |
| Turn-On Delay Time | $t_{d(ON)}$ | — | — | 10 | ns | $V_{DD}$ = –25V,<br>$I_D$ = –300 mA,<br>$R_{GEN}$ = 25Ω |
| Rise Time | $t_r$ | — | — | 15 | ns | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | — | — | 60 | ns | |
| Fall Time | $t_f$ | — | — | 40 | ns | |
| **DIODE PARAMETER** | | | | | | |
| Diode Forward Voltage Drop | $V_{SD}$ | — | — | 1.8 | V | $V_{GS}$ = 0V, $I_{DS}$ = –200 mA (Note 1) |
| Reverse Recovery Time | $t_{rr}$ | — | 300 | — | ns | $V_{GS}$ = 0V, $I_{DS}$ = –200 mA |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle

## TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | |
| Operating Ambient Temperature | $T_A$ | –55 | — | +150 | °C | |
| Storage Temperature | $T_S$ | –55 | — | +150 | °C | |
| **PACKAGE THERMAL RESISTANCE** | | | | | | |
| 3-lead TO-92 | $\theta_{JA}$ | — | 132 | — | °C/W | |
| 8-lead SOIC | $\theta_{JA}$ | — | 101 | — | °C/W | |

## THERMAL CHARACTERISTICS

| Package | $I_D$ (Note 1) (Continuous) (mA) | $I_D$ (Pulsed) (mA) | Power Dissipation at $T_A$ = 25°C (W) | $I_{DR}$ (Note 1) (mA) | $I_{DRM}$ (mA) |
|---|---|---|---|---|---|
| 3-lead TO-92 | –180 | –800 | 1 | –180 | –800 |
| 8-lead SOIC | –86 | –600 | 0.74 (Note 2) | –86 | –600 |

**Note 1:** $I_D$ (continuous) is limited by maximum $T_J$.

**2:** Mounted on an FR board, 25 mm x 25 mm x 1.57 mm

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

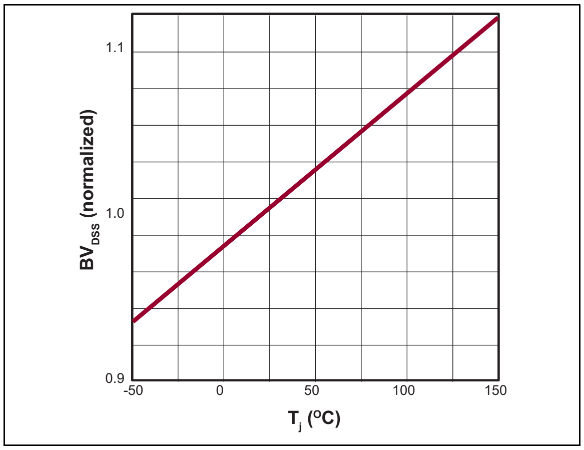


**FIGURE 2-1:** *$BV_{DSS}$ Variation with Temperature.*

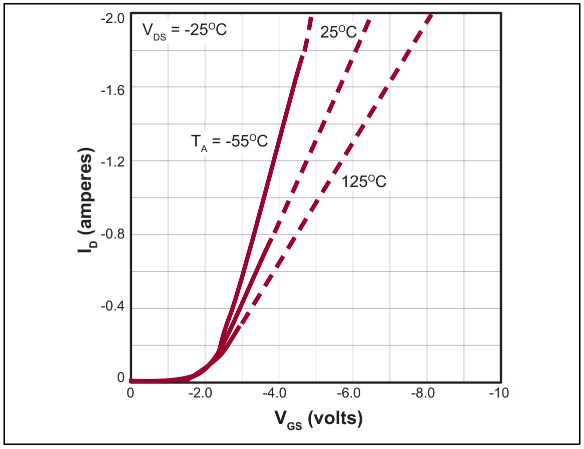


**FIGURE 2-2:** *Transfer Characteristics.*

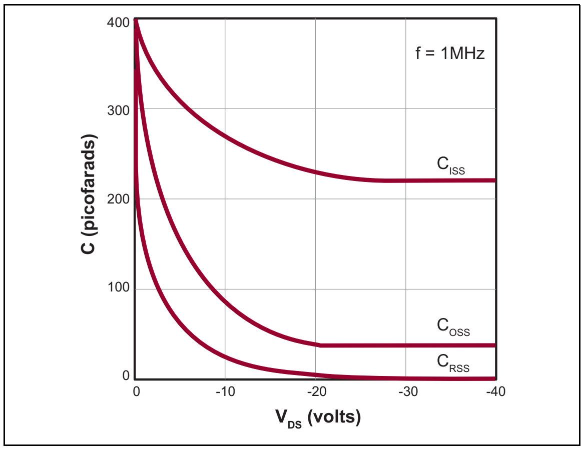


**FIGURE 2-3:** *Capacitance vs. Drain-to-Source Voltage.*

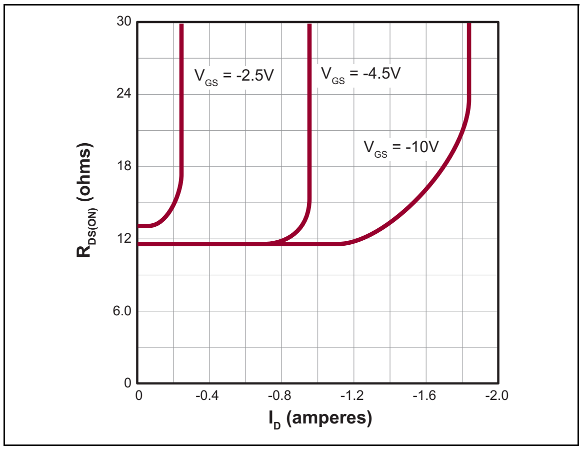


**FIGURE 2-4:** *On-Resistance vs. Drain Current.*

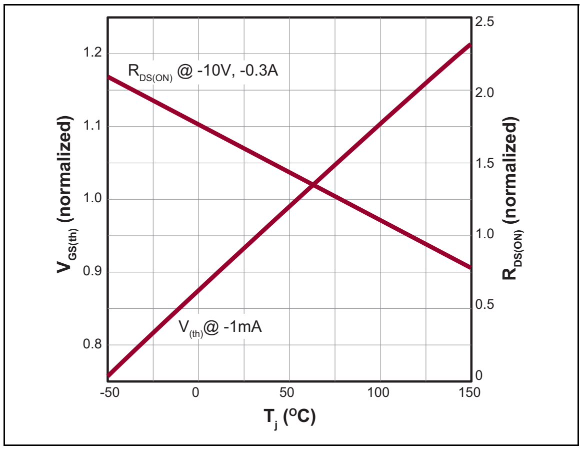


**FIGURE 2-5:** *$V_{GS(th)}$ and $R_{DS}$ Variation with Temperature.*

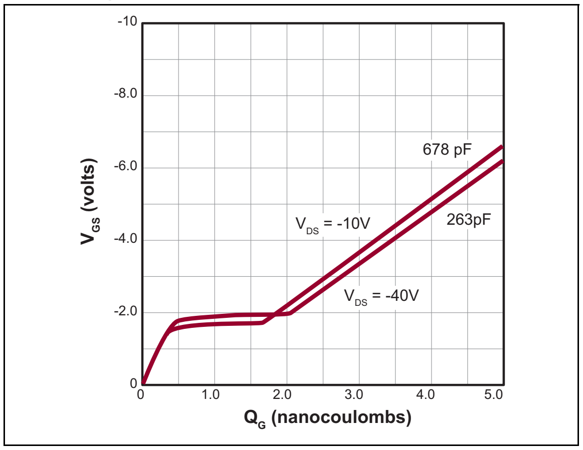


**FIGURE 2-6:** *Gate Drive Dynamic Characteristics.*

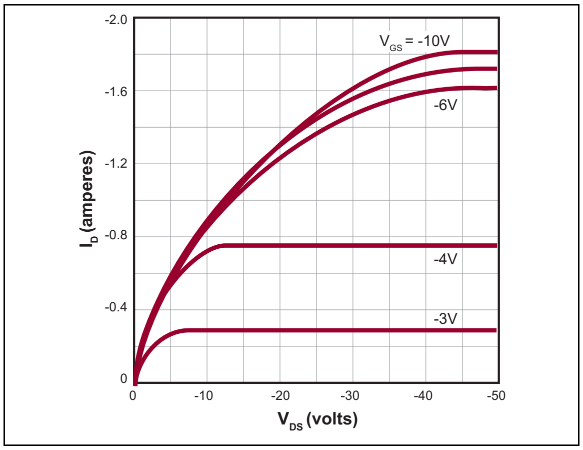


**FIGURE 2-7:** *Output Characteristics.*

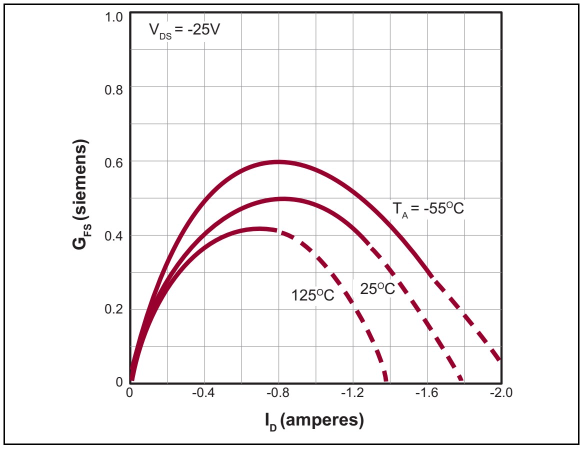


**FIGURE 2-8:** *Transconductance vs. Drain Current.*

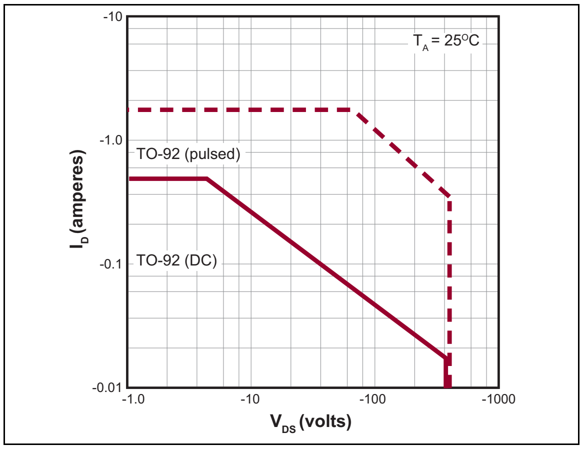


**FIGURE 2-9:** *Maximum Rated Safe Operating Area.*

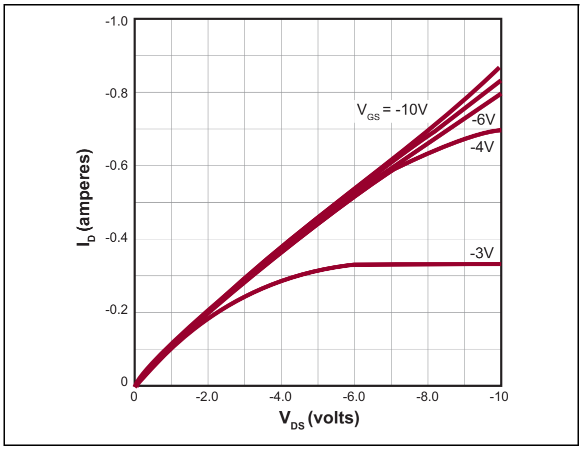


**FIGURE 2-10:** *Saturation Characteristics.*

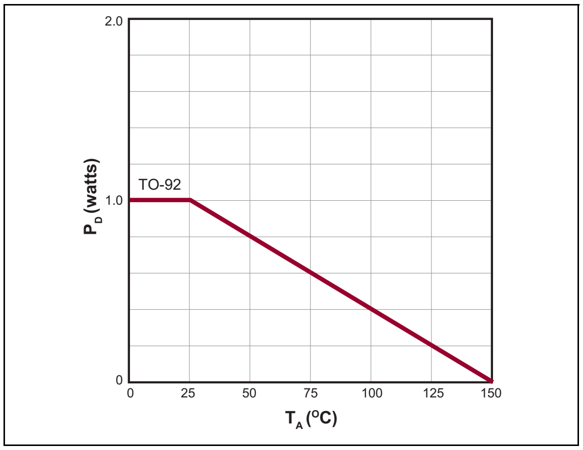


**FIGURE 2-11:** *Power Dissipation vs. Temperature.*

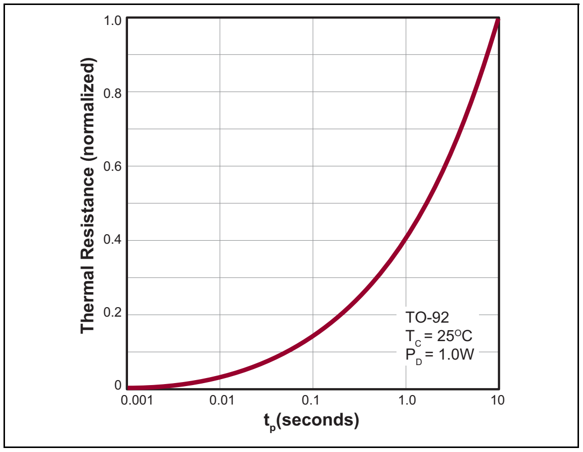


**FIGURE 2-12:** *Thermal Response Characteristics.*

## 3.0 PIN DESCRIPTION

The details on the pins of TP2640 TO-92 and SOT-89 packages are listed in Table 3-1 and Table 3-2, respectively. Refer to **Package Type** for the location of pins.

**TABLE 3-1: 3-LEAD TO-92 PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | Source | Source |
| 2 | Gate | Gate |
| 3 | Drain | Drain |

**TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | N/C | No Connection |
| 2 | N/C | No Connection |
| 3 | Source | Source |
| 4 | Gate | Gate |
| 5 | Drain | Drain |
| 6 | Drain | Drain |
| 7 | Drain | Drain |
| 8 | Drain | Drain |

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TP2640.

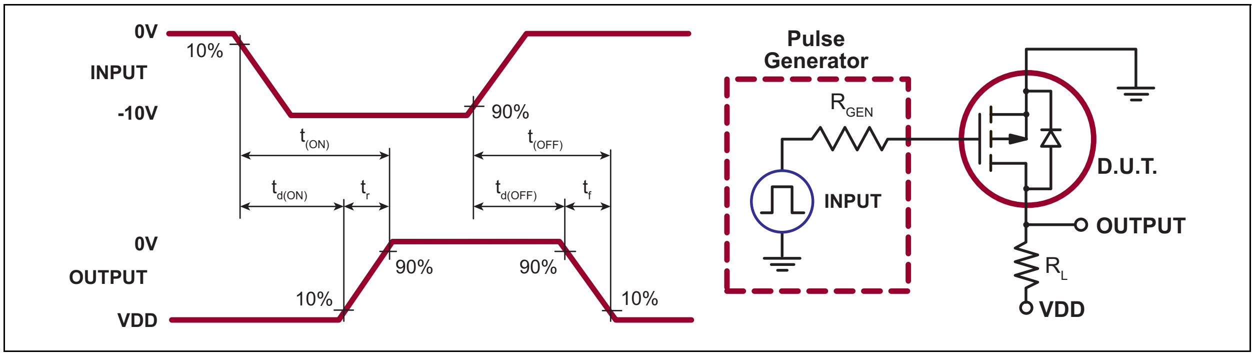


*FIGURE 4-1: Switching Waveforms and Test Circuit.*

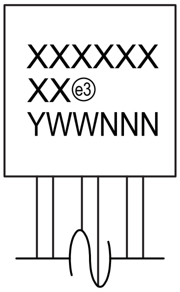
**TABLE 4-1: PRODUCT SUMMARY**

| $BV_{DSS}/BV_{DGS}$ (V) | $R_{DS(ON)}$ (Maximum) (Ω) | $I_{D(ON)}$ (Minimum) (A) | $V_{GS(th)}$ (Maximum) (V) |
|---|---|---|---|
| –400 | 15 | –2 | –0.7 |

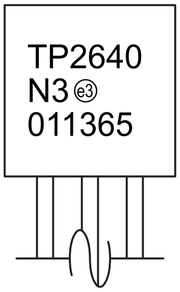
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

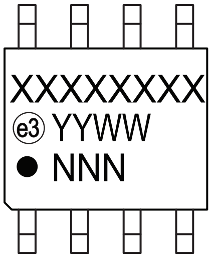
3-lead TO-92



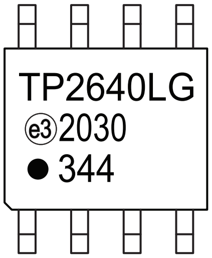
Example



8-lead SOIC



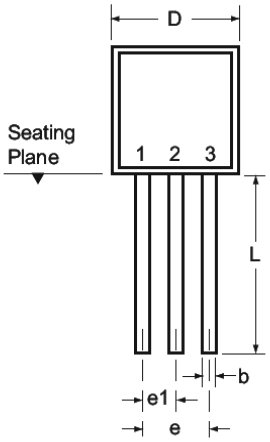
Example



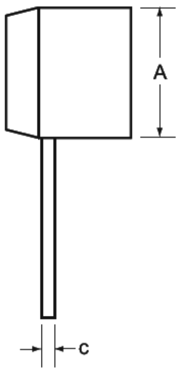
| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | e3 | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

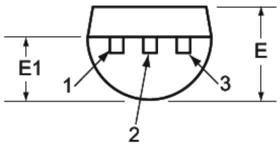
## 3-Lead TO-92 Package Outline (L/LL/N3)



**Front View**



**Side View**



**Bottom View**

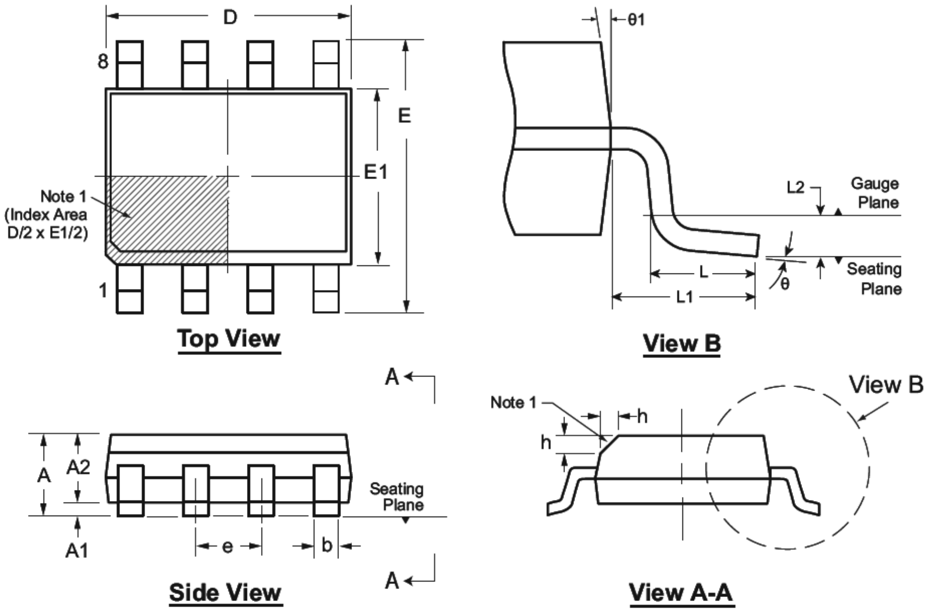
Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

| Symbol | | A | b | c | D | E | E1 | e | e1 | L |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (inches) | MIN | .170 | .014† | .014† | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022† | .022† | .205 | .165 | .105 | .105 | .055 | .610* |

*JEDEC Registration TO-92.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***

## 8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

***4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch***



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

***Note:***

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 4.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 4.90 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* | | 0.50 | 1.27 | | | 8° | 15° |

*JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.*

** This dimension is not specified in the JEDEC drawing.*

***Drawings are not to scale.***

## APPENDIX A: REVISION HISTORY

### Revision A (July 2020)

- Converted Supertex Doc# DSFP-TP2640 to Microchip DS20006372A
- Changed the package marking format
- Updated the quantity of the 8-lead SOIC LG package from 2500/Reel to 3300/Reel to align it with the actual BQM
- Removed the P002, P003, P005, P013, P014 media types for the 3-lead TO-92 N3 package
- Made minor text changes throughout the document

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| **Device** | **Package Options** | | **Environmental** | | **Media Type** |

| | | | |
|---|---|---|---|
| Device: | TP2640 | = | P-Channel Enhancement-Mode Vertical DMOS FET |
| Packages: | N3 | = | 3-lead TO-92 |
| | LG | = | 8-lead SOIC |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package |
| Media Types: | (blank) | = | 1000/Bag for an N3 Package |
| | (blank) | = | 3300/Reel for an LG Package |

**Examples:**

| | |
|---|---|
| a) TP2640N3-G: | P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag |
| b) TP2640LG-G: | P-Channel Enhancement-Mode Vertical DMOS FET, 8-lead SOIC, 3000/Reel |

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