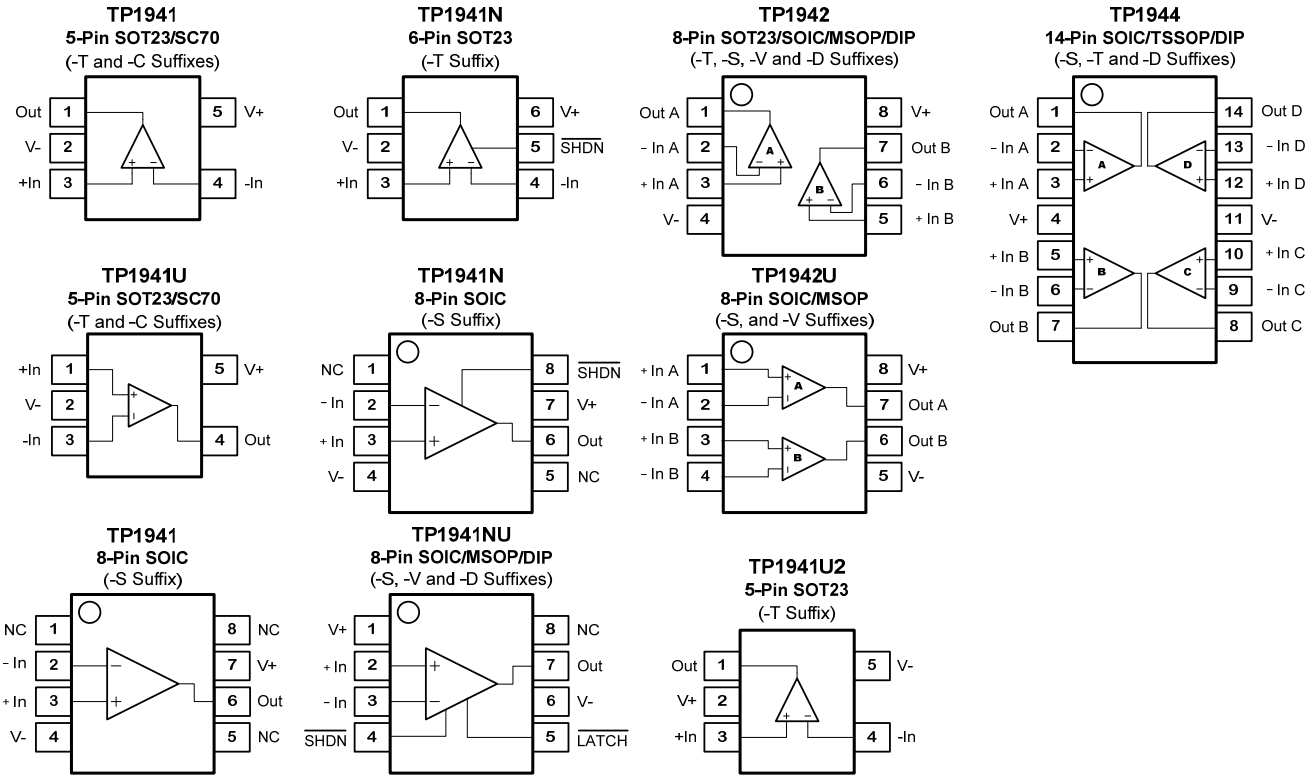
68ns, 1.8V, Ultra-low Power, RRI, Push-Pull Output Comparators

Pin Configuration (Top View)



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP1941	TP1941-TR	5-Pin SOT23	Tape and Reel, 3000	C4TYW (1)
	TP1941-CR	5-Pin SC70	Tape and Reel, 3000	C4CYW (1)
	TP1941-SR	8-Pin SOIC	Tape and Reel, 4000	1941S
TP1941U	TP1941U-TR	5-Pin SOT23	Tape and Reel, 3000	C4AYW (1)
	TP1941U-CR	5-Pin SC70	Tape and Reel, 3000	C4UYW (1)
TP1941U2	TP1941U2-TR	5-Pin SOT23	Tape and Reel, 3000	C4EYW (1)
TP1941N	TP1941N-TR	6-Pin SOT23	Tape and Reel, 3000	C4NYW (1)
	TP1941N-SR	8-Pin SOIC	Tape and Reel, 4000	1941NS
TP1941NU	TP1941NU-SR	8-Pin SOIC	Tape and Reel, 4000	1941NUS
	TP1941NU-VR	8-Pin MSOP	Tape and Reel, 3000	1941NU
	TP1941NU-DR	8-Pin DIP	Tape and Reel, 3000	1941NUD
TP1942	TP1942-TR	8-Pin SOT23	Tape and Reel, 3000	C42YW (1)
	TP1942-SR	8-Pin SOIC	Tape and Reel, 4000	1942S
	TP1942-VR	8-Pin MSOP	Tape and Reel, 3000	1942V
	TP1942-DR	8-Pin DIP	Tape and Reel, 3000	1942D
TP1942U	TP1942U-SR	8-Pin SOIC	Tape and Reel, 4000	1942US
	TP1942U-VR	8-Pin MSOP	Tape and Reel, 3000	1942U
TP1944	TP1944-SR	14-Pin SOIC	Tape and Reel, 2500	1944S
	TP1944-TR	14-Pin TSSOP	Tape and Reel, 3000	1944T
	TP1944-DR	14-Pin DIP	Tape and Reel, 3000	1944D

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$.....6.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, Note 2.....±10mA
Output Current: OUT..... ±45mA
Output Short-Circuit Duration Note 3..... Indefinite

Operating Temperature Range.....–40°C to 85°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4500	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1500	kV

Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 27°C. V_{DD} = +1.8V to +5.5V, V_{IN+} = V_{DD}, V_{IN-} = 1.2V, R_{PU}=10kΩ, C_L =15pF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	1.8		5.5	V
V_{OS}	Input Offset Voltage Note 1	V_{CM} = 1.2V		-3	±0.6	+3	mV
V_{OS} TC	Input Offset Voltage Drift Note 1	V_{CM} = 1.2V			0.3		μV/°C
V_{HYST}	Input Hysteresis Voltage Note 1	V_{CM} = 1.2V		4	6	8	mV
V_{HYST} TC	Input Hysteresis Voltage Drift Note 1	V_{CM} = 1.2V			20		μV/°C
I_B	Input Bias Current	V_{CM} = 1.2V			6		pA
I_{OS}	Input Offset Current				4		pA
R_{IN}	Input Resistance				> 100		GΩ
C_{IN}	Input Capacitance	Differential Common Mode			2 4		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = V_{SS} to V_{DD}			70		dB
V_{CM}	Common-mode Input Voltage Range			V_{SS}-0.1		V_{DD}+0.1	V
PSRR	Power Supply Rejection Ratio				75		dB
V_{OH}	High-Level Output Voltage	I_{OUT}=-1mA	●	V_{DD}-0.3			V
V_{OL}	Low-Level Output Voltage	I_{OUT}=1mA	●			V_{SS}+0.3	V
I_{SC}	Output Short-Circuit Current	Sink or source current			25		mA
I_Q	Quiescent Current per Comparator				46	58	μA
$I_{Q(off)}$	Supply Current in Shutdown Note 2					1.5	μA
V_{IL}	SHDN Input Low Voltage Note 2	Disable	●			0.2V_{DD}	V
V_{IH}	SHDN Input High Voltage Note 2	Enable	●	0.8V_{DD}			V
t_{ON}	Turn-On Time Note 2	SHDN Toggle from V_{SS} to V_{DD}			15		μs
t_{OFF}	Turn-Off Time Note 2	SHDN Toggle from V_{DD} to V_{SS}			1		μs
t_{LPD}	Latch Propagation Delay Note 3				200		ns
t_R	Rising Time				5		ns
t_F	Falling Time				5		ns
T_{PD+}	Propagation Delay (Low-to-High)	Overdrive=100mV, V_{IN-} =1.2V			89		ns
	Propagation Delay (Low-to-High)	V_{IN+} 0 to VCC, V_{IN-} =1.2V			300		ns
T_{PD-}	Propagation Delay (High-to-Low)	Overdrive=100mV, V_{IN-} =1.2V			93		ns
	Propagation Delay (High-to-Low)	V_{IN+} VCC to 0, V_{IN-} =1.2V			28		ns
T_{PDSKEW}	Propagation Delay Skew	Overdrive=100mV, V_{IN-} =1.2V			-4		ns

Note 1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

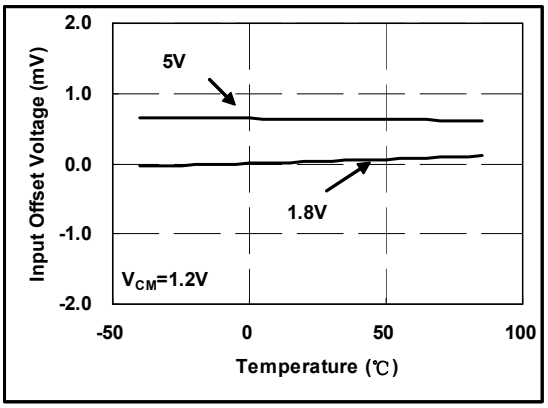
Note 2: Specifications apply to the TP1941N with shutdown.

Note 3: Specifications apply to the TP1941NU with shutdown and latch enable.

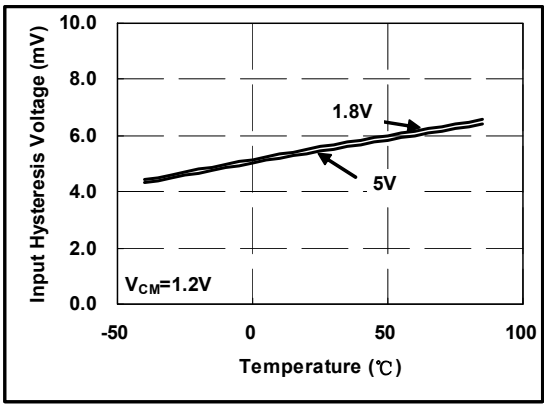
Note 4: Propagation Delay Skew is defined as: $t_{PD-SKEW}$ = t_{PD+} - t_{PD-}.

Typical Performance Characteristics

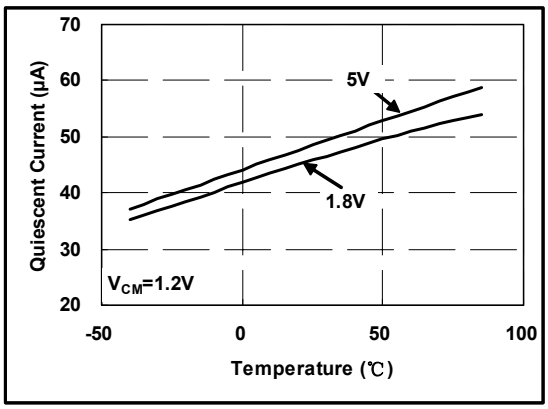
Input Offset Voltage V.S. Temperature



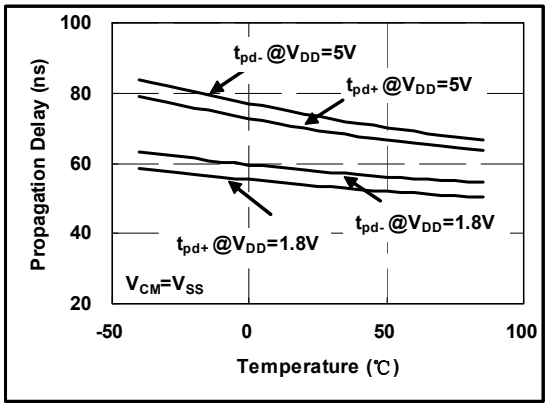
Input Hysteresis Voltage V.S. Temperature



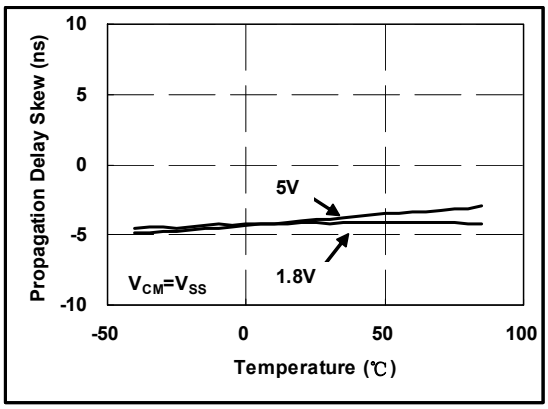
Quiescent Current V.S. Temperature



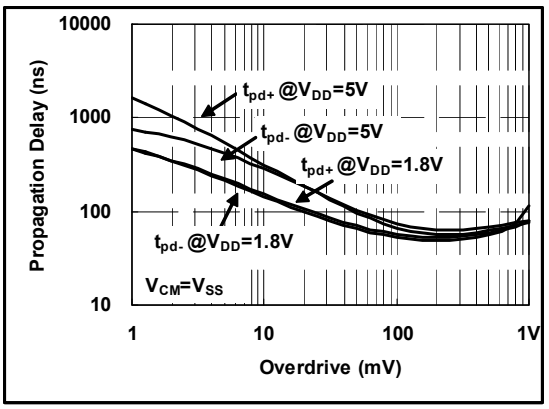
Propagation Delay V.S. Temperature



Propagation Delay Skew V.S. Temperature

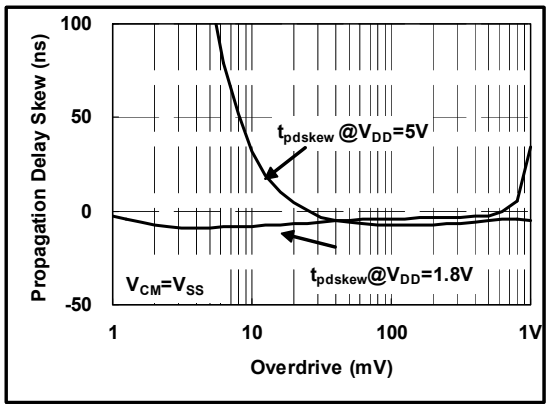


Propagation Delay V.S. Overdrive Voltage

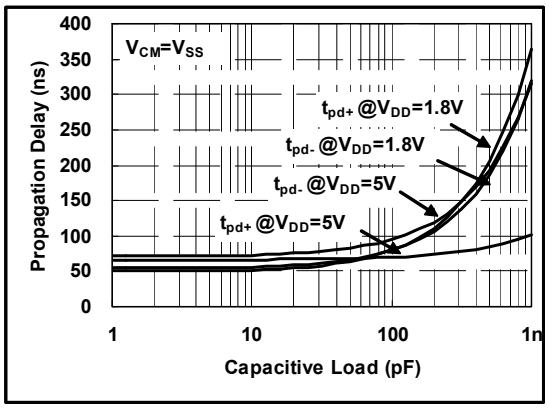


Typical Performance Characteristics

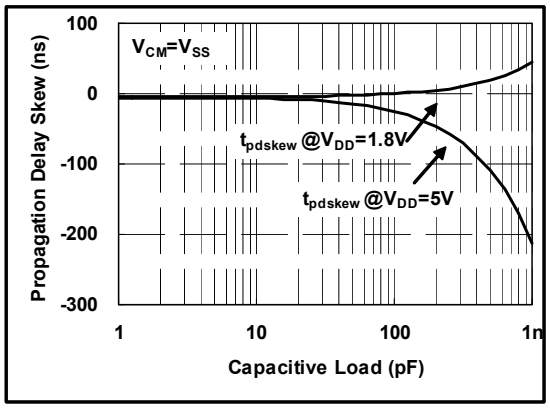
Propagation Delay Skew V.S. Overdrive Voltage



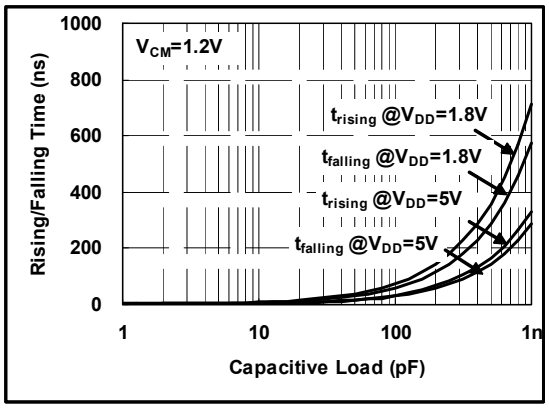
Propagation Delay V.S. Capacitor Loading



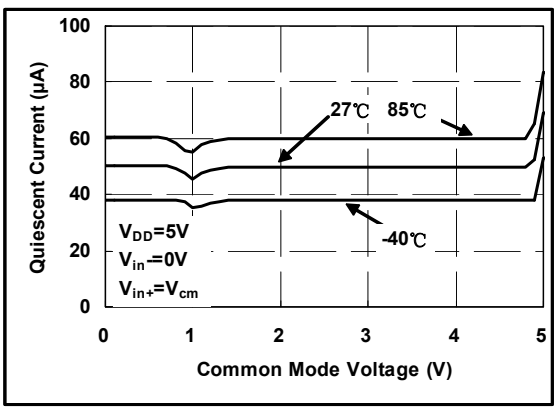
Propagation Delay Skew V.S. Capacitor Loading



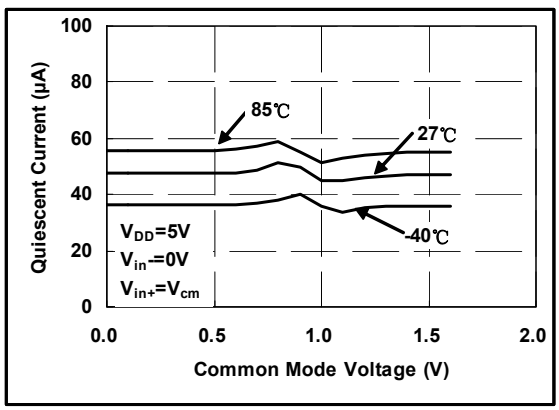
Rising/Falling Time V.S. Capacitor Loading



Quiescent Current V.S. Common Mode Voltage

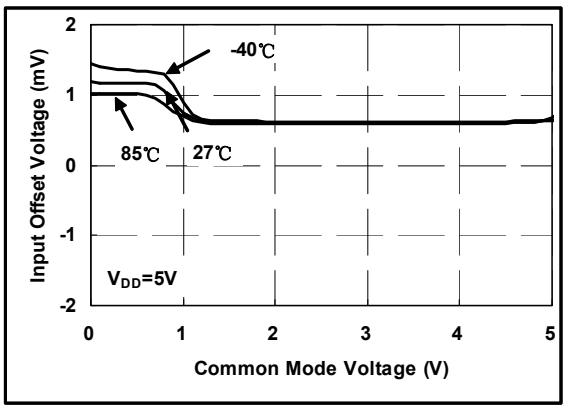


Quiescent Current V.S. Common Mode Voltage

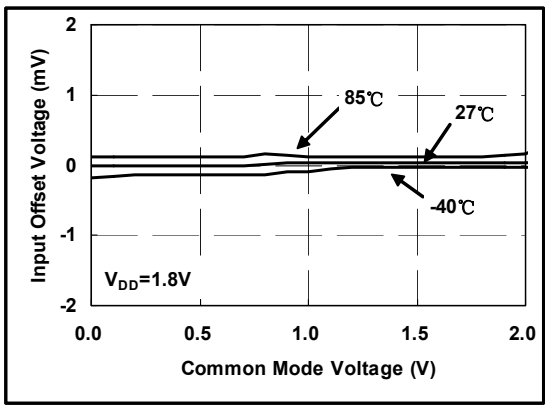


Typical Performance Characteristics

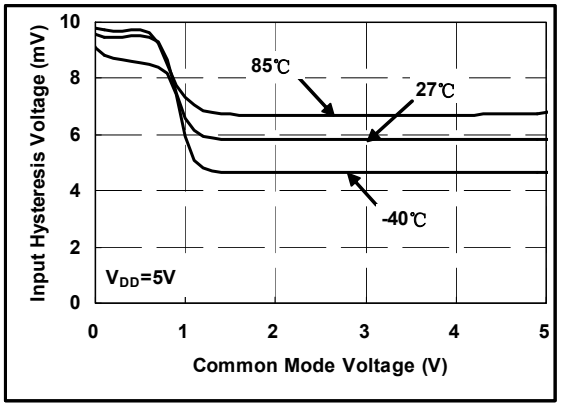
Input Offset Voltage V.S. Common Mode Voltage



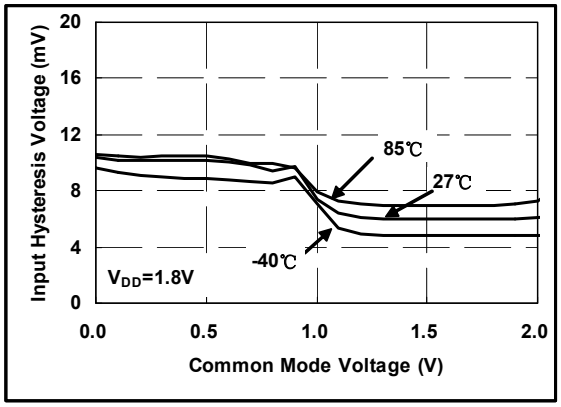
Input Offset Voltage V.S. Common Mode Voltage



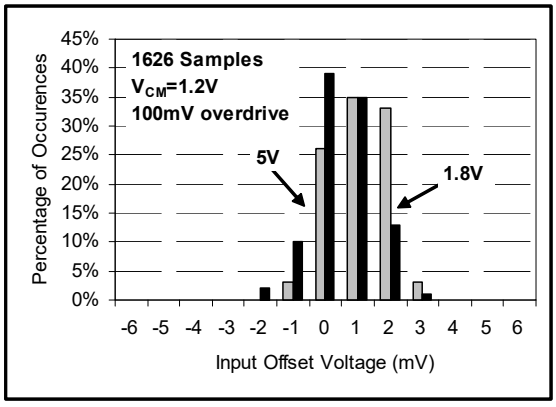
Input Hysteresis Voltage V.S. Common Mode Voltage



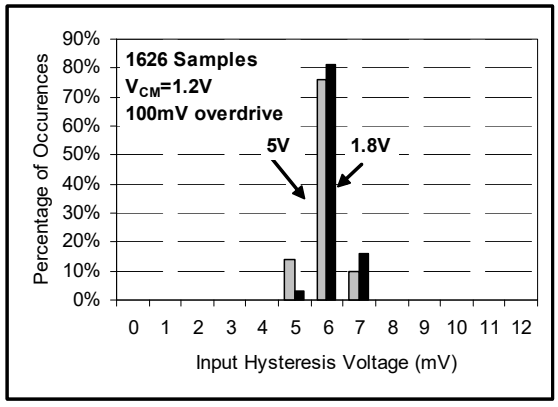
Input Hysteresis Voltage V.S. Common Mode Voltage



Input Offset Voltage Distribution

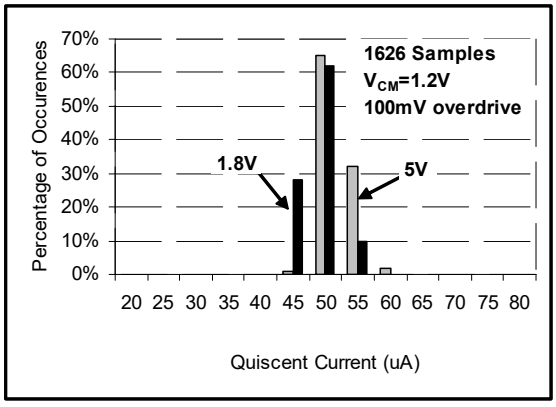


Input Hysteresis Voltage Distribution

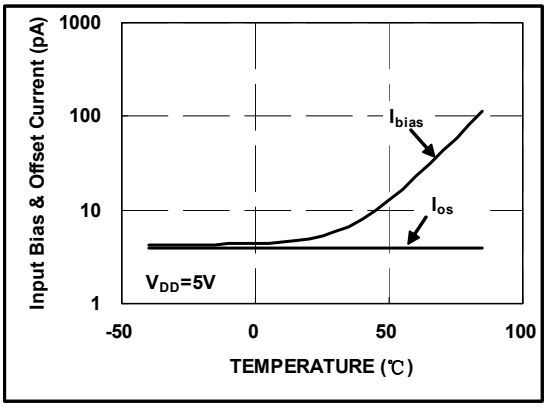


Typical Performance Characteristics

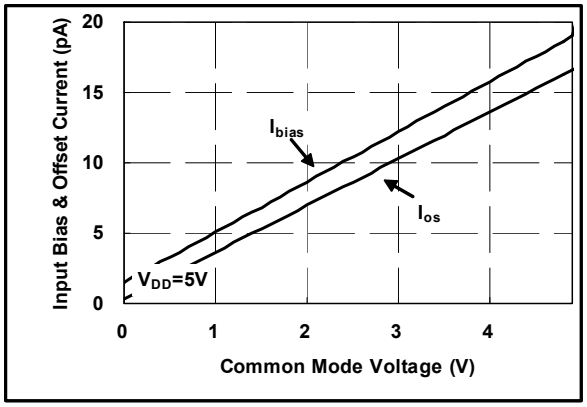
Quiescent Current Distribution



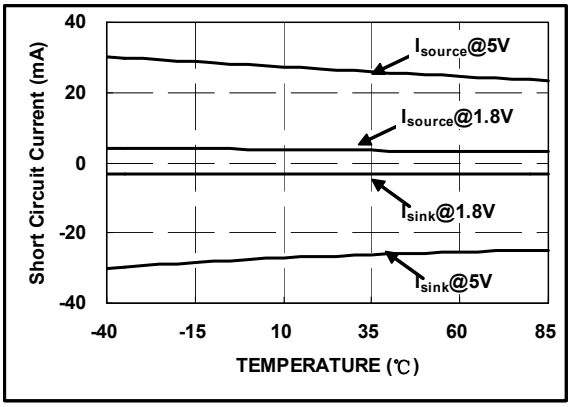
Input Bias and Offset Current V.S. Temperature



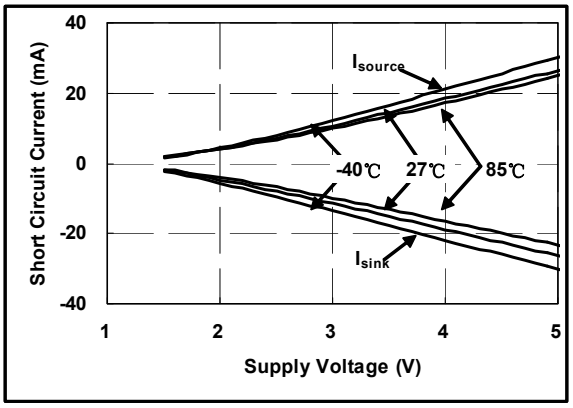
Input Bias Current V.S. Common Mode Voltage



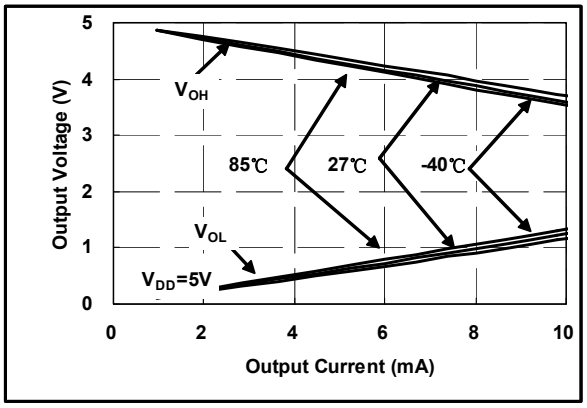
Output Short Circuit Current V.S. Temperature



Output Short Circuit Current V.S. Supply Voltage

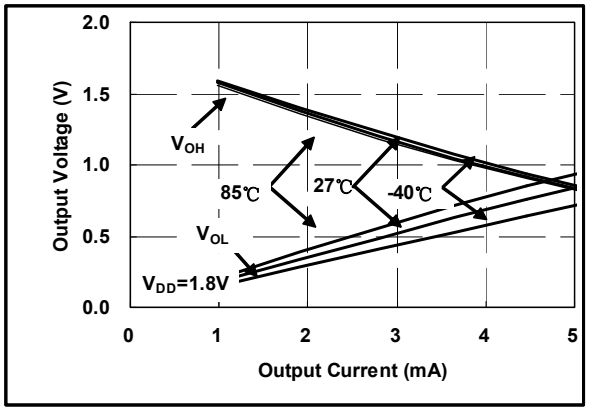


Output Voltage Headroom V.S. Output Current

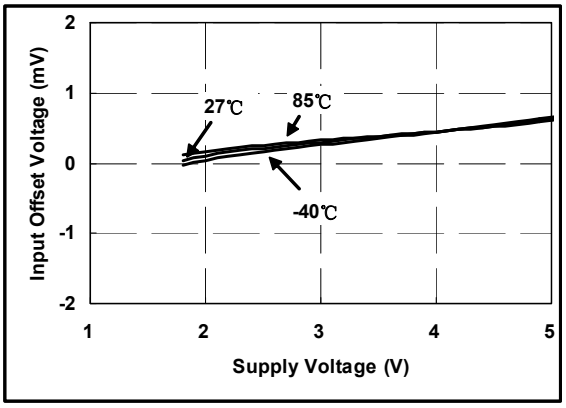


Typical Performance Characteristics

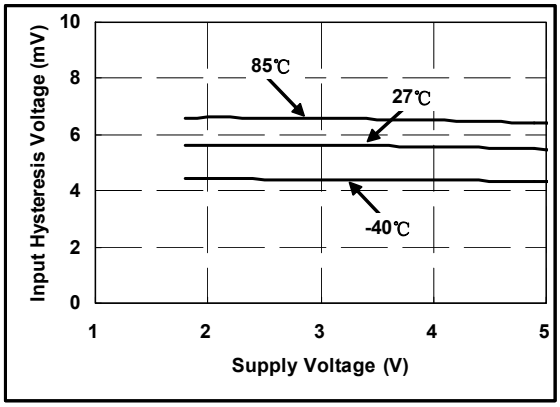
Output Voltage Headroom V.S. Output Current



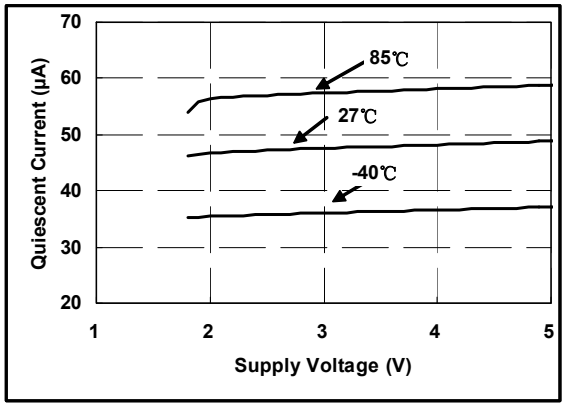
Input Offset Voltage V.S. Supply Voltage



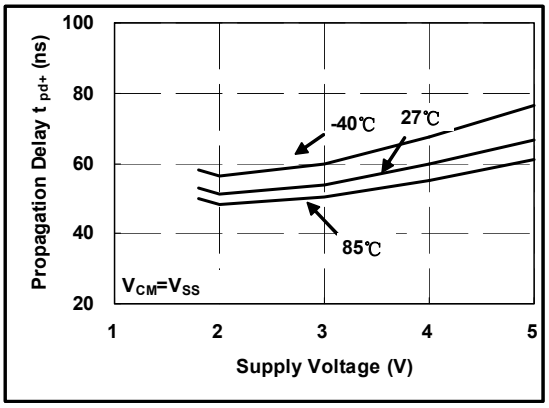
Input Hysteresis Voltage V.S. Supply Voltage



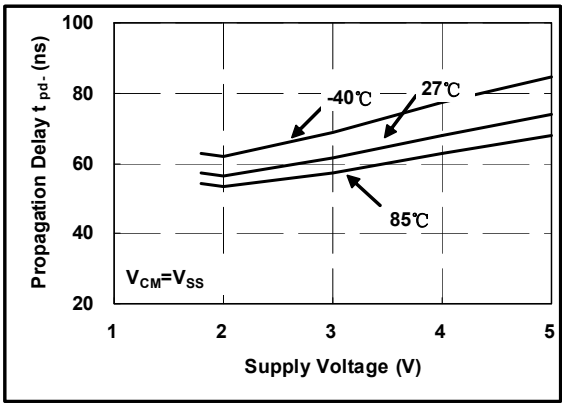
Quiescent Current V.S. Supply Voltage



Low to High Propagation Delay V.S. Supply Voltage

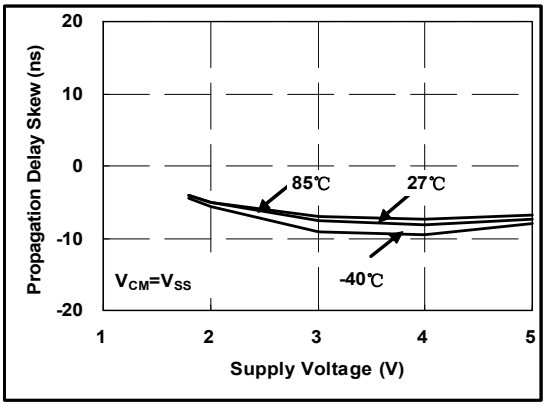


High to low Propagation Delay V.S. Supply Voltage



Typical Performance Characteristics

Propagation Skew Delay V.S. Supply Voltage



Pin Functions

–IN: Inverting Input of the Comparator. Voltage range of this pin can go from V^- – 0.3V to V^+ + 0.3V.

+IN: Non-Inverting Input of Comparator. This pin has the same voltage range as –IN.

V+ (V_{DD}): Positive Power Supply. Typically the voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V+ and V– is between 1.8V and 5.5V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

N/C: No Connection.

V^- (V_{SS}): Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

$\overline{\text{SHDN}}$: Active **Low** Shutdown. Shutdown threshold is 1/2V+ above negative supply rail.

$\overline{\text{LATCH}}$: Active **Low** Latch enable. Latch enable threshold is 1/2V+ above negative supply rail.

OUT: Comparator Output. The voltage range extends to within millivolts of each supply rail.

Operation

The TP194x family single-supply comparators feature internal hysteresis, high speed, and low power. Input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is active over different ranges of common mode input voltage. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment.

Applications Information

Inputs

The TP194x comparator family uses CMOS transistors at the input which prevent phase inversion when the input pins exceed the supply voltages. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion.

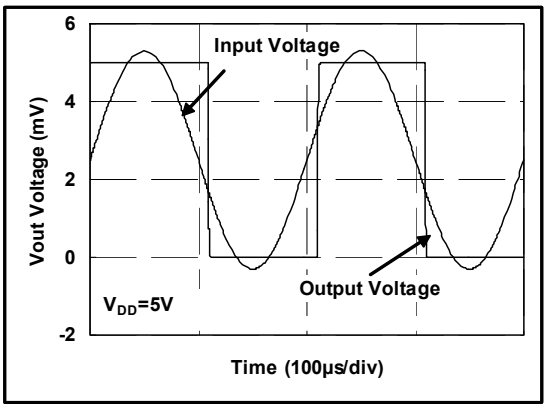


Figure 1. Comparator Response to Input Voltage

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed supply voltages, as shown in Figure 2. Large differential voltages exceeding the supply voltage should be avoided to prevent damage to the input stage.

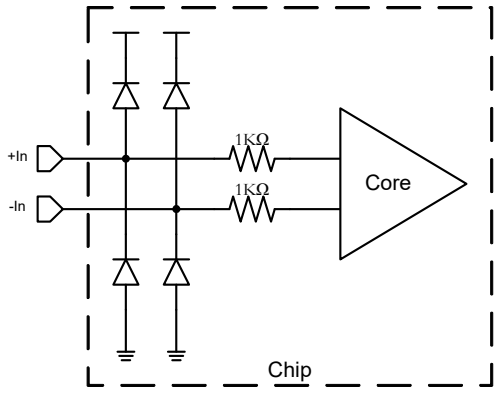


Figure 2. Equivalent Input Structure

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the TP194x implements internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the

input out of the region where oscillation occurs. Figure 3 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

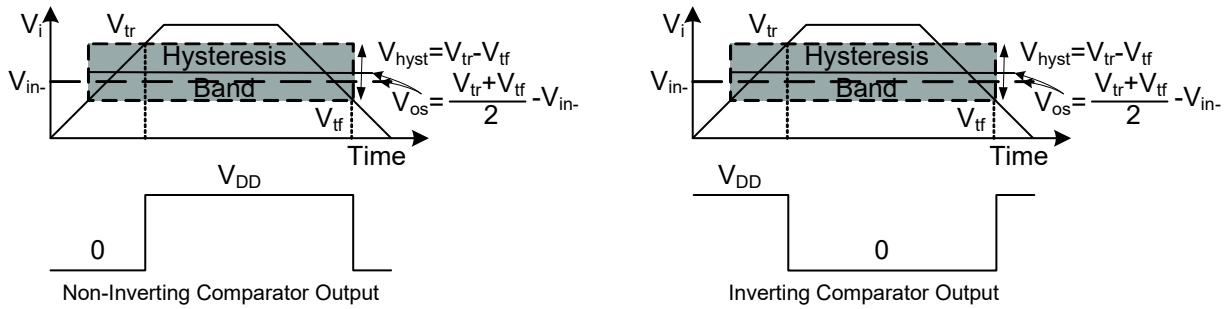


Figure 3. Comparator's hysteresis and offset

External Hysteresis

Greater flexibility in selecting hysteresis is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). Output chatter also increases the dynamic supply current.

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 4 and a voltage reference (V_r) at the inverting input.

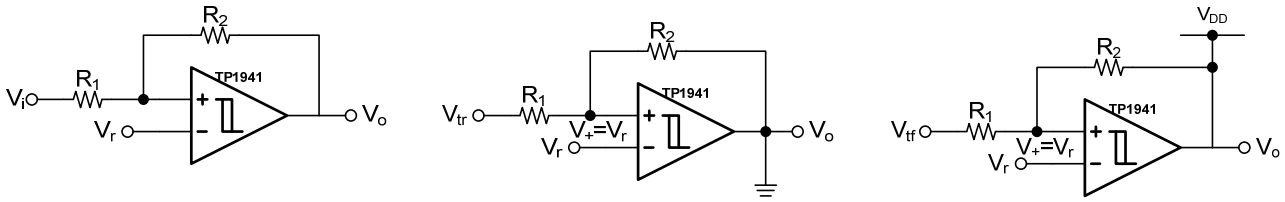


Figure 4. Non-Inverting Configuration with Hysteresis

When V_i is low, the output is also low. For the output to switch from low to high, V_i must rise up to V_{tr}. When V_i is high, the output is also high. In order for the comparator to switch back to a low state, V_i must equal V_{tf} before the non-inverting input V_+ is again equal to V_r.

$$V_r = \frac{R_2}{R_1 + R_2} V_{tr}$$

$$V_r = (V_{DD} - V_{tf}) \frac{R_1}{R_1 + R_2} + V_{tf}$$

$$V_{tr} = \frac{R_1 + R_2}{R_2} V_r$$

$$V_{tf} = \frac{R_1 + R_2}{R_2} V_r - \frac{R_1}{R_2} V_{DD}$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1}{R_2} V_{DD}$$

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{DD}), as shown in Figure 5.

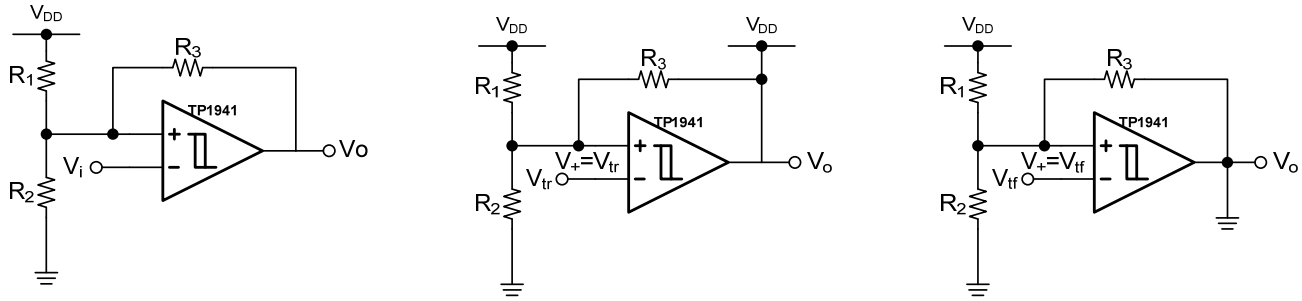


Figure 5. Inverting Configuration with Hysteresis

When V_i is greater than V_+, the output voltage is low. In this case, the three network resistors can be presented as paralleled resistor R_2 || R_3 in series with R_1. When V_i at the inverting input is less than V_+, the output voltage is high. The three network resistors can be represented as R_1 ||R_3 in series with R_2.

$$V_{tr} = \frac{R_2}{R_1 \parallel R_3 + R_2} V_{DD}$$

$$V_{tf} = \frac{R_2 \parallel R_3}{R_2 \parallel R_3 + R_1} V_{DD}$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_3} V_{DD}$$

Low Input Bias Current

The TP194x family is a CMOS comparator family and features very low input bias current in pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP194x’s input bias current at +27°C (±6pA, typical). It is recommended to use multi-layer PCB layout and route the comparator’s -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 6 for Inverting configuration application.

1. For Non-Inverting Configuration:

   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.

   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the same reference as the comparator.

2. For Inverting Configuration:

   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD}/2 or ground).

   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

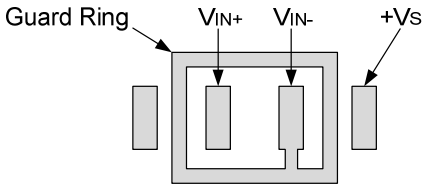


Figure 6. Example Guard Ring Layout for Inverting Comparator

Ground Sensing and Rail to Rail Output

The TP194x family implements a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300mV beyond either rail, the comparator can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage of the comparator increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit condition. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP194x family has reverse-biased ESD protection diodes on all inputs and output. Input and output pins can not be biased more than 300mV beyond either supply rail.

Shut-down

The TP1941N/TP1941NU has $\overline{\text{SHDN}}$ pins that can shut down the amplifier to less than 1.5μA supply current. The $\overline{\text{SHDN}}$ pin voltage needs to be within 0.2V+ of V– for the amplifier to shut down. During shutdown, the output will be in high output resistance state, which is suitable for multiplexer applications. It should be noted that $\overline{\text{SHDN}}$ pin is forbidden to be left floating.

Latch-enable

The TP1941NU includes an internal latch that allows storage of comparison results. The $\overline{\text{LATCH}}$ pin has a high input impedance. If $\overline{\text{LATCH}}$ is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when $\overline{\text{LATCH}}$ is pulled low. All timing constraints must be met when using the latch function (Figure 7).

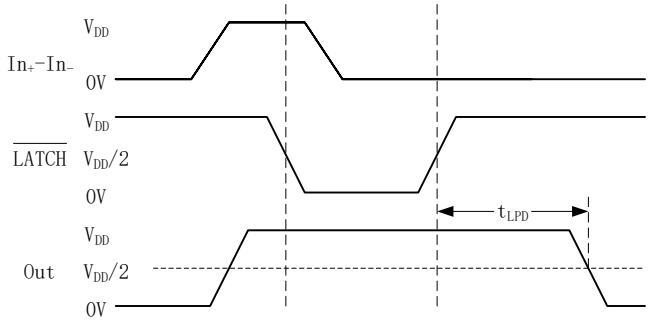


Figure 7. TP1941NU Timing Diagram with Latch Operator

Power Supply Layout and Bypass

The TP194x family's power supply pin should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Good ground layout improves performance by decreasing the amount of stray capacitance and noise at the comparator's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components as close to the comparator' pins as possible.

Proper Board Layout

The TP194x family is a series of fast-switching, high-speed comparator and requires high-speed layout considerations. For best results, the following layout guidelines should be followed:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.

2. Place a decoupling capacitor (0.1μF ceramic, surface-mount capacitor) as close as possible to supply.

3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.

4. Solder the device directly to the PCB rather than using a socket.

5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane should be placed between the output and inputs.

6. The ground pin ground trace should run under the device up to the bypass capacitor, thus shielding the inputs from the outputs.

Typical Applications

IR Receiver

The TP1941 is an ideal candidate to be used as an infrared receiver shown in Figure 8. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions. Optional R_o provides additional hysteresis for noise immunity.

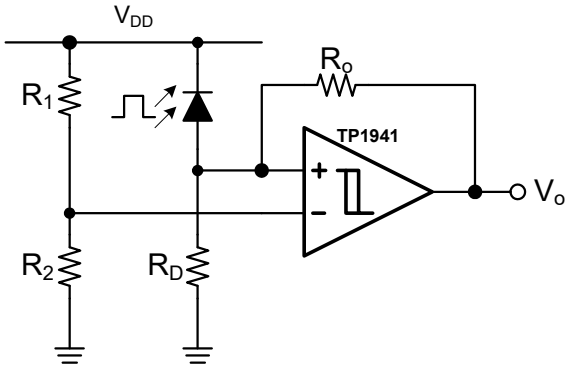


Figure 8. IR Receiver

Relaxation Oscillator

A relaxation oscillator using TP1941 is shown in Figure 9. Resistors R_1 and R_2 set the bias point at the comparator's inverting input. The period of oscillator is set by the time constant of R_4 and C_1. The maximum frequency is limited by the large signal propagation delay of the comparator. TP1941's low propagation delay guarantees the high frequency oscillation.

If the inverted input (V_{C1}) is lower than the non-inverting input (V_A), the output is high which charges C_1 through R_4 until V_{C1} is equal to V_A. The value of V_A at this point is

$$V_{A1} = \frac{V_{DD} \bullet R_2}{R_1 \parallel R_3 + R_2}$$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{DD} \bullet R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$

If $R_1=R_2=R_3$, then $V_{A1}=2V_{DD}/3$, and $V_{A2}= V_{DD}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{DD}/3$ to $V_{DD}/3$. Hence the frequency is:

$$Freq = \frac{1}{2 \bullet \ln 2 \bullet R_4 \bullet C_1}$$

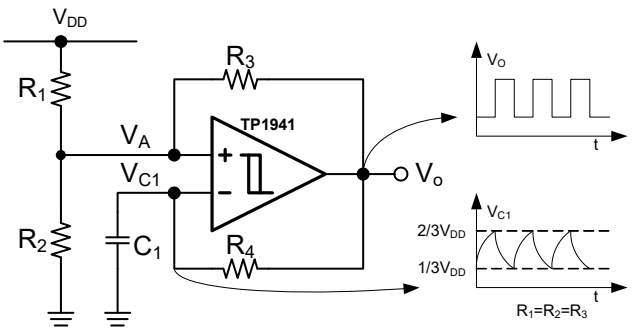


Figure 9. Relaxation Oscillator

Windowed Comparator

Figure 10 shows one approach to designing a windowed comparator using a single TP1942 chip. Choose different thresholds by changing the values of R1, R2, and R3. OutA provides an active-low undervoltage indication, and OutB gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal. When input voltage V_i reaches the overvoltage threshold V_{OH}, the OutB gets low. Once V_i falls to the undervoltage threshold V_{UH}, the OutA gets low. When $V_{UH}<V_i<V_{OH}$, the AND Gate gets high.

$$V_{OH} = V_r \bullet (R_1 + R_2 + R_3)/R_1$$

$$V_{UH} = V_r \bullet (R_1 + R_2 + R_3)/(R_1 + R_2)$$

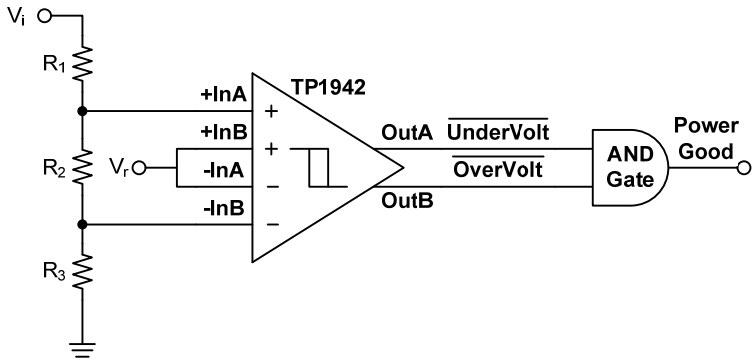
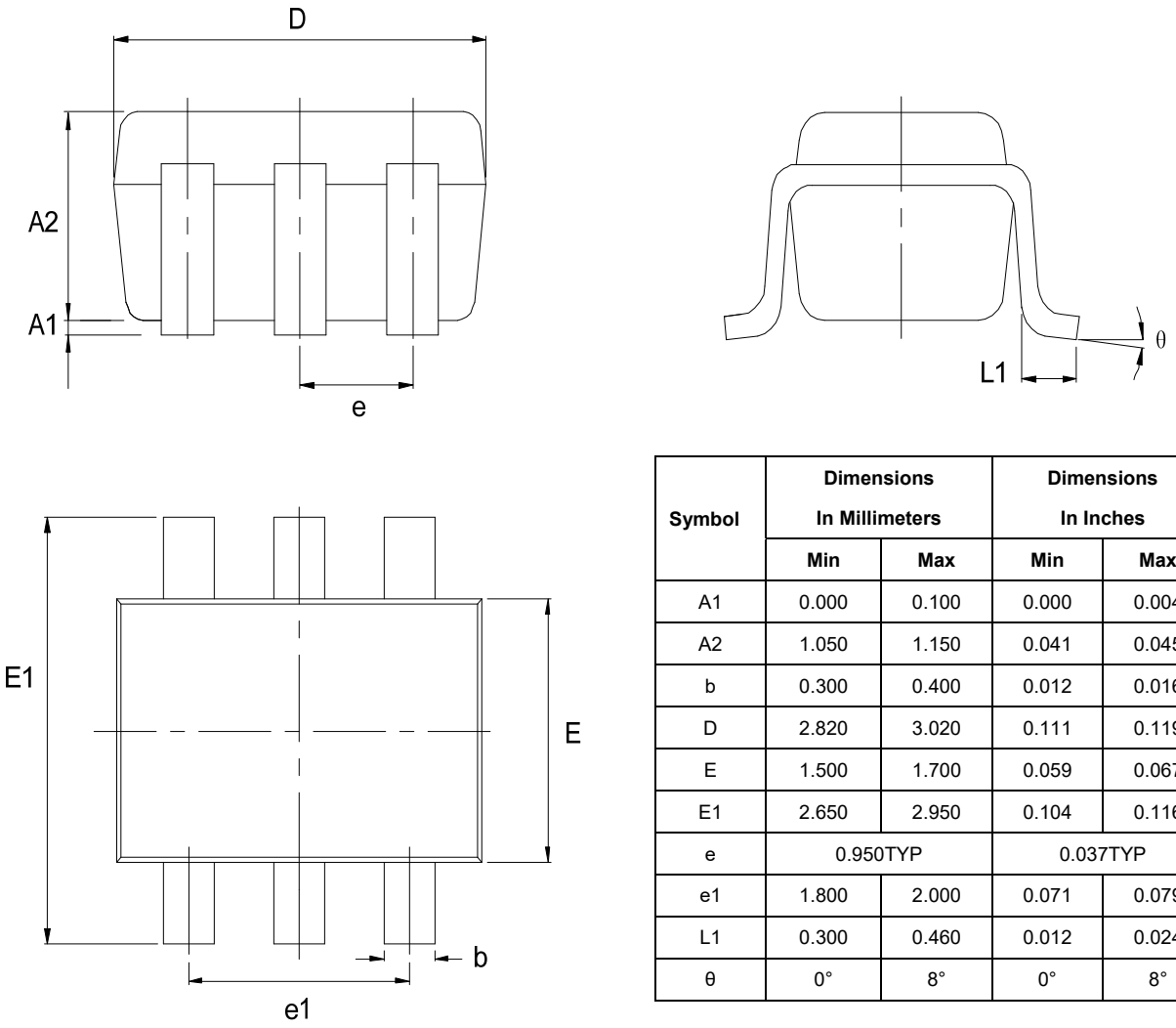


Figure 10. Windowed Comparator

Package Outline Dimensions

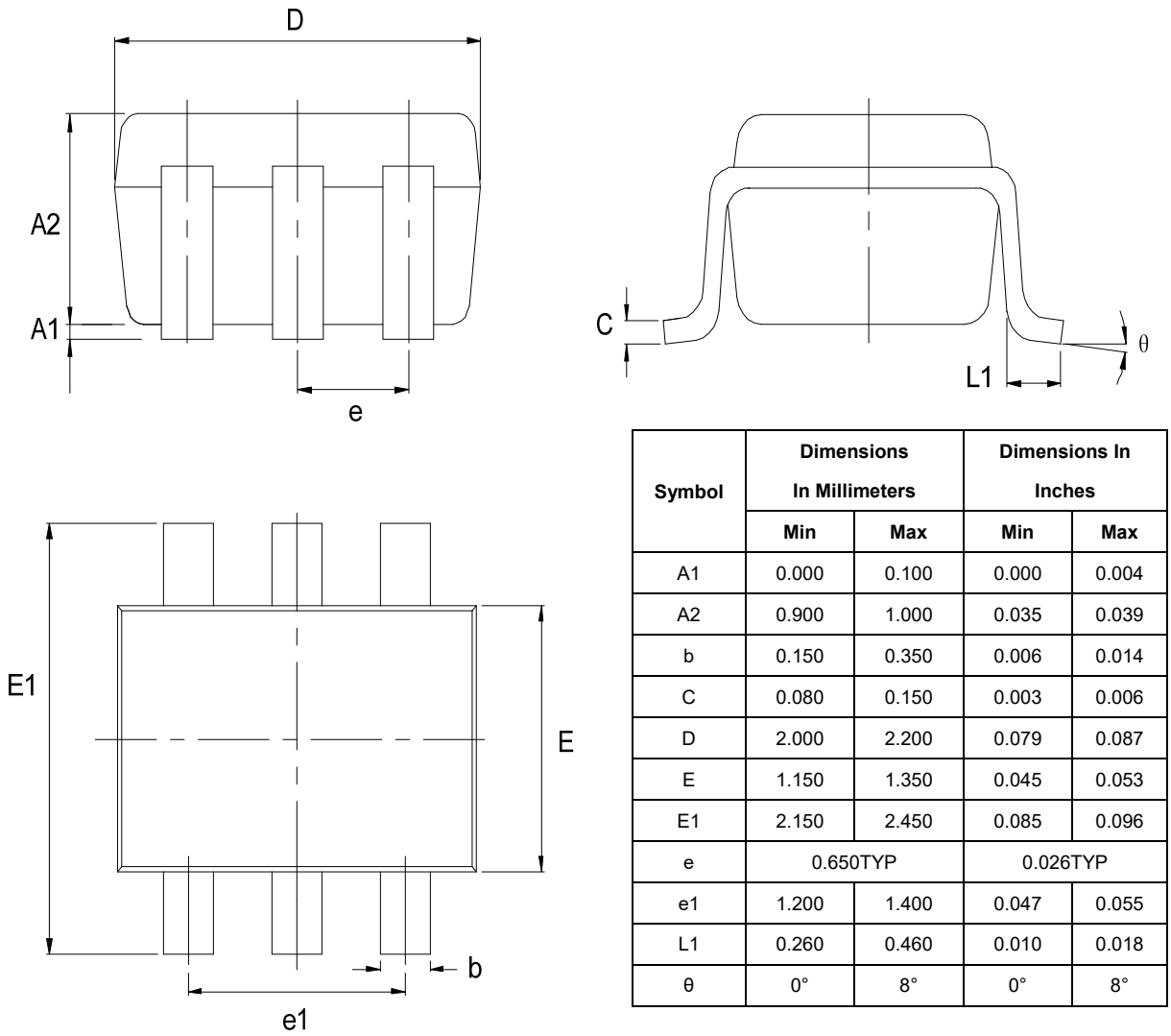
SOT23-5 / SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

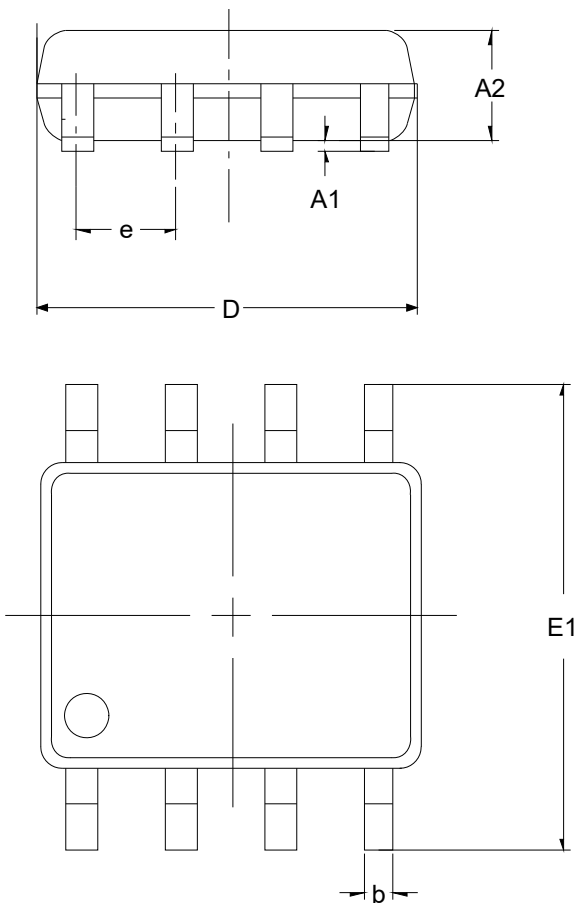
SC-70-5 / SC-70-6 (SOT353 / SOT363)

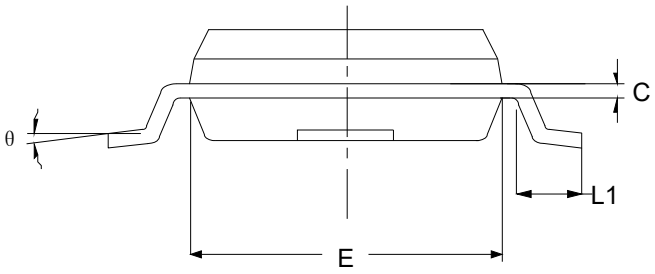


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Package Outline Dimensions

SO-8 (SOIC-8)

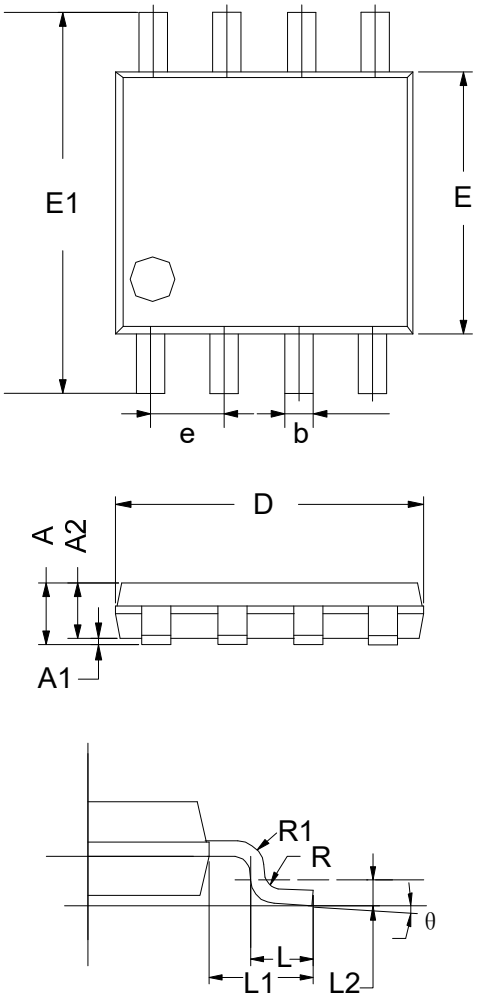




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

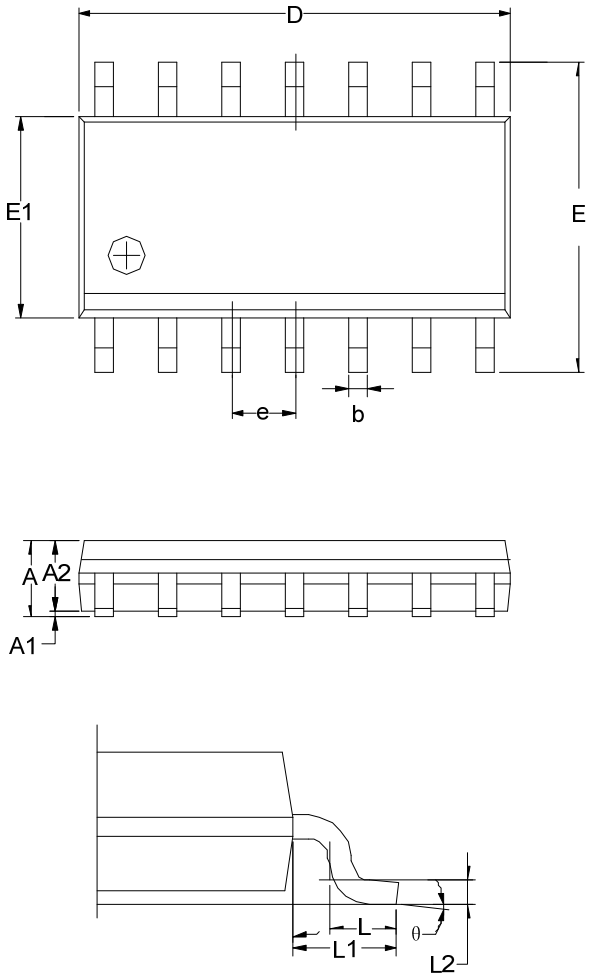
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

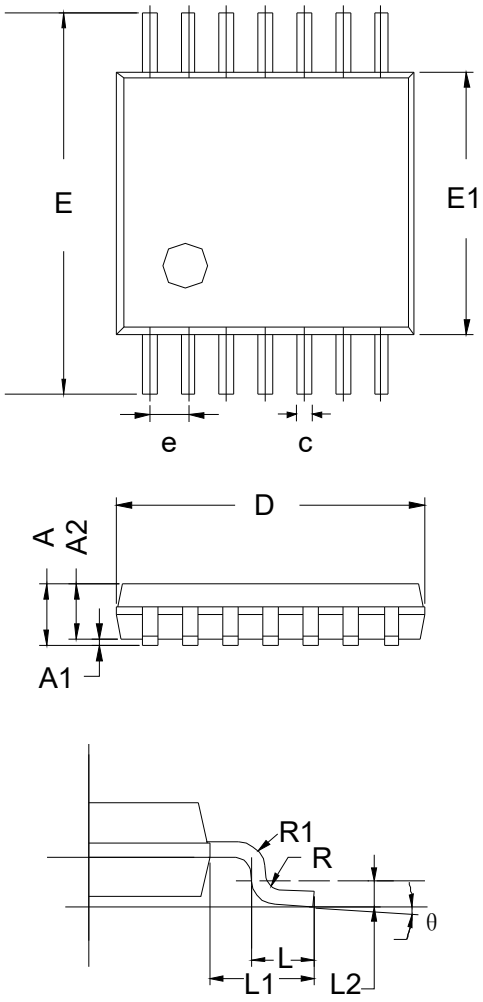
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°