

TP1271 / TP1272 / TP1274

36V Single supply, Precision RRO Op-amps With 7MHz Bandwidth

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP1271	TP1271-SR	8-Pin SOIC	Tape and Reel, 4,000	TP1271
	TP1271-TR	5-Pin SOT23	Tape and Reel, 3,000	D12T
TP1272	TP1272-SR	8-Pin SOIC	Tape and Reel, 4,000	TP1272
	TP1272-VR	8-Pin MSOP	Tape and Reel, 3,000	TP1272
TP1274	TP1274-SR	14-Pin SOIC	Tape and Reel, 2,500	TP1274
	TP1274-TR	14-Pin TSSOP	Tape and Reel, 3,000	TP1274

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$ Note 2 40.0V
Input Voltage..... $V^- - 0.3$ to $V^+ + 0.3$
Input Current: $+I_{IN}$, $-I_{IN}$ Note 3 $\pm 20\text{mA}$
Output Short-Circuit Duration Note 4 Indefinite
Current at Supply Pins..... $\pm 60\text{mA}$

Operating Temperature Range..... -40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	3	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin SOT23	250	81	$^\circ\text{C/W}$
8-Pin SOIC	158	43	$^\circ\text{C/W}$
8-Pin MSOP	210	45	$^\circ\text{C/W}$
14-Pin SOIC	120	36	$^\circ\text{C/W}$
14-Pin TSSOP	180	35	$^\circ\text{C/W}$

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Electrical Characteristics

The specifications are at $T_A = 27^\circ\text{C}$. $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$, $R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$. Unless otherwise noted.

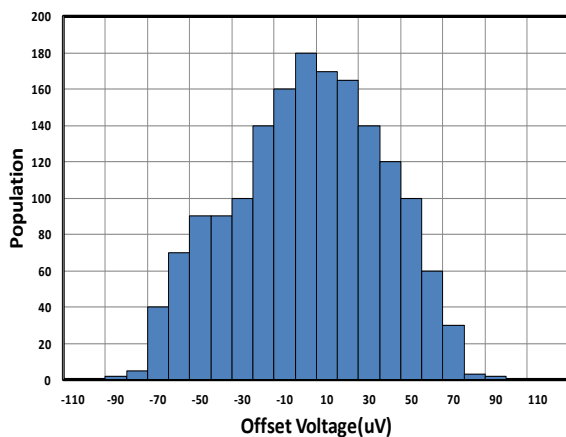
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V_{\text{DD}}/2$	-150	± 50	+150	μV
$V_{\text{OS TC}}$	Input Offset Voltage Drift	-40°C to 125°C		0.9		$\mu\text{V}/^\circ\text{C}$
I_{B}	Input Bias Current	$T_A = 27^\circ\text{C}$		3		pA
		$T_A = 85^\circ\text{C}$		250		pA
		$T_A = 125^\circ\text{C}$		7.7		nA
I_{OS}	Input Offset Current			0.001		pA
V_{n}	Input Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		2.35		μV_{RMS}
e_{n}	Input Voltage Noise Density	$f = 1\text{kHz}$		19		$\text{nV}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	Differential		4		pF
		Common Mode		2.5		
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -14.6\text{V}$ to 13V		126		dB
V_{CM}	Common-mode Input Voltage Range		$V - 0.3$		$V - 2.0$	V
PSRR	Power Supply Rejection Ratio			130		dB
A_{VOL}	Open-Loop Large Signal Gain	$R_{\text{LOAD}} = 2\text{k}\Omega$	100	118		dB
$V_{\text{OL}}, V_{\text{OH}}$	Output Swing from Supply Rail	$R_{\text{LOAD}} = 100\text{k}\Omega$		50		mV
R_{OUT}	Closed-Loop Output Impedance	$G = 1$, $f = 1\text{kHz}$, $I_{\text{OUT}} = 0$		0.01		Ω
R_{O}	Open-Loop Output Impedance	$f = 1\text{kHz}$, $I_{\text{OUT}} = 0$		125		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current		80		mA
V_{DD}	Supply Voltage		2.7		36	V
I_{Q}	Quiescent Current per Amplifier			900		μA
PM	Phase Margin	$R_{\text{LOAD}} = 2\text{k}\Omega$, $C_{\text{LOAD}} = 100\text{pF}$		60		$^\circ$
GM	Gain Margin	$R_{\text{LOAD}} = 2\text{k}\Omega$, $C_{\text{LOAD}} = 100\text{pF}$		8		dB
GBWP	Gain-Bandwidth Product	$f = 1\text{kHz}$		7		MHz
SR	Slew Rate	$A_{\text{V}} = 1$, $V_{\text{OUT}} = 0\text{V}$ to 10V , $C_{\text{LOAD}} = 100\text{pF}$, $R_{\text{LOAD}} = 2\text{k}\Omega$		20		$\text{V}/\mu\text{s}$
FPBW	Full Power Bandwidth ^{Note 1}			210		kHz
t_{s}	Settling Time, 0.1%	$A_{\text{V}} = -1$, 10V Step		1		μs
	Settling Time, 0.01%			1		
THD+N	Total Harmonic Distortion and Noise	$f = 1\text{kHz}$, $A_{\text{V}} = 1$, $R_L = 2\text{k}\Omega$, $V_{\text{OUT}} = 3.5\text{V}_{\text{RMS}}$		0.0001		%
X_{talk}	Channel Separation	$f = 1\text{kHz}$, $R_L = 2\text{k}\Omega$		110		dB

Note 1: Full power bandwidth is calculated from the slew rate $\text{FPBW} = \text{SR}/\pi \cdot V_{\text{P-P}}$

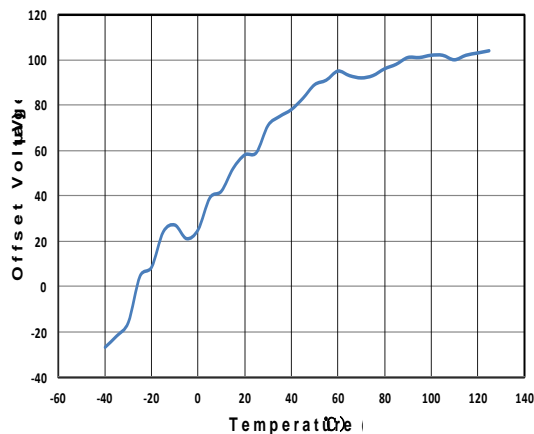
Typical Performance Characteristics

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified.

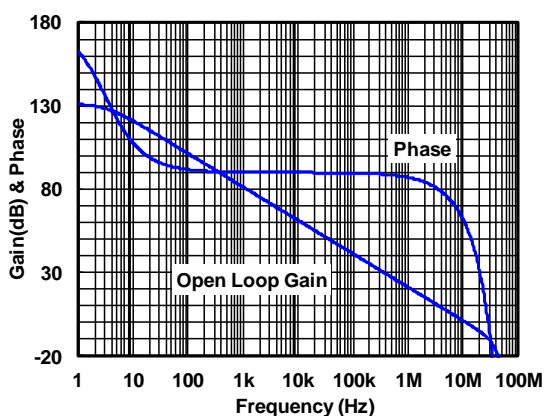
Offset Voltage Production Distribution



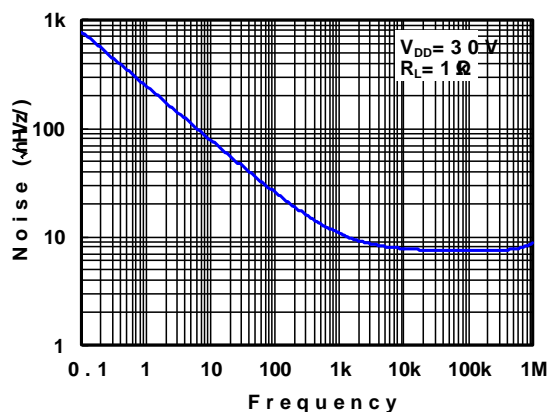
Offset Voltage vs. Temperature



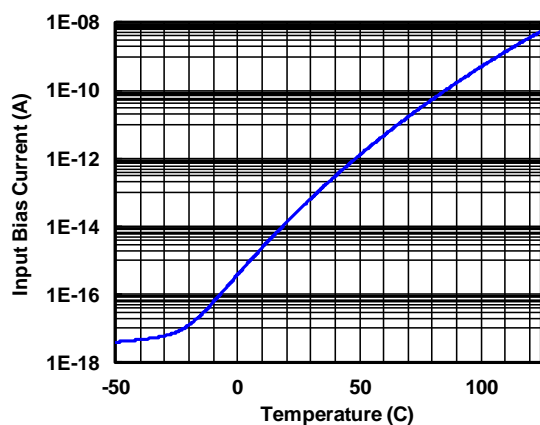
Open-Loop Gain and Phase



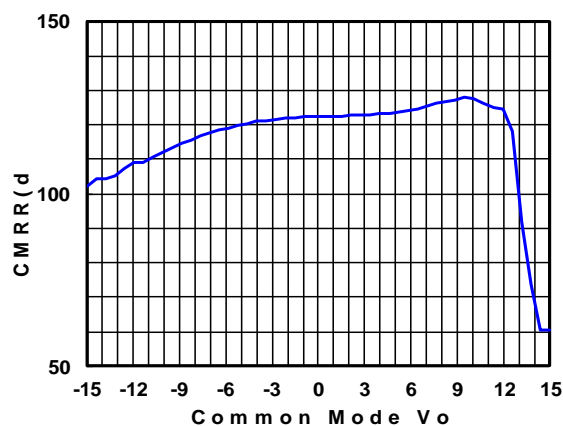
Input Voltage Noise Spectral Density



Input Bias Current vs. Temperature



Input Bias Current vs. Input Common Mode Voltage

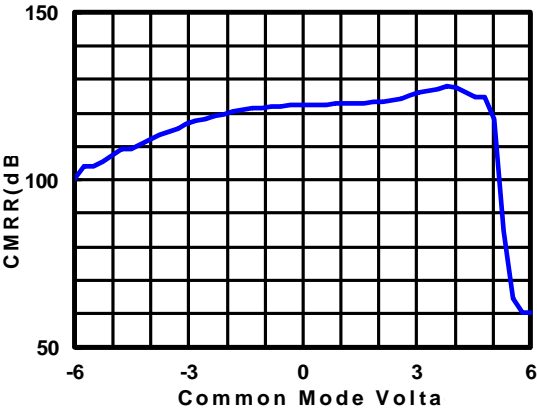


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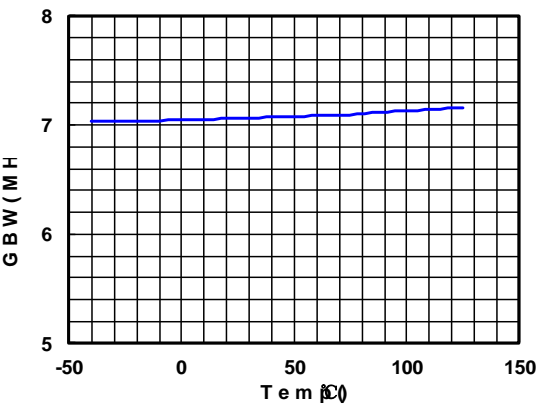
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified.(Continue)

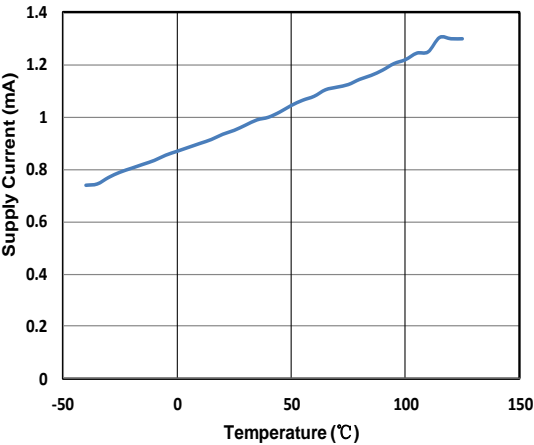
Common Mode Rejection Ratio



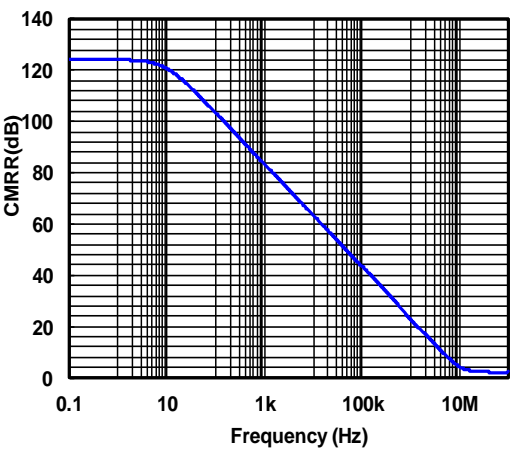
Unity Gain Bandwidth vs. Temperature



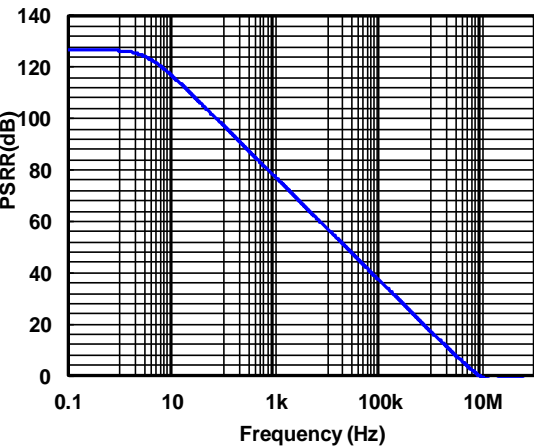
Quiescent Current vs. Temperature



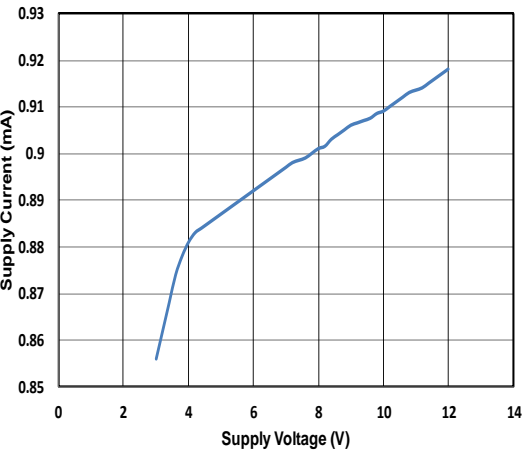
CMRR vs. Frequency



Power-Supply Rejection Ratio



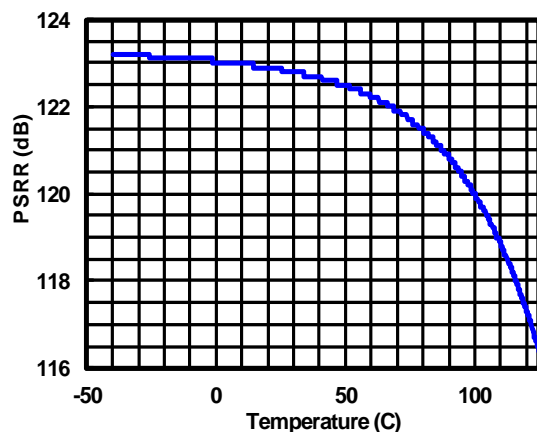
Quiescent Current vs. Supply Voltage



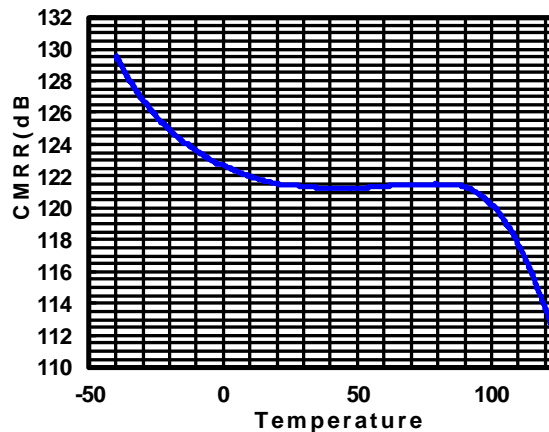
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified. (Continue)

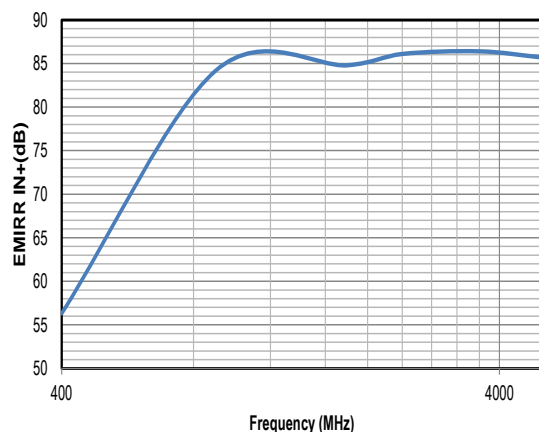
Power-Supply Rejection Ratio vs. Temperature



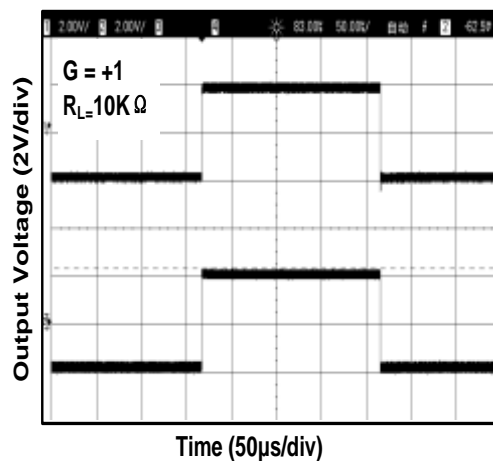
CMRR vs. Temperature



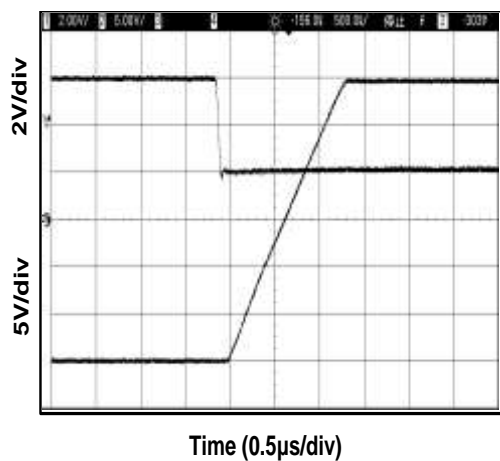
EMIRR IN+ vs. Frequency



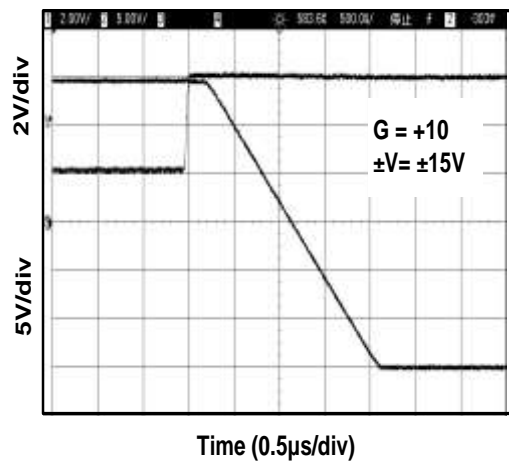
Large-Scale Step Response



Negative Over-Voltage Recovery



Positive Over-Voltage Recovery

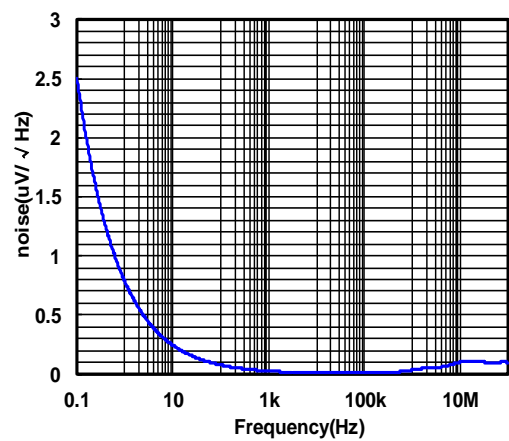


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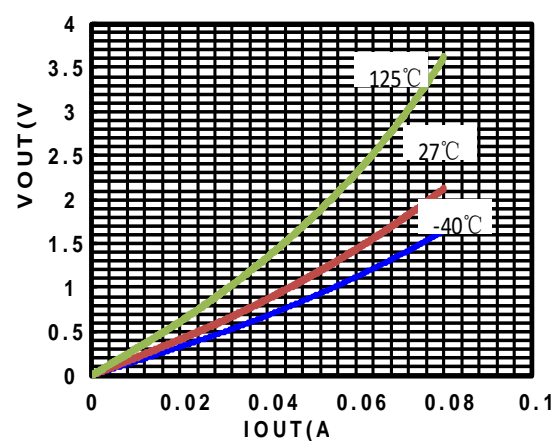
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified.(Continue)

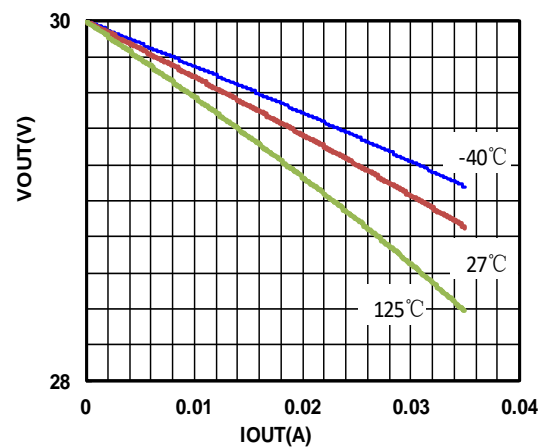
Voltage Noise Spectral Density vs. Frequency



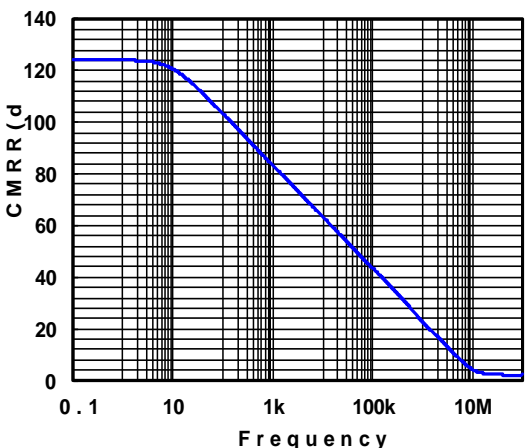
Negative Output Swing vs. Load Current



Positive Output Swing vs. Load Current



CMRR vs. Frequency



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Pin Functions

-IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- to $(V^+ - 2.0V)$.

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as $-IN$.

V^+ or $+V_S$: Positive Power Supply. Typically the voltage is from 2.7V to 36V. Split supplies are possible as long as the voltage between V^+ and V^- is between 2.7V and 36V. A bypass capacitor of 0.1 μ F as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- or $-V_S$: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.7V to 36V. If it is not connected to ground, bypass it

with a capacitor of 0.1 μ F as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within milli-volts of each supply rail.

Operation

The TP127X have input signal range from V^- to $(V^+ - 2.0V)$. The output can extend all the way to the supply rails. The input stage is comprised of a PMOS differential amplifier. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

EMI Harden

The EMI hardening makes the TP1271/1272/1274 a must for almost all op amp applications. Most applications are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The TP1271/1272/1274 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding. Using this EMI resistant series of op amps will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

Wide Supply Voltage

The TP1271/1272/1274 operational amplifiers can operate with power supply voltages from 2.7V to 36V. Each amplifier draws 0.9mA quiescent current at 36V supply voltage. The TP1271/1272/1274 is optimized for wide bandwidth low power applications. They have an industry leading high GBW to power ratio and the GBW remains nearly constant over specified temperature range.

Low Input Bias Current

The TP1271/1272/1274 is a CMOS OPA family and features very low input bias current in 3pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP1271/1272/1274 OPA's input bias current at +27°C ($\pm 3pA$, typical). It is recommended to use multi-layer PCB layout and route the OPA's $-IN$ and $+IN$ signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

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1. For Non-Inverting Gain and Unity-Gain Buffer:

- Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
- Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

- Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_{DD}/2$ or ground).
- Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

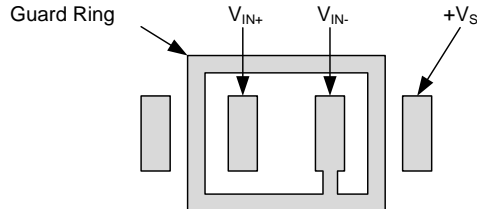


Figure 2 The Layout of Guard Ring

Ground Sensing and Rail to Rail Output

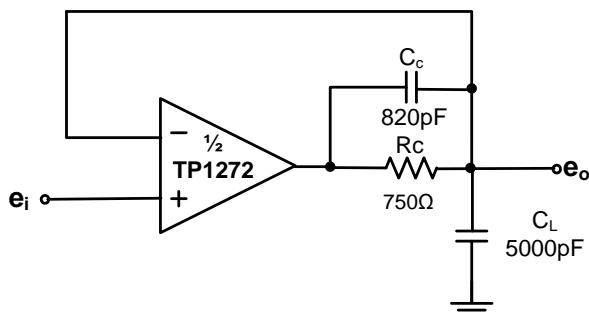
The TP1271/1272/1274 family has excellent output drive capability. It drives $2k\Omega$ load directly with good THD performance. The output stage is a rail-to-rail topology that is capable of swinging to within 50mV of either rail.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

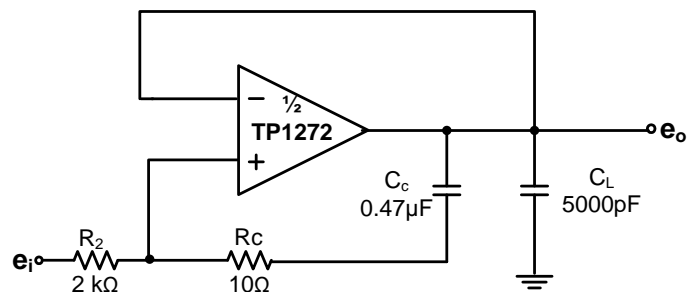
Driving Large Capacitive Load

The TP1271/1272/1274 op-amp family is designed to drive large capacitive loads. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer ($G = +1\text{V/V}$) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP1271/1272/1274 op-amp family (e.g., $> 1,000 \text{ pF}$), different compensation schemes (Figure 3) improve the feedback loop's phase margin and stability.

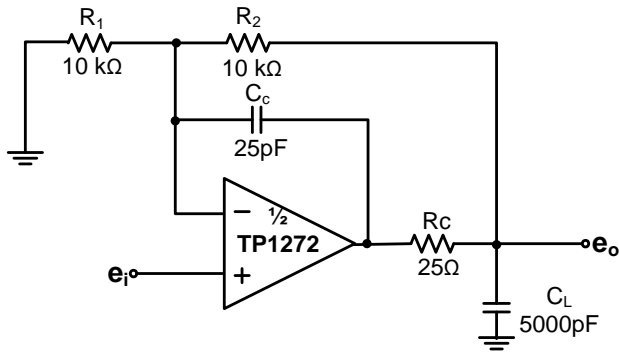


$$C_c = \sqrt{120 \times 10^{-12} C_L}$$

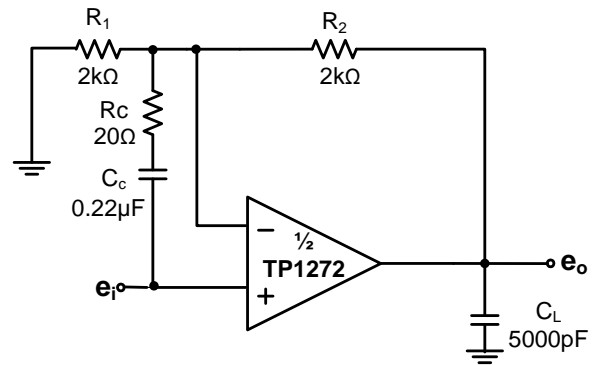


$$R_c = \frac{R_2}{4C_L \times 10^{-10} - 1} \quad C_c = \frac{C_L \times 10^3}{R_c}$$

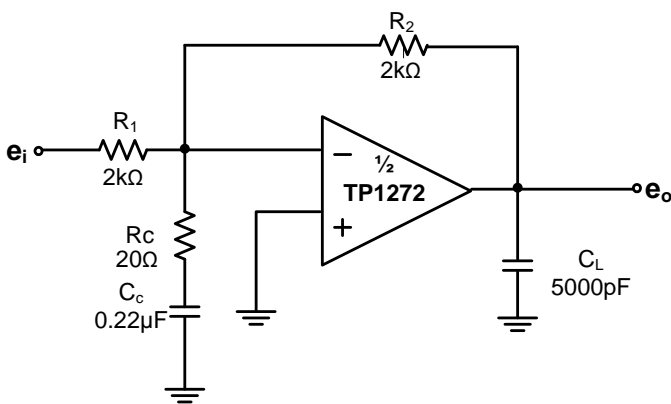
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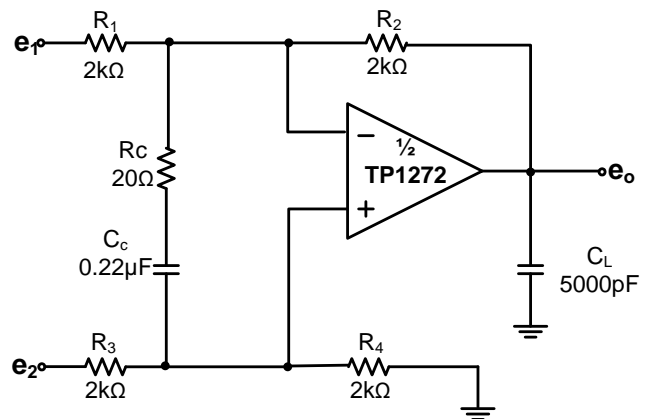
$$C_c = \frac{50}{R_2} C_L$$



$$R_c = \frac{R_2}{2C_L \times 10^{10} - (1 + R_2/R_1)} \quad C_c = \frac{C_L \times 10^3}{R_c}$$



$$R_c = \frac{R_2}{2C_L \times 10^{10} - (1 + R_2/R_1)} \quad C_c = \frac{C_L \times 10^3}{R_c}$$



$$R_c = \frac{R_2}{2C_L \times 10^{10} - (1 + R_2/R_1)} \quad C_c = \frac{C_L \times 10^3}{R_c}$$

NOTE: Design equations and component values are approximate, User adjustment is required for optimum performance.

Figure 3 Driving Large Capacitive Loads

Power Supply Layout and Bypass

The TP1271/1272/1274 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

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A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

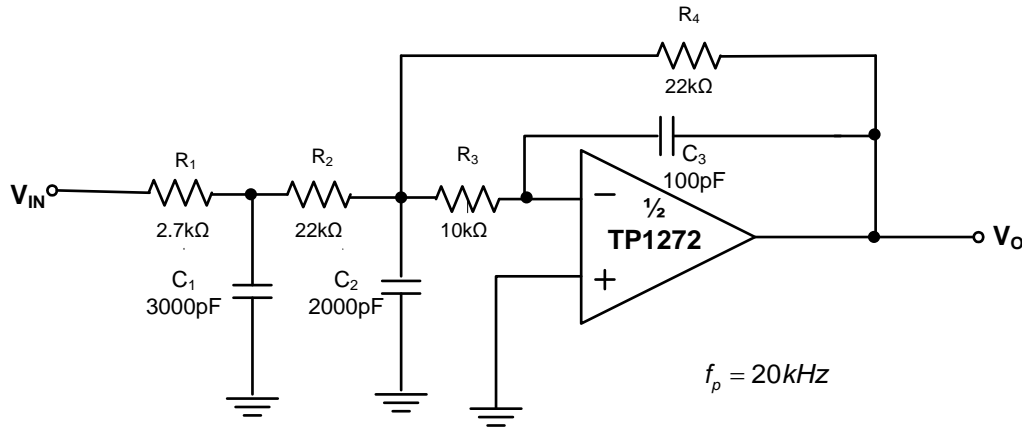


Figure 4 Three-Pole Low-Pass Filter

DAC I/V Amplifier and Low-Pass Filter

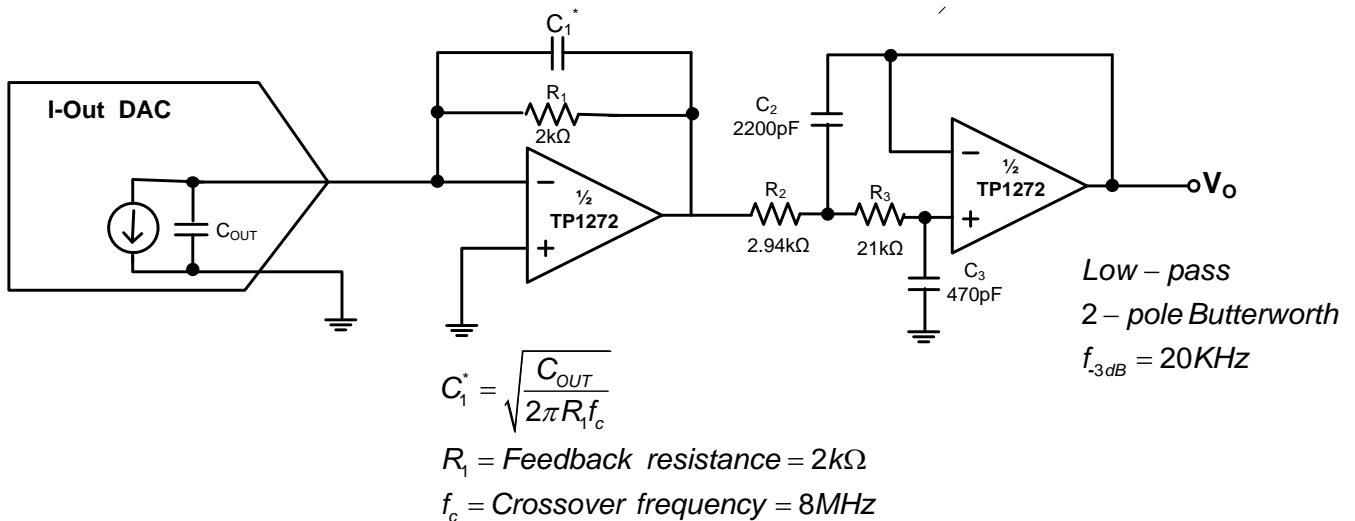
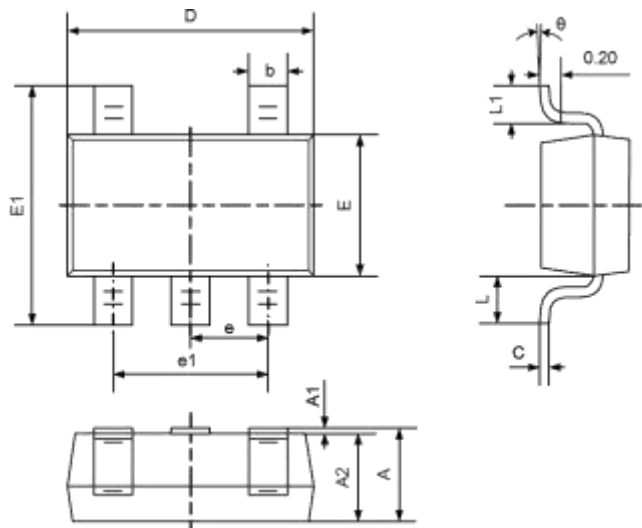


Figure 5 DAC I/V Amplifier and Low-Pass Filter

Package Outline Dimensions

SOT23-5

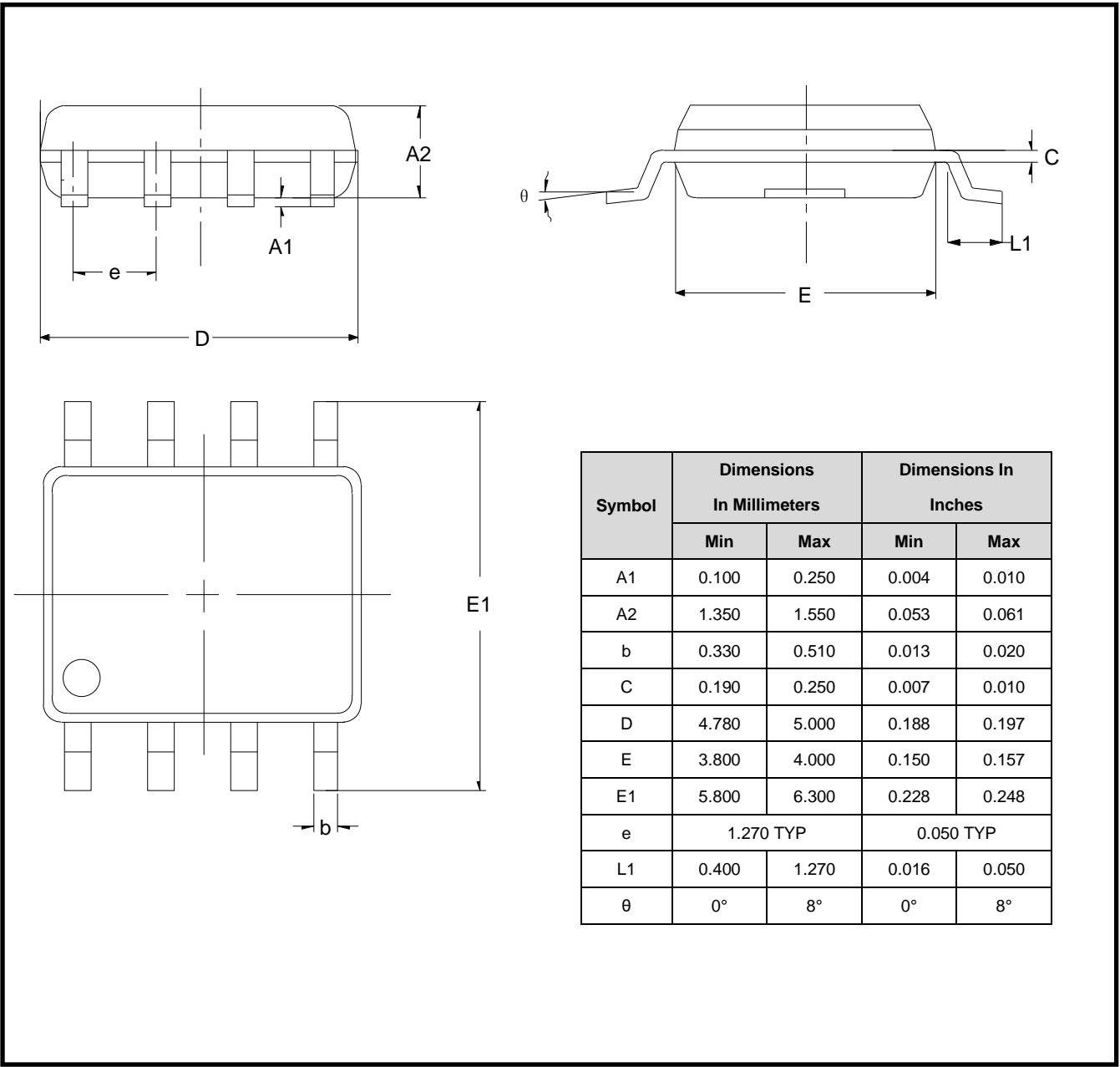


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

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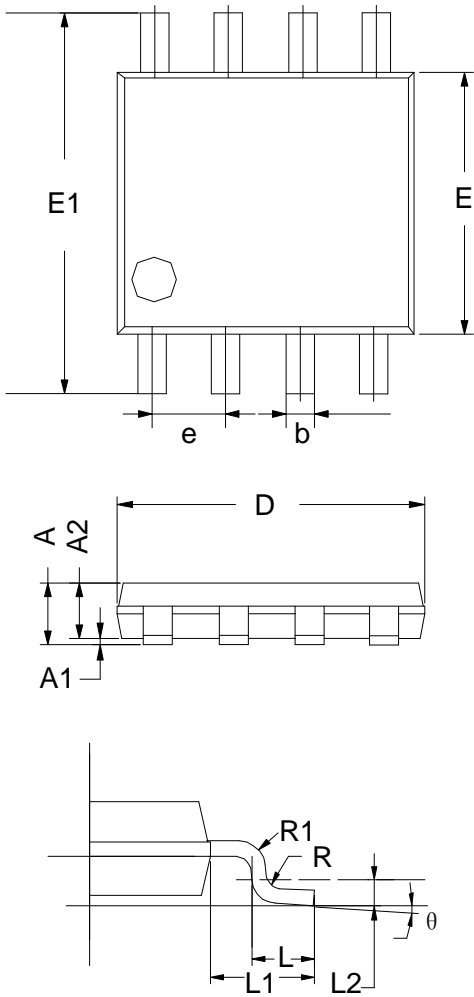
Package Outline Dimensions

SO-8 (SOIC-8)



Package Outline Dimensions

MSOP-8

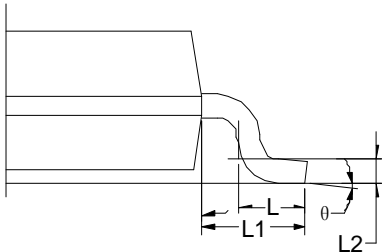
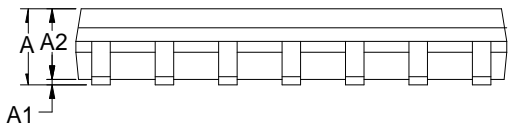
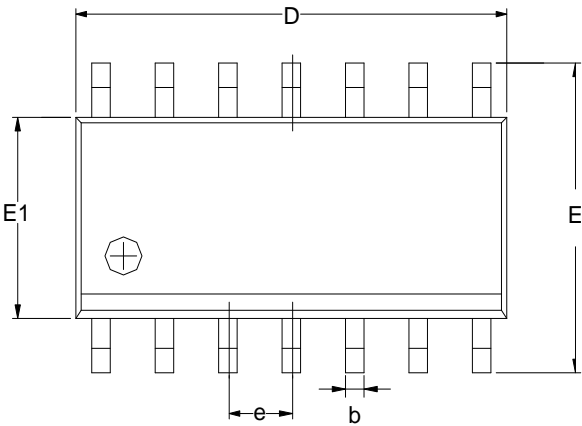


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

36V Single supply, Precision RRO Op-amps With 7MHz Bandwidth

Package Outline Dimensions

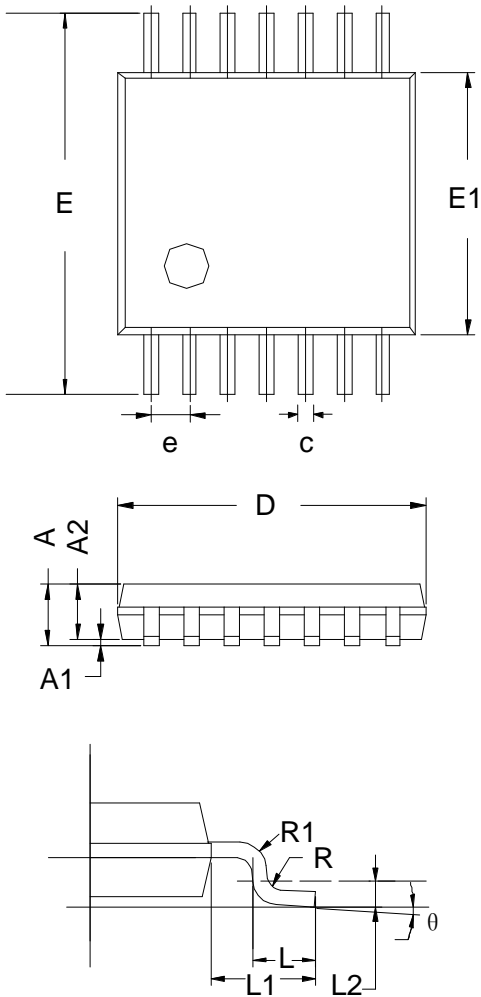
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°