Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	15	V
I_O	Ouput Peak Current	1.5	A
T_J	Junction Temperature	150	°C
T_{stg}	Storage Temperature	150	°C

Figure 3. PIN CONNECTION POWERDIP12+2+2

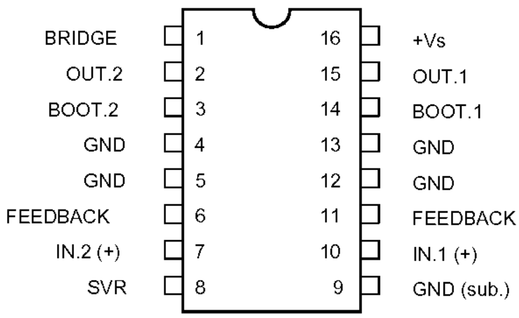


Figure 4. PIN CONNECTION SO12+4+4

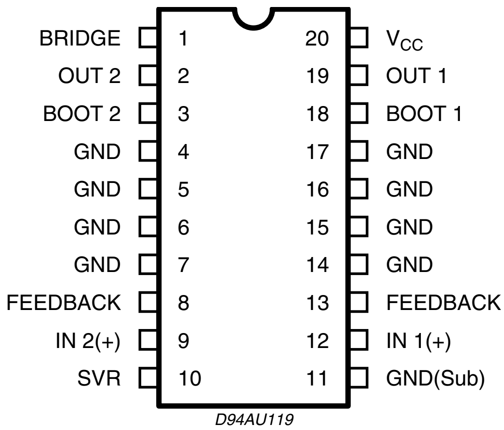


Table 3. Thermal Data

Symbol	Description		SO 12+4+4 (1)	PDIP 12+2+2 (2)	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	15	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65	60	°C/W

Note: 1. The $R_{th\ j\text{-}amb}$ is measured with 4sq cm copper area heatsink
2. The $R_{th\ j\text{-}amb}$ is measured on devices bonded on a 10 x 5 x 0.15cm glass-epoxy substrate with a 35µm thick copper surface of 5 cm^2

Table 4. Electrical Characteristcs (T_{amb} = 25°**C**, V_{CC} = 9V, Stereo unless otherwise specified**)**

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_S	Supply Voltage				3		12	V
I_Q	Quiescent Current					35	50	mA
V_O	Quiescent Output Voltage					4.5		V
A_V	Voltage Gain	Stereo			43	45	47	dB
		Bridge			49	51	53	dB
ΔA_V	Voltage Gain Difference						±1	dB
R_j	Input Impedance					30		KΩ
P_O	Output Power (d = 10%)	Stereo 8 (per channel)	9V	4Ω	1.7	2.3		W
			9V	8Ω		1.3		W
			6V	4Ω	0.7	1		W
			6V	8Ω		0.6		W
			6V	16Ω		0.25		W
			6V	32Ω		0.13		W
			3V	4Ω		0.1		W
			3V	32Ω		0.02		W
			12V	8Ω		2.4		W
		Bridge	9V	8Ω		4.7		W
			6V	4Ω		2.8		W
			6V	8Ω		1.5		W
			3V	16Ω		0.18		W
			3V	32Ω		0.06		W
d	Distortion	Vs = 9V; R_L = 4Ω	Stereo Bridge			0.3 0.5	1.5	%
SVR	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V, R_g = 0			40	46		dB
$E_{N(IN)}$	Input Noise Voltage	R_G = 0				1.5	3	mV
		R_G = 10 4Ω				3	6	mV
CT	Cross-Talk	f = 1KHz, R_g= 10KΩ			40	52		dB

Table 5.

Term. N° (PDIP)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DC VOLT (V)	0.04	4.5	8.9	0	0	0.6	0.04	8.5	0	0.04	0.6	0	0	8.9	4.5	9

Figure 5. Bridge Application (Powerdip)

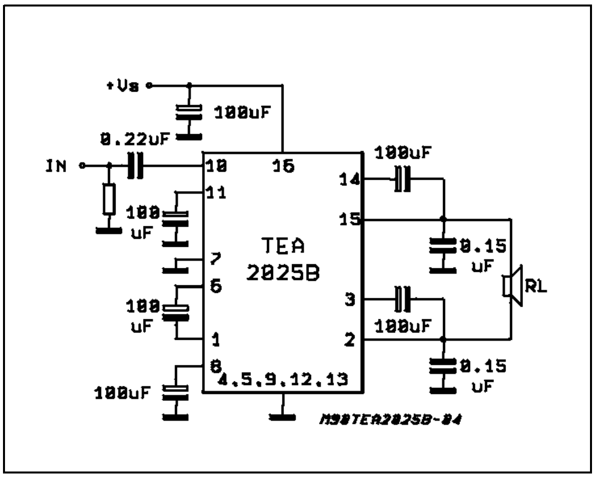


Figure 8. Output Voltage vs. Supply Voltage

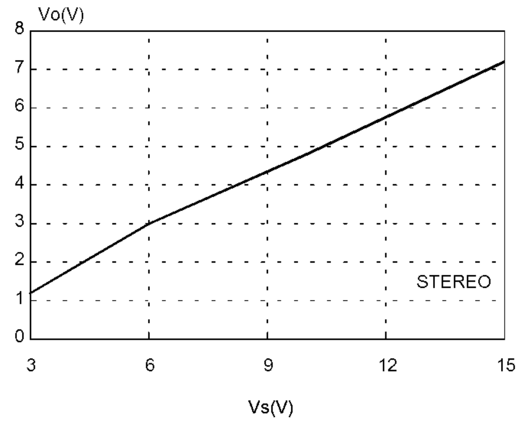


Figure 6. Stereo Application (Powerdip)

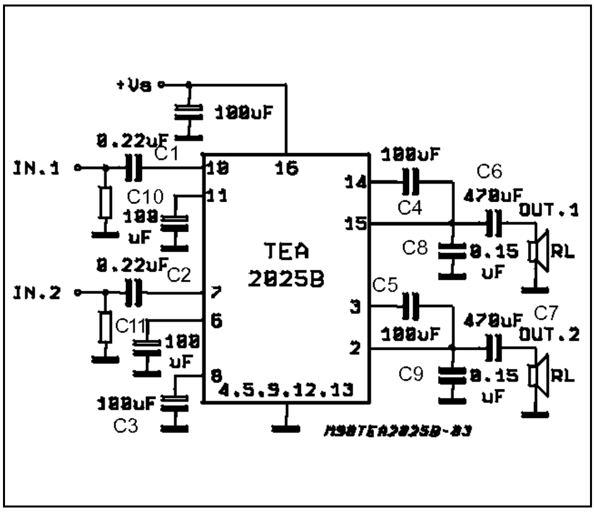


Figure 9. Output Power vs. Supply Voltage (THD = 10%, f = 1KHz)

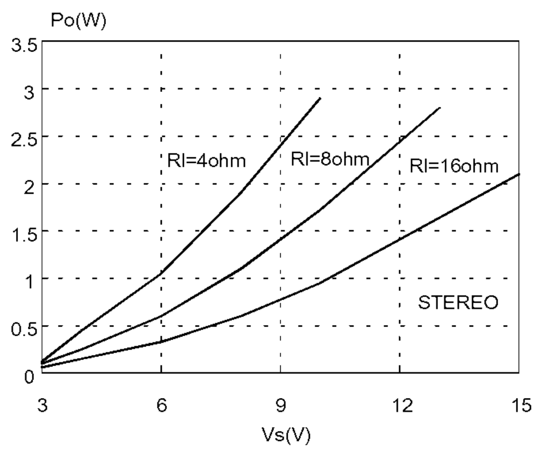


Figure 7. Supply Current vs. Supply Voltage ($R_L = 4\Omega$)

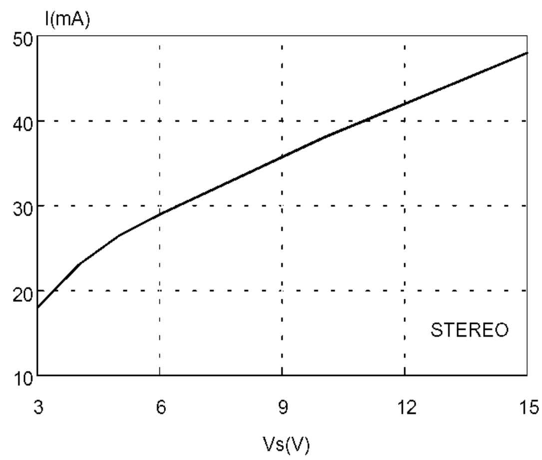
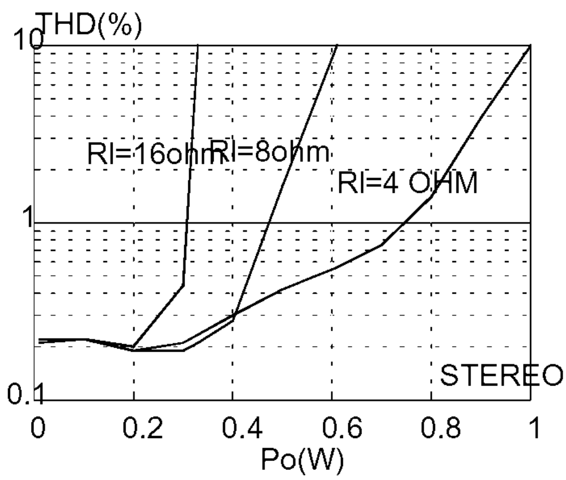


Figure 10. THD versus Output Power (f = 1KHz, V_S = 6V)



3 APPLICATION INFORMATION

3.1 Input Capacitor

Input capacitor is PNP type allowing source to be referenced to ground.

In this way no input coupling capacitor is required. However, a series capacitor (0.22 µF)to the input side can be useful in case of noise due to variable resistor contact.

3.2 Bootstrap

The bootstrap connection allows to increase the output swing.

The suggested value for the bootstrap capacitors (100µF) avoids a reduction of the output signal also at low frequencies and low supply voltages.

3.3 Voltage Gain Adjust

3.3.1 STEREO MODE

The voltage gain is determined by on-chip resistors R1 and R2 together with the external RfC1 series connected between pin 6 (11) and ground. The frequency response is given approximated

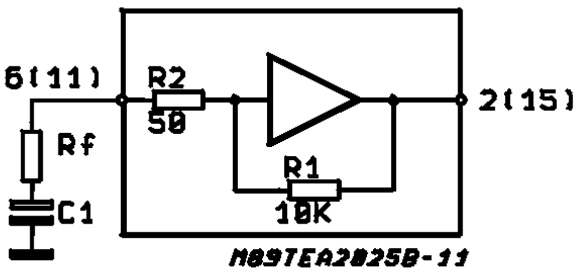
$$\frac{V_{OUT}}{V_{IN}} = \frac{R1}{Rf \div R2 + \frac{1}{JWC1}}$$

With Rf=0, C1=100 µF, the gain results 46 dB with pole at f=32 Hz.

THE purpose of Rf is to reduce the gain. It is recommended to not reduce it under 36 dB.

3.3.2 BRIDGE MODE

Figure 11.



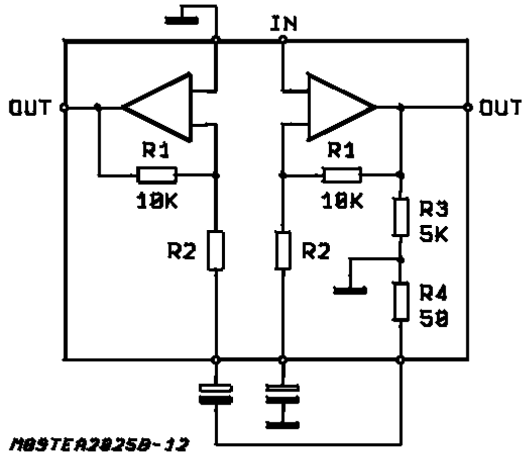
The bridge configuration is realized very easily thanks to an internal voltage divider which provides (at pin 1) the CH 1 output signal after reduction.

It is enough to connect pin 6 (inverting input of CH 2) with a capacitor to pin 1 and to connect to ground the pin 7. The total gain of the bridge is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R1}{Rf \div R2 + \frac{1}{JWC1}}\left(1 + \frac{R3}{R4}\frac{R1}{R2 + R4 + \frac{1}{JWC1}}\right)$$

and with the suggested values (C1 = C2 = 100 µF, Rf= 0) means: Gv = 52 dB with first pole at f = 32 Hz

Figure 12.



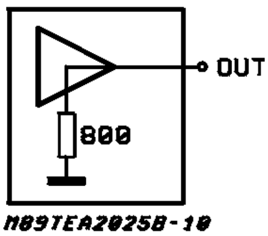
3.4 Output Capacitors.

The low cut off frequency due to output capacitor depending on the load is given by: $F_L = \frac{1}{2\Pi C_{OUT} \cdot R_L}$
with C_{OUT} 470mF and R_L = 4 ohm it means F_L = 80 Hz.

3.5 Pop Noise

Most amplifiers similar to TEA 2025B need external resistors between DC outputs and ground in order to optimize the pop on/off performance and crossover distortion.

Figure 13.



The TEA 2025B solution allows to save components because of such resistors (800 ohm)are included into the chip.

3.6 Stability

A good layout is recommended in order to avoid oscillations.

Generally the designer must pay attention on the following points:

– Short wires of components and short connections.
– No ground loops.
– Bypass of supply voltage with capacitors as nearest as possible to the supply I.C.pin. The low value(poliester)capacitors must have good temperature and frequency characteristics.
– No sockets.
  the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that PO (and

therefore Ptot) and Id are reduced.

4 APPLICATION SUGGESTION

The recommended values of the components are those shown on stereo application circuit of Fig. 6 different values can be used, the following table can help the designer.

Table 6.

COMPONENT	RECOMMENDED VALUE	PURPOSE	LARGER THAN	SMALLER THAN
C1,C2	0.22µF	INPUT DC DECOUPLING IN CASE OF SLIDER CONTACT NOISE OF VARIABLE RESISTOR		
C3	100µF	RIPPLE REJECTON		DEGRADATION OF SVR, INCREASE OF AT LOW FREQUENCY AND LOW VOLTAGE
C4,C5	100µF	BOOTSTRAP		
C6,C7	470µF	OUTPUT DC DECOUPLING		INCREASE OF LOW FREQUENCY CUTOFF
C8,C9	0.15µF	FREQUENCY STABILITY		DANGEROF OSCILLATIONS
C10, C11	100µF	INVERTING INPUT DC DECOUPLING		INCREASE OFLOW FREQUENCYCUTOFF

5 PACKAGE MECHANICAL DATA

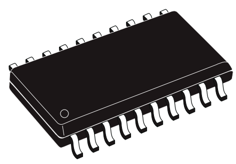
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. SO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0˚ (min.), 8˚ (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20

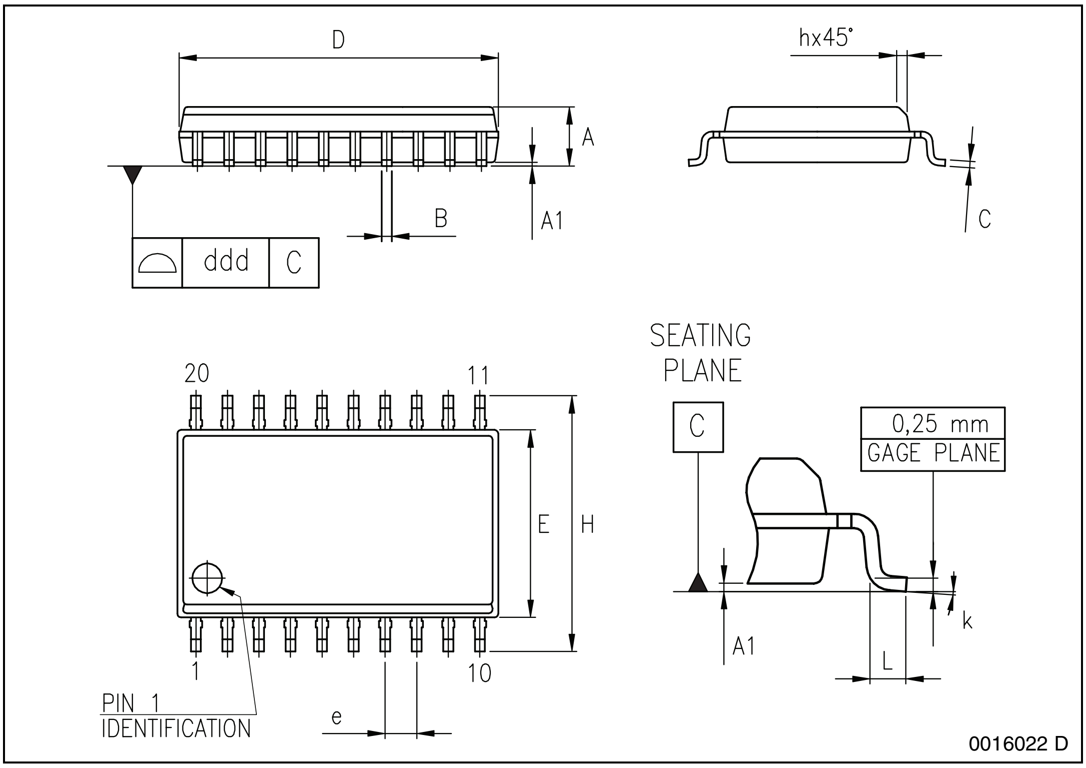
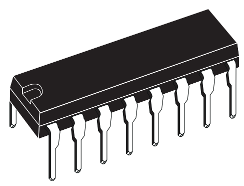


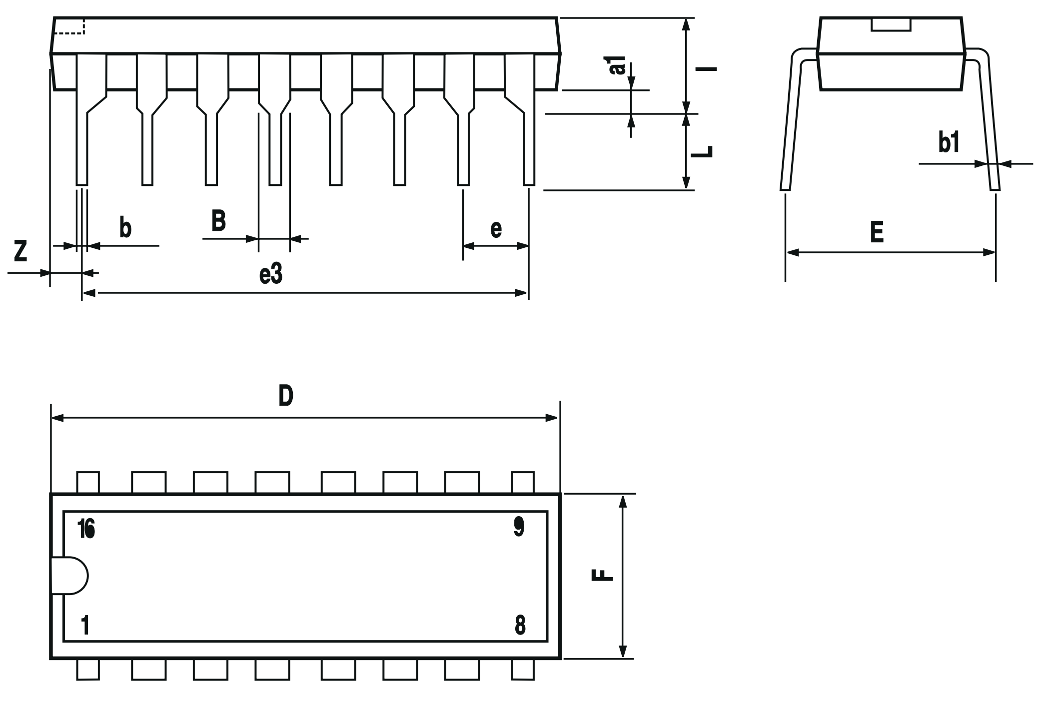
Figure 15. DIP16 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



DIP16



6 REVISION HISTORY

Table 7. Revision History

Date	Revision	Description of Changes
September 2003	2	Updates not recorded
30-Apr-2010	3	Updated title and added environmental compliance statement for package