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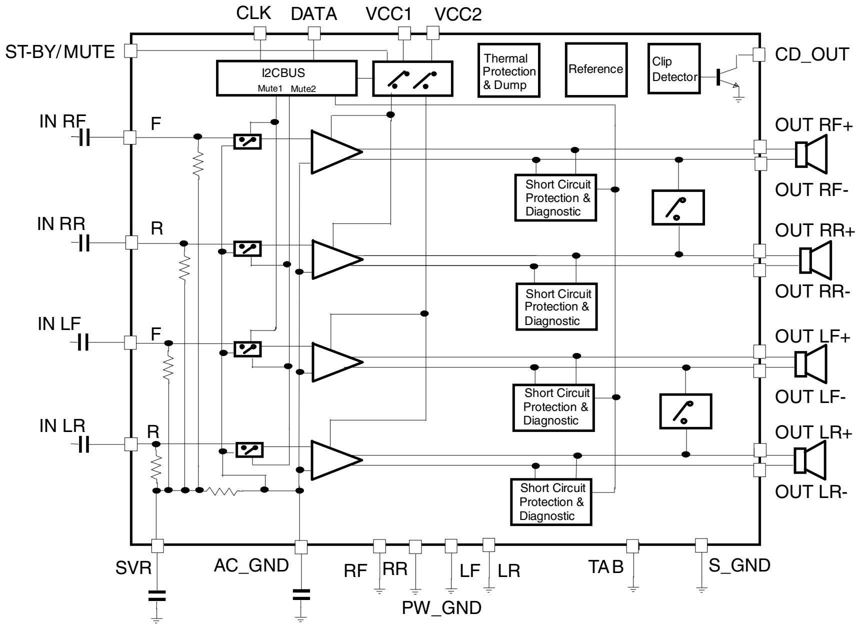
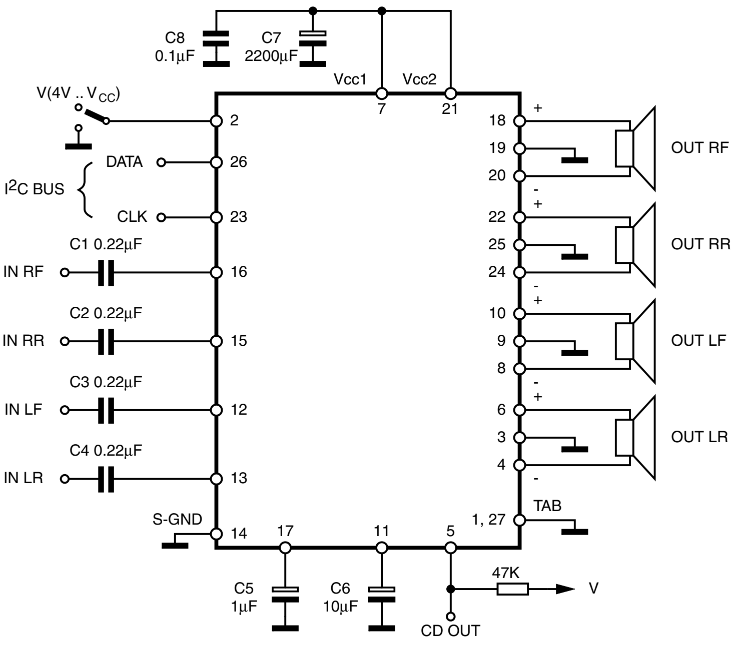
1 Block, pins connection and application diagrams

Figure 1. Block diagram



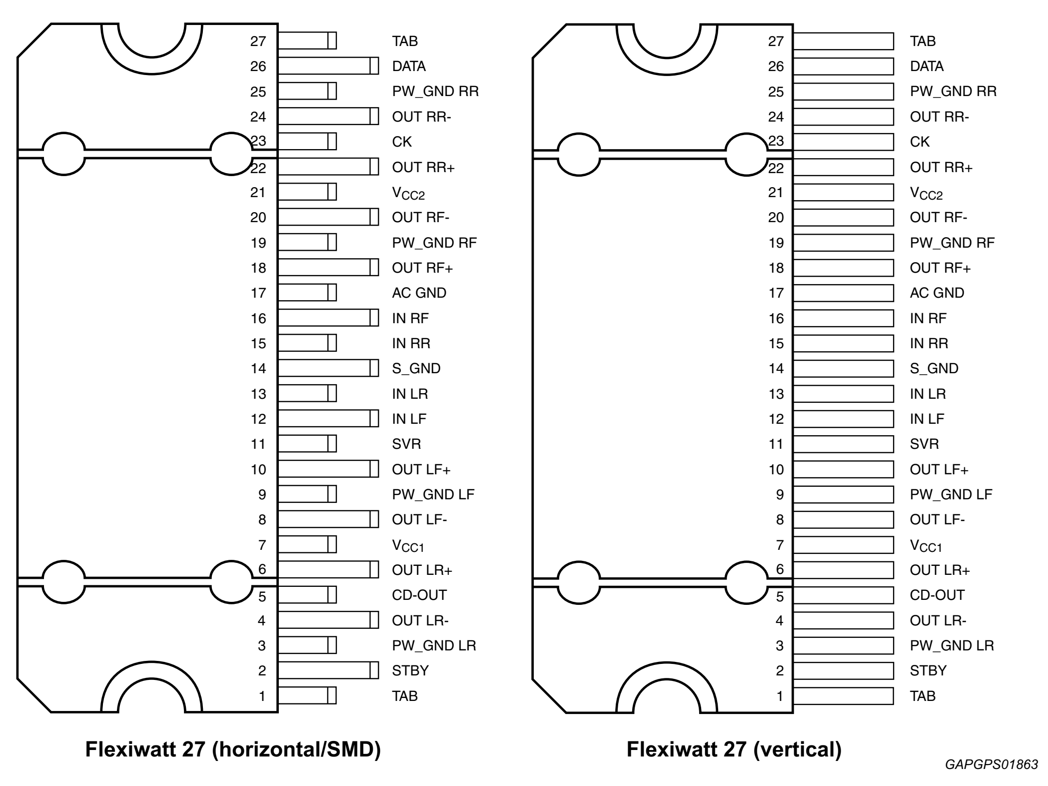
GAPGPS01861

Figure 2. Application circuit



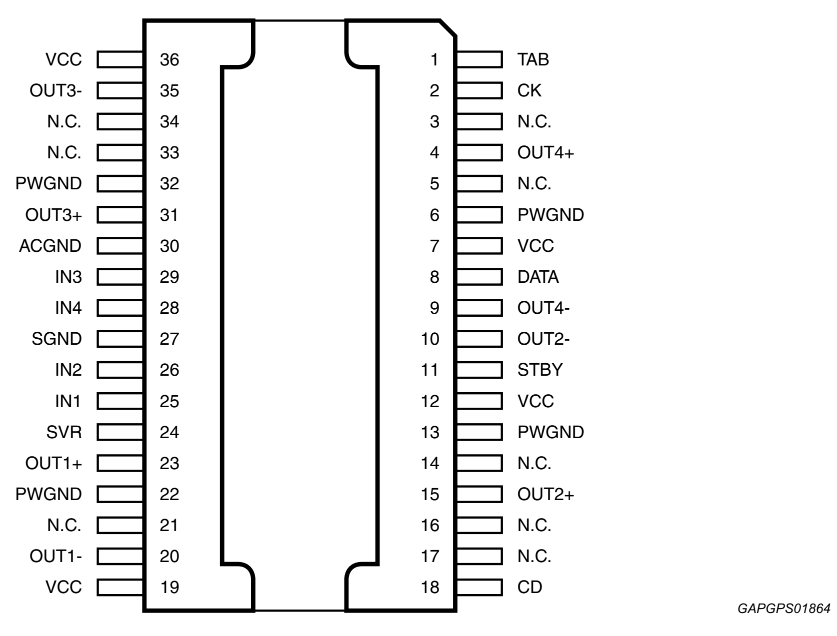
GAPGPS01862

Figure 3. Pin connections - Flexiwatt27 (Top view)



Flexiwatt 27 (horizontal/SMD) Flexiwatt 27 (vertical)

Figure 4. Pin connections - PowerSO36 (Top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{op}	Operating supply voltage	18	V
V_S	DC supply voltage	28	V
V_{peak}	Peak supply voltage (for t = 50 ms)	50	V
V_{CK}	CK pin voltage	6	V
V_{DATA}	Data pin voltage	6	V
I_O	Output peak current (not repetitive t = 100 ms)	8	A
I_O	Output peak current (repetitive f > 10 Hz)	6	A
P_{tot}	Power dissipation T_{case} = 70 °C	85	W
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter		PowerSO36	Flexiwatt 27	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	Max	1	1	°C/W

2.3 Electrical characteristics

Refer to the test circuit, V_S = 14.4 V; f = 1 kHz; R_L = 4 Ω; T_{amb}= 25 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power amplifier						
V_S	Supply voltage range	-	8	-	18	V
I_d	Total quiescent drain current	-	-	170	300	mA
P_O	Output power	Max. power (V_S = 15.2 V, square wave input (2-Vrms))	-	50	-	W
		THD = 10-%	25	28	-	W
		THD = 1-%	20	22		W
		R_L = 2-Ω; EIAJ (V_S = 13.7-V)	55	68	-	W
		R_L = 2-Ω; THD 10-%	40	50		W
		R_L = 2-Ω; THD 1-%	32	40		W
		R_L = 2-Ω; max power	60	75		W

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion	P_O = 1 to 10 W; STD MODE HE MODE; P_O = 1.5 W HE MODE; P_O = 8 W	-	0.015 0.01 0.1	0.1 0.1 0.5	% % %
		P_O = 1-10 W, f = 10kHz; STD mode	-	0.15	0.5	%
		R_L = 2 Ω; HE MODE; P_O = 3W	-	0.02	0.5	%
		G_V = 12 dB; STD mode V_O = 0.1 to 5 V_{RMS}	-	0.015	0.1	%
C_T	Cross talk	f = 1 kHz to 10 kHz, R_g = 600 Ω	50	60	-	dB
R_{IN}	Input impedance	-	60	100	130	kΩ
G_{V1}	Voltage gain 1 (default)	-	25	26	27	dB
ΔG_{V1}	Voltage gain match 1	-	-1		1	dB
G_{V2}	Voltage gain 2	-	11	12	13	dB
ΔG_{V2}	Voltage gain match 2	-	-1	-	1	dB
E_{IN1}	Output noise voltage 1	R_g = 600 Ω; filter 20 Hz to 22 kHz	-	35	-	µV
E_{IN2}	Output noise voltage 2	R_g = 600 Ω; G_V = 12 dB filter 20 Hz to 22 kHz	-	11	-	µV
SVR	Supply voltage rejection	f = 100 Hz to 10 kHz; V_r = 1 Vpk; R_g = 600 Ω	50	70	-	dB
BW	Power bandwidth	-	100	-	-	kHz
A_{SB}	Standby attenuation	-	90	110		dB
I_{SB}	Standby current	$V_{standby}$ = 0	-	1	10	µA
A_M	Mute attenuation	-	80	100		dB
V_{OS}	Offset voltage	Mute & Play	-60	0	60	mV
V_{AM}	Min. supply mute threshold	-	7	7.5	8	V
T_{ON}	Turn on delay	D2/D1 (IB1) 0 to 1	-	5	20	ms
T_{OFF}	Turn off delay	D2/D1 (IB1) 1 to 0	-	5	20	ms
V_{SBY}	Standby/mute pin for standby	-	0	-	1.5	V
V_{MU}	Standby/mute pin for mute	-	3.5	-	5	V
CMRR	Input CMRR	V_{CM} = 1 Vpk-pk; Rg = 0 Ω	-	55	-	dB
V_{OP}	Standby/mute pin for operating		7	-	V_S	V
I_{MU}	Standby/mute pin current	$V_{standby/mute}$ = 8.5 V	-	20	40	µA
		$V_{standby/mute}$ < 1.5 V	-	0	5	µA
CD_{LK}	Clip det. high leakage current	CD off / V_{CD} = 6 V	-	0	5	µA
CD_{SAT}	Clip det. saturation voltage	CD on; I_{CD} = 1 mA	-	-	300	mV

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CD_{THD}	Clip det. THD level	D0 (IB1) = 1	5	10	15	%
		D0 (IB1) = 0	1	2	3	%
Turn on diagnostics 1 (Power amplifier mode)						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	Power amplifier in standby	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the output is considered in short circuit to VS)		Vs -1.2	-	-	V
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).		1.8	-	Vs -1.8	V
Lsc	Shorted load det.		-	-	0.5	Ω
Lop	Open load det.		130	-	-	Ω
Lnop	Normal load det.		1.5	-	70	Ω
Turn on diagnosticS 2 (Line driver mode)						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	Power amplifier in standby	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the output is considered in short circuit to VS)	-	Vs -1.2	-	-	V
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).	-	1.8	-	Vs -1.8	V
Lsc	Shorted load det.	-		-	1.5	Ω
Lop	Open load det.	-	400	-	-	Ω
Lnop	Normal load det.	-	4.5	-	200	Ω
Permanent diagnostics 2 (Power amplifier mode or line driver mode)						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	Power amplifier in mute or play, one or more short circuits protection activated	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the output is considered in short circuit to Vs)		Vs -1.2	-	-	V
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).		1.8	-	Vs -1.8	V
L_{SC}	Shorted load det.	Power amplifier mode	-	-	0.5	Ω
		Line driver mode	-	-	1.5	Ω

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Offset detection	Power amplifier in play, STD mode AC input signals = 0	±1.5	±2	±2.5	V
I_{NL}	Normal load current detection	$V_O < (V_S\text{-}5)pk$	500	-	-	mA
I_{OL}	Open load current detection		-	-	250	mA
I^2C bus interface						
S_{CL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	1.5	V
V_{IH}	Input high voltage	-	2.3	-	-	V

2.4 Electrical characteristics curves

Figure 5. Quiescent current vs. supply voltage

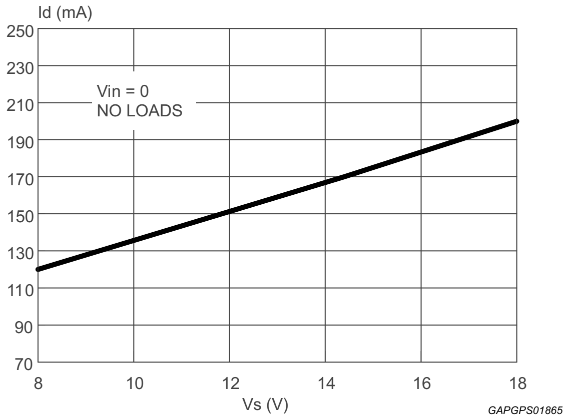


Figure 6. Output power vs. supply voltage (4 Ω)

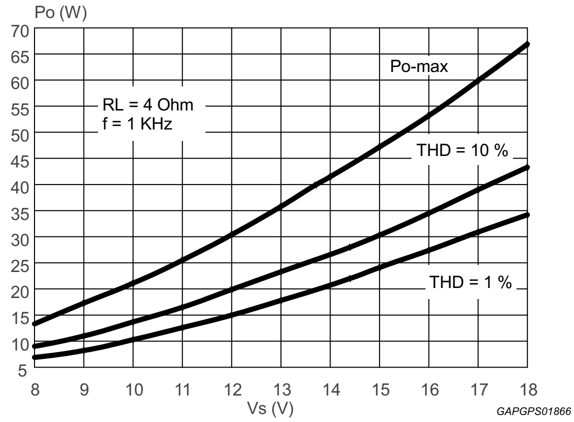


Figure 7. Output power vs. supply voltage (2 Ω)

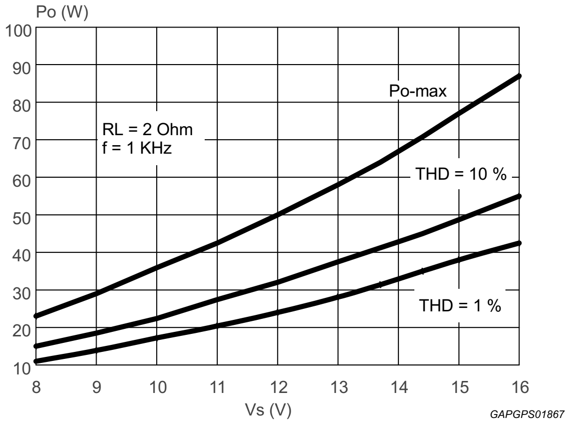


Figure 8. Distortion vs. output power (4 Ω, STD)

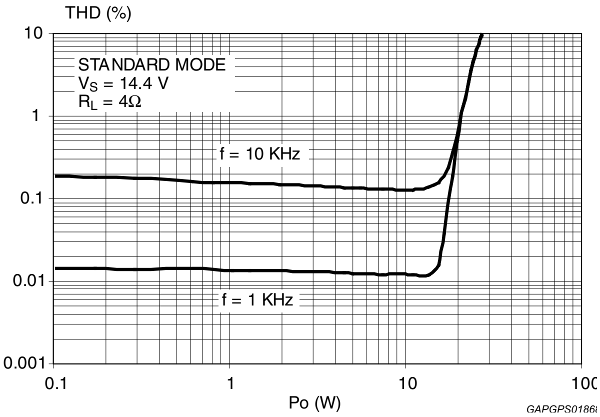


Figure 9. Distortion vs. output power (4 Ω, HI-EFF)

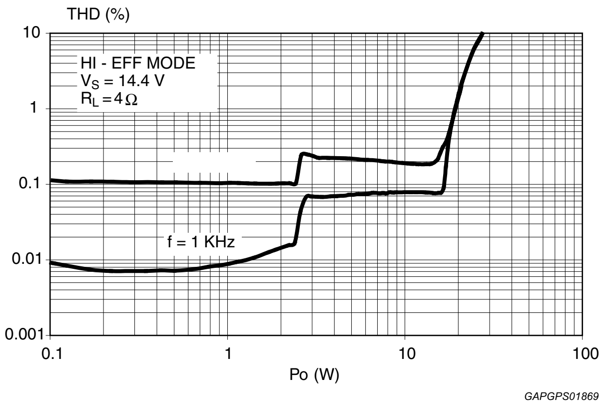


Figure 10. Distortion vs. output power (2 Ω, STD)

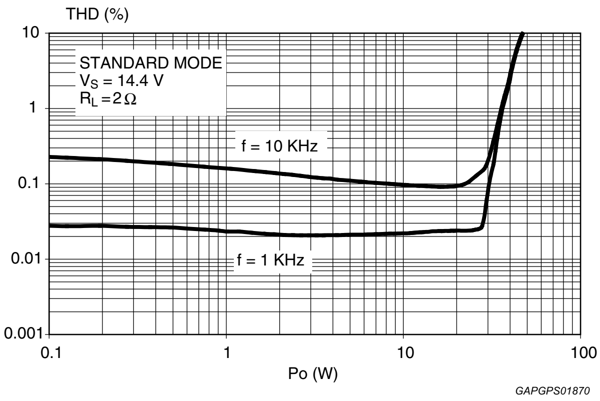


Figure 11. Distortion vs. frequency (4 Ω)

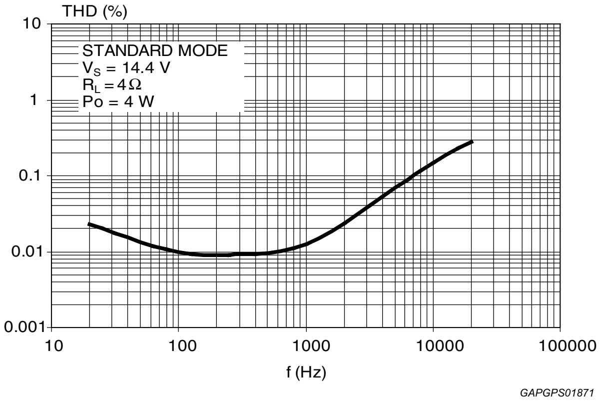


Figure 12. Distortion vs. frequency (2 Ω)

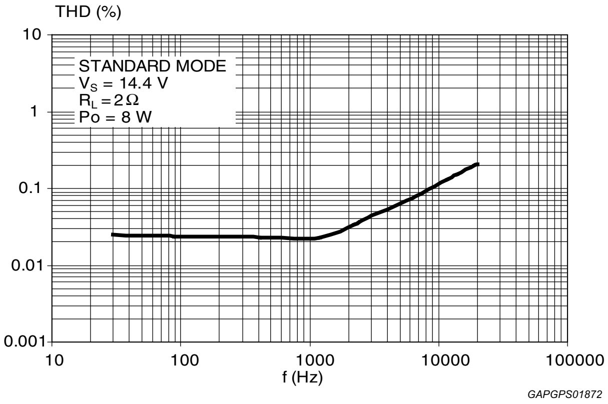


Figure 13. Crosstalk vs. frequency

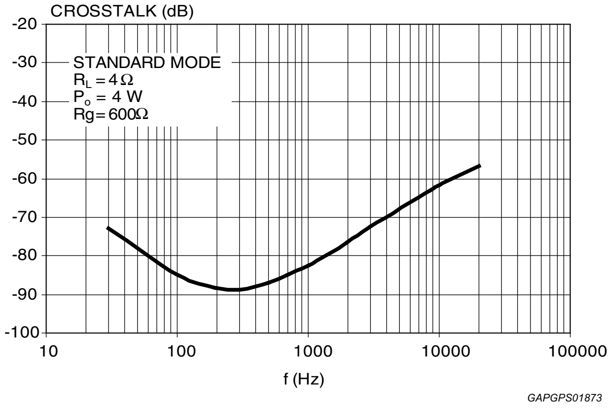


Figure 14. Supply voltage rejection vs. frequency

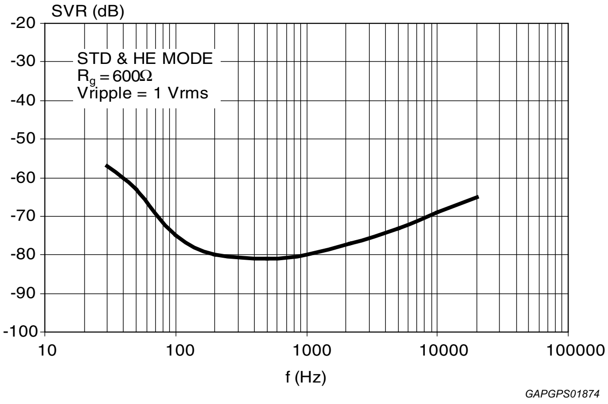


Figure 15. Power dissipation and efficiency vs. output power (4 Ω, STD, SINE)

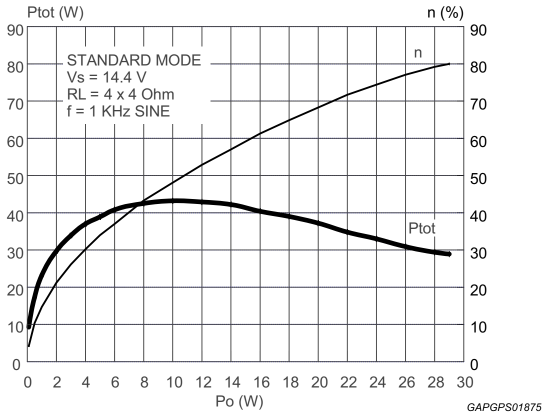


Figure 16. Power dissipation and efficiency vs. output power (4 Ω, HI-EFF, SINE)

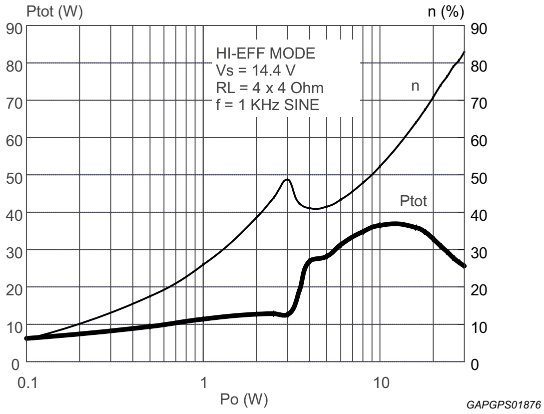


Figure 17. Power dissipation vs. average output power (audio program simulation, 4 Ω)

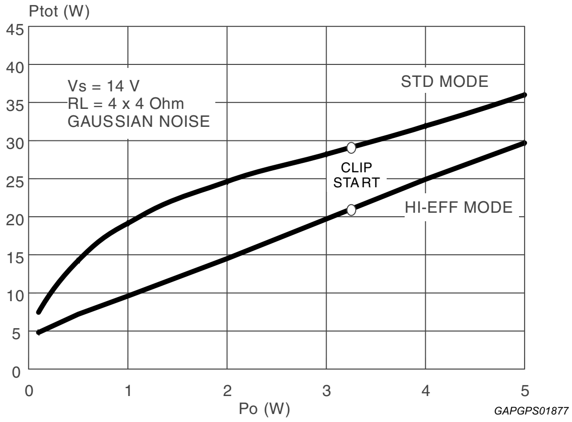
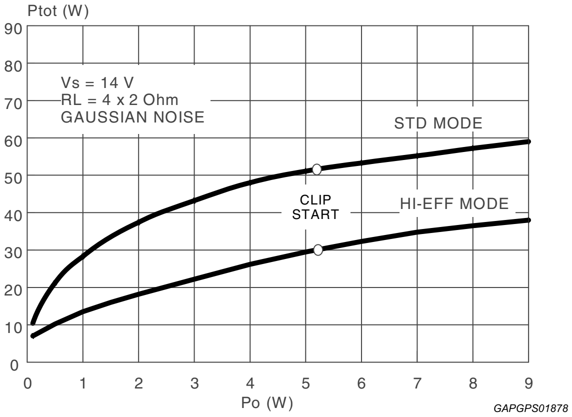


Figure 18. Power dissipation vs. average output power (audio program simulation, 2 Ω)



3 Diagnostics functional description

3.1 Turn-on diagnostic

It is activated at the turn-on (standby out) under I^2C bus request. Detectable output faults are:

- Short to GND
- Short to Vs
- Short across the speaker
- Open speaker

To verify if any of the above misconnections are in place, a subsonic (inaudible) current pulse (*Figure 19*) is internally generated, sent through the speaker(s) and sunk back.The Turn On diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I^2C reading).

If the "standby out" and "diagnostic enable" commands are both given through a single programming step, the pulse takes place first (power stage still in standby mode, low, outputs = high impedance).

Afterwards, when the amplifier is biased, the PERMANENT diagnostic takes place. The previous Turn On state is kept until a short appears at the outputs.

Figure 19. Turn-on diagnostic: working principle

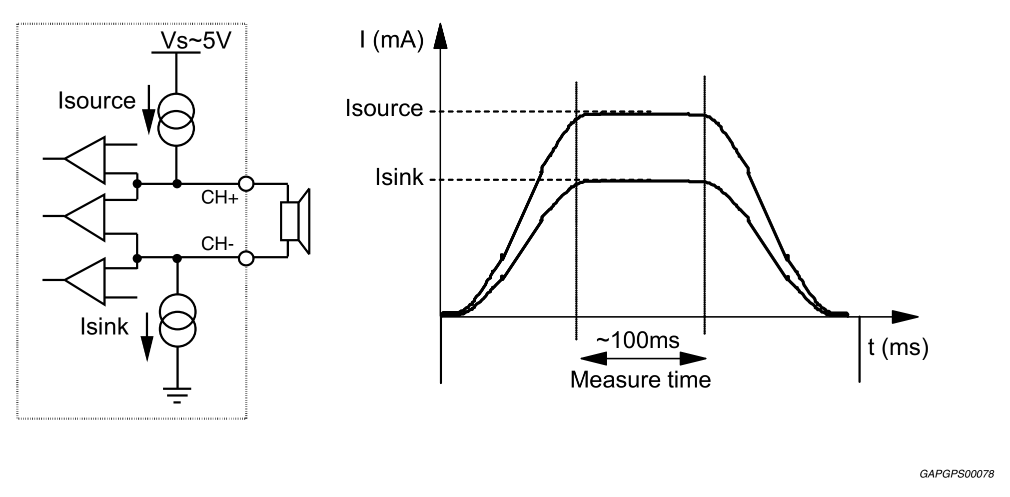


Figure 20 and *21* show SVR and OUTPUT waveforms at the turn-on (standby out) with and without TURN-ON DIAGNOSTIC.

Figure 20. SVR and output behavior (case 1: without turn-on diagnostic)

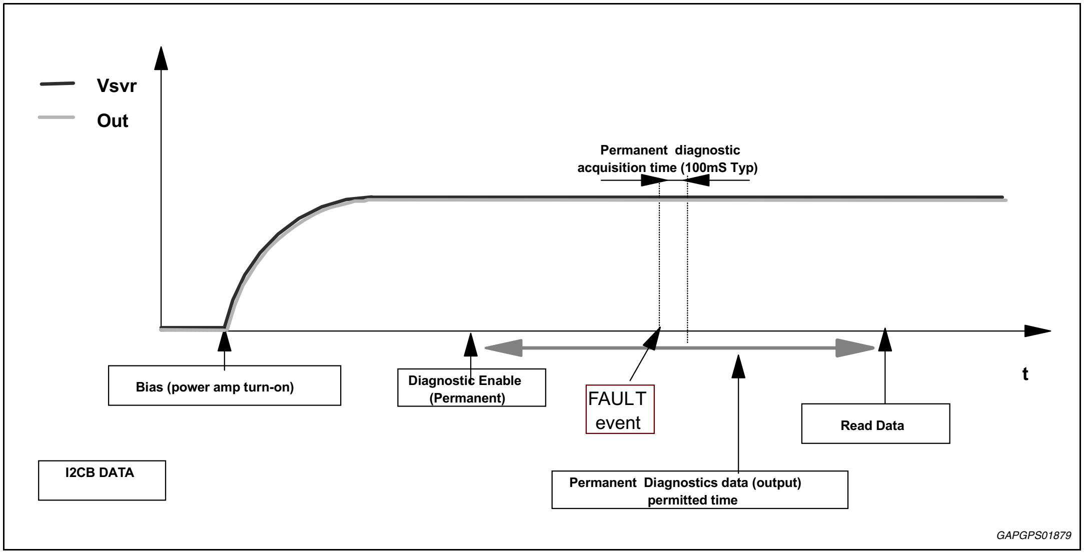
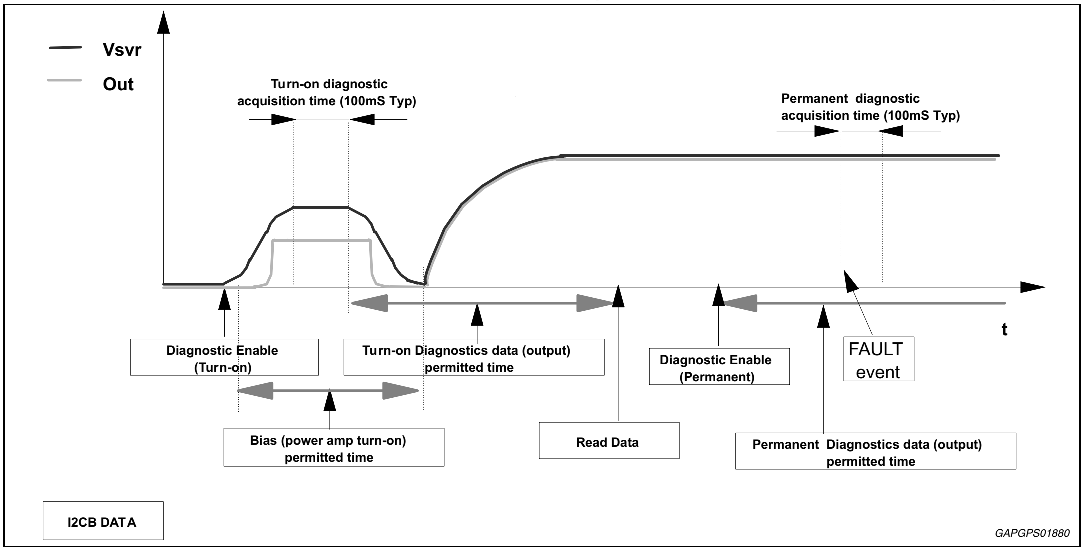
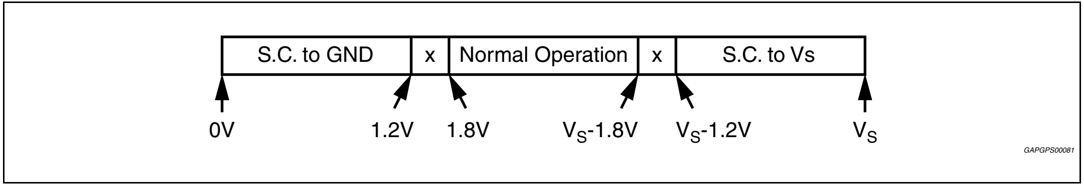


Figure 21. SVR and output pin behavior (case 2: with turn-on diagnostic)



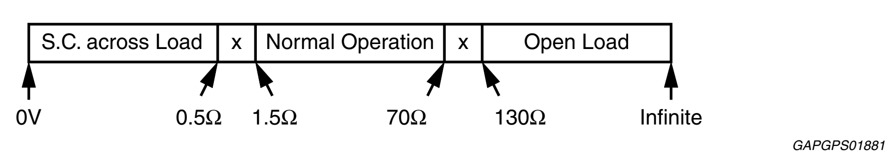
The information related to the outputs status is read and memorized at the end of the current pulse top. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for SHORT TO GND / V_S the fault-detection thresholds remain unchanged from 26 dB to 12 dB gain setting. They are as follows:TDA7563A

Figure 22. Thresholds for short to GND/V_S



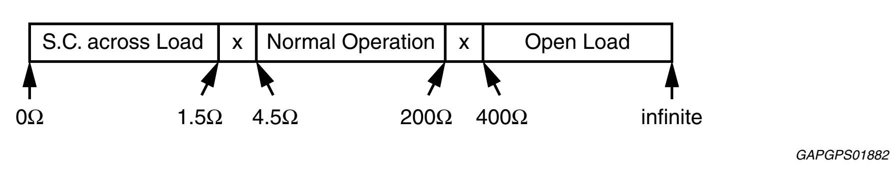
Concerning SHORT ACROSS THE SPEAKER / OPEN SPEAKER, the threshold varies from 26 dB to 12 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 26 dB gain are as follows:

Figure 23. Thresholds for short across the speaker/open speaker



If the Line-Driver mode (Gv= 12 dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:

Figure 24. Thresholds for line-drivers



3.2 Permanent diagnostics

Detectable conventional faults are:

- Short to GND
- Short to Vs
- Short across the speaker

The following additional features are provided:

- Output offset detection

The TDA7563A has 2 operating statuses:

1. RESTART mode. The diagnostic is not enabled. Each audio channel operates independently from each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms (*Figure 25*). Restart takes place when the overload is removed.
2. DIAGNOSTIC mode. It is enabled via I^2C bus and self activates if an output overload (such to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as follows (*Figure 26*):
   - To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns back active.
   - Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.
   - After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated

by an I^{2}C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.

– To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (over half a second is recommended).

Figure 25. Restart timing without diagnostic enable (permanent) - Each 1ms time, a sampling of the fault is done

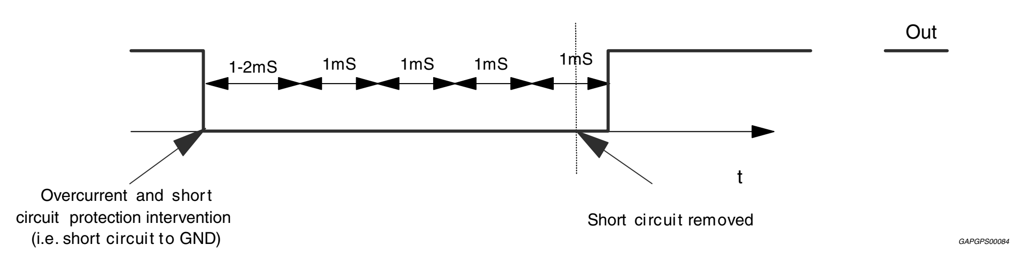
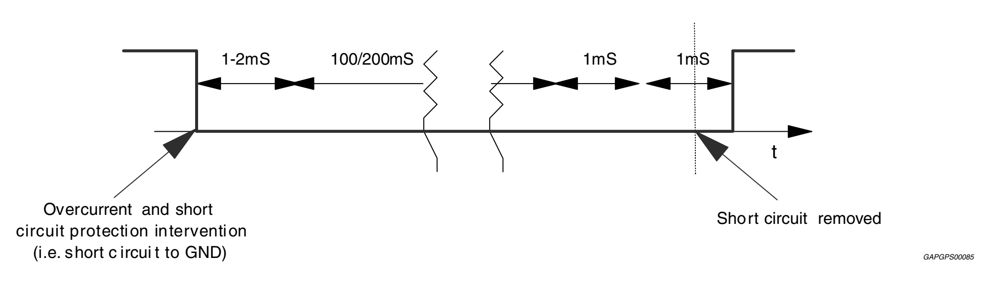


Figure 26. Restart timing with diagnostic enable (permanent)



4 Output DC offset detection

Any DC output offset exceeding ± 2 V are signalled out. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating.

This diagnostic has to be performed with low-level output AC signal (or Vin = 0).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

- START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1
- STOP = Actual reading operation

Excess offset is signalled out if it is persistent for all the assigned testing time. This feature is disabled if any overload leading to activation of the short-circuit protection occurs in the process.

4.1 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitively (AC) coupled loads.
This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance). The diagnostic decision is made according to peak output current thresholds, as follows:

Iout > 500 mApk = NORMAL STATUS

Iout < 250 mApk = OPEN TWEETER

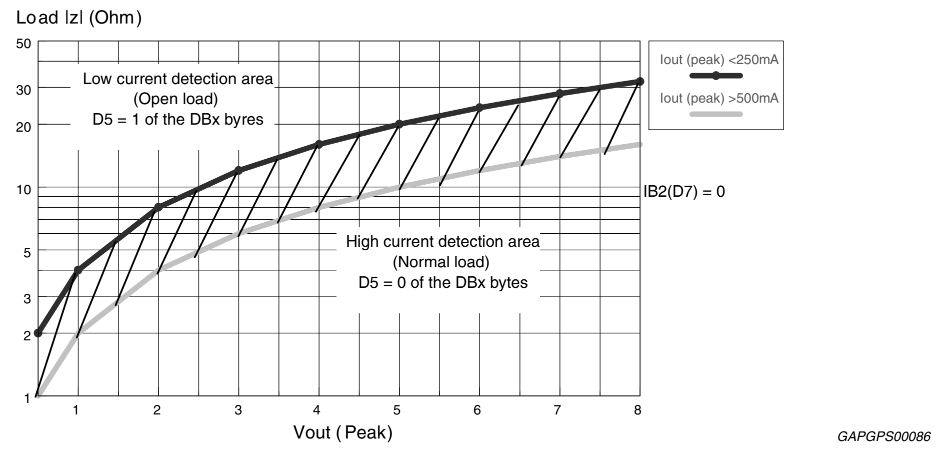
To correctly implement this feature, it is necessary to briefly provide a signal tone (with the amplifier in "play") whose frequency and magnitude are such as to determine an output current higher than 500 mApk in normal conditions and lower than 250 mApk should the parallel tweeter be missing.

The test has to last for a minimum number of 3 sine cycles starting from the activation of the AC diagnostic function IB2<D2>) up to the I^2C reading of the results (measuring period). To confirm presence of tweeter, it is necessary to find at least 3 current pulses over 500 mA over all the measuring period, else an "open tweeter" message will be issued.

The frequency / magnitude setting of the test tone depends on the impedance characteristics of each specific speaker being used, with or without the tweeter connected (to be calculated case by case). High-frequency tones (> 10 kHz) or even ultrasonic signals are recommended for their negligible acoustic impact and also to maximize the impedance module's ratio between with tweeter-on and tweeter-off.

Figure 27 shows the Load Impedance as a function of the peak output voltage and the relevant diagnostic fields.
This feature is disabled if any overload leading to activation of the short-circuit protection occurs in the process.

Figure 27. Current detection: Load impedance |Z| vs. output peak voltage



4.2 Multiple faults

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of I^2C reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4 ohm speaker unconnected is considered as double fault.

Table 5. Double fault table for turn on diagnostic

	S. GND (so)	S. GND (sk)	S. Vs	S. Across L.	Open L.
S. GND (so)	S. GND	S. GND	S. Vs + S. GND	S. GND	S. GND
S. GND (sk)	/	S. GND	S. Vs	S. GND	Open L. (*)
S. Vs	/	/	S. Vs	S. Vs	S. Vs
S. Across L.	/	/	/	S. Across L.	N.A.
Open L.	/	/	/	/	Open L. (*)

S. GND (so) / S. GND (sk) in the above table make a distinction according to which of the 2 outputs is shorted to ground (test-current source side= so, test-current sink side = sk). More precisely, in Channels LF and RR, so = CH+, sk = CH-; in Channels LR and RF, so = CH-, sk = CH+.

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*), which is not among the recognizable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive Car Radio Turn on).

4.3 Faults availability

All the results coming from I^2C bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out.

To guarantee always resident functions, every kind of diagnostic cycles (Turn on, Permanent, Offset) will be reactivated after any I^2C reading operation. So, when the micro reads the I^2C, a new cycle will be able to start, but the read data will come from the previous diag. cycle (i.e. The device is in Turn On state, with a short to Gnd, then the short is removed and micro reads I^2C. The short to Gnd is still present in bytes, because it is the result of the previous cycle. If another I^2C reading operation occurs, the bytes do not show the short). In general to observe a change in Diagnostic bytes, two I^2C reading operations are necessary.

5 Thermal protection

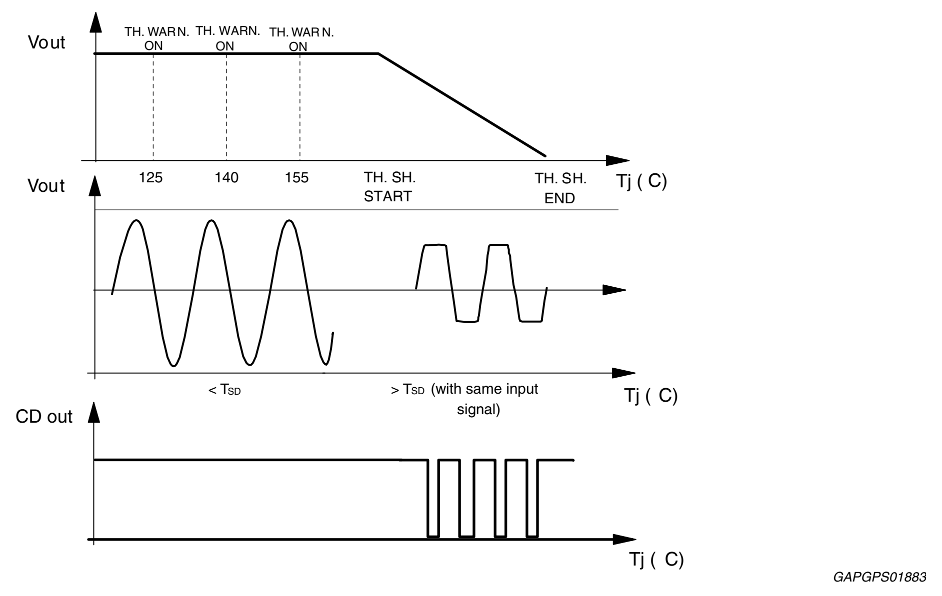
Thermal protection is implemented through thermal foldback (*Figure 28*).

Thermal foldback begins limiting the audio input to the amplifier stage as the junction temperatures rise above the normal operating range. This effectively limits the output power capability of the device thus reducing the temperature to acceptable levels without totally interrupting the operation of the device.

The output power will decrease to the point at which thermal equilibrium is reached. Thermal equilibrium will be reached when the reduction in output power reduces the dissipated power such that the die temperature falls below the thermal foldback threshold. Should the device cool, the audio level will increase until a new thermal equilibrium is reached or the amplifier reaches full power. Thermal foldback will reduce the audio output level in a linear manner.

Three Thermal warnings are available through the I^{2}C bus data.

Figure 28. Thermal foldback diagram



6 Fast muting

The muting time can be shortened to less than 1.5 ms by setting (IB2) D5 = 1. This option can be useful in transient battery situations (i.e. during car engine cranking) to quickly turnoff the amplifier for avoiding any audible effects caused by noise/transients being injected by preamp stages. The bit must be set back to “0” shortly after the mute transition.

7 I^2C bus

7.1 I^2C programming/reading sequences

A correct turn on/off sequence respectful of the diagnostic timings and producing no audible noises could be as follows (after battery connection):

TURN-ON: PIN2 > 7V --- 10ms --- (STANDBY OUT + DIAG ENABLE) --- 500 ms (min) --- MUTING OUT

TURN-OFF: MUTING IN --- 20 ms --- (DIAG DISABLE + STANDBY IN) --- 10ms --- PIN2 = 0

Car Radio Installation: PIN2 > 7V --- 10ms DIAG ENABLE (write) --- 200 ms --- I^2C read (repeat until All faults disappear).

OFFSET TEST: Device in Play (no signal) -- OFFSET ENABLE - 30ms - I^2C reading (repeat I^2C reading until high-offset message disappears).

7.2 I^2C bus interface

Data transmission from microprocessor to the TDA7563A and vice versa takes place through the 2 wires I^2C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

7.3 Data validity

As shown by *Figure 29*, the data on the SDA line must be stable during the high period of the clock.
The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

7.4 Start and stop conditions

As shown by *Figure 30* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.
The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

7.5 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

7.6 Acknowledge

The transmitter(*) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 31*). The receiver(**) has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

(*) Transmitter
- master (µP) when it writes an address to the TDA7563A
- slave (TDA7563A) when the µP reads a data byte from TDA7563A

(**) Receiver
- slave (TDA7563A) when the µP writes an address to the TDA7563A
- master (µP) when it reads a data byte from TDA7563A

Figure 29. Data validity on the I²C bus

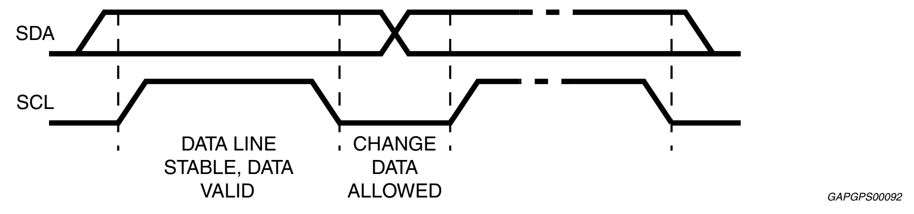


Figure 30. Timing diagram on the I²C bus

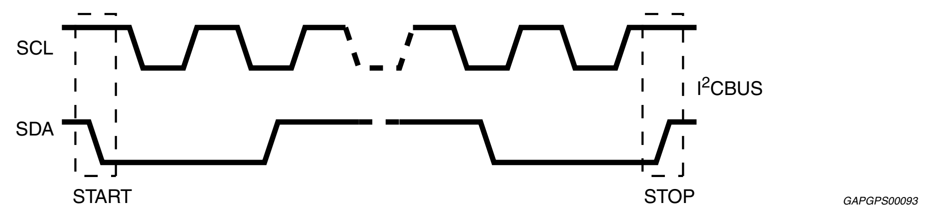
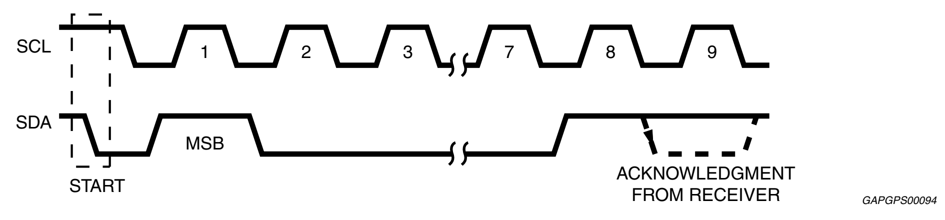


Figure 31. Timing acknowledge clock pulse



8 Software specifications

All the functions of the TDA7563A are activated by I^{2}C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from µP to TDA7563A) or read instruction (from TDA7563A to µP).

Chip address

D7							D0	
1	1	0	1	1	0	0	X	D8 Hex

X = 0 Write to device
X = 1 Read from device

If R/W = 0, the µP sends 2 "Instruction Bytes": IB1 and IB2.

Table 6. IB1

Bit	Instruction decoding bit
D7	0
D6	Diagnostic enable (D6 = 1) Diagnostic defeat (D6 = 0)
D5	Offset Detection enable (D5 = 1) Offset Detection defeat (D5 = 0)
D4	Front Channel Gain = 26dB (D4 = 0) Gain = 12dB (D4 = 1)
D3	Rear Channel Gain = 26dB (D3 = 0) Gain = 12dB (D3 = 1)
D2	Mute front channels (D2 = 0) Unmute front channels (D2 = 1)
D1	Mute rear channels (D1 = 0) Unmute rear channels (D1 = 1)
D0	CD 2% (D0 = 0) CD 10% (D0 = 1)

Table 7. IB2

Bit	Instruction decoding bit
D7	0
D6	0
D5	Normal muting time (D5 = 0) Fast muting time (D5 = 1)
D4	Standby on - Amplifier not working - (D4 = 0) Standby off - Amplifier working - (D4 = 1)
D3	Power amplifier mode diagnostic (D3 = 0) Line driver mode diagnostic (D3 = 1)
D2	Current Detection Diagnostic Enabled (D2 =1) Current Detection Diagnostic Defeat (D2 =0)
D1	Right Channel Power amplifier working in standard mode (D1 = 0) Power amplifier working in high efficiency mode (D1 = 1)
D0	Left Channel Power amplifier working in standard mode (D0 = 0) Power amplifier working in high efficiency mode (D0 = 1)

If R/W = 1, the TDA7563A sends 4 "Diagnostics Bytes" to µP: DB1, DB2, DB3 and DB4.

Table 8. DB1

Bit	Instruction decoding bit
D7	Thermal warning active (D7 = 1), T_J = 155°C
D6	Diag. cycle not activated or not terminated (D6 = 0) Diag. cycle terminated (D6 = 1)
D5	Channel LF Current Detection Output peak current <250mA - Output load (D5 = 1) Output peak current >500mA - Output load (D5 = 0)
D4	Channel LF Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel LF Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel LF Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Offset diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel LF No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel LF No short to GND (D1 = 0) Short to GND (D1 = 1)

Table 9. DB2

Bit	Instruction decoding bit
D7	Offset detection not activated (D7 = 0) Offset detection activated (D7 = 1)
D6	0
D5	Channel LR Current Detection Output peak current <250mA - Output load (D5 = 1) Output peak current >500mA - Output load (D5 = 0)
D4	Channel LR Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel LR Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel LR Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel LR No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel LR No short to GND (D1 = 0) Short to GND (D1 = 1)

Table 10. DB3

Bit	Instruction decoding bit
D7	Standby status (= IB2 - D4)
D6	Diagnostic status (= IB1 - D6)
D5	Channel RF Current Detection Output peak current <250mA - Output load (D5 = 1) Output peak current >500mA - Output load (D5 = 0)
D4	Channel RF Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel RF Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel RF Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel RF No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel RF No short to GND (D1 = 0) Short to GND (D1 = 1)

Table 11. DB4

Bit	Instruction decoding bit
D7	Thermal warning 2 active (D7 = 1), T_J = 140°C
D6	Thermal warning 3 active (D6 = 1), T_J = 120°C
D5	Channel RR Current Detection Output peak current <250mA - Output load (D5 = 1) Output peak current >500mA - Output load (D5 = 0)
D4	Channel RR Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel R R Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel RR Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel RR No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel RR No short to GND (D1 = 0) Short to GND (D1 = 1)

9 Examples of bytes sequence

1 - Turn-On diagnostic - Write operation

Start	Address byte with D0 = 0	ACK	IB1 with D6 = 1	ACK	IB2	ACK	STOP

2 - Turn-On diagnostic - Read operation

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP

- The delay from 1 to 2 can be selected by software, starting from 1ms

3a - Turn-On of the power amplifier with 26dB gain, mute on, diagnostic defeat, CD = 2%.

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X0000000		XXX1XX11		

3b - Turn-Off of the power amplifier

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X0XXXXXX		XXX0XXXX		

4 - Offset detection procedure enable

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX1XX11X		XXX1XXXX		

5 - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2, DB3, DB4).

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP

- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 4 to 5 can be selected by software, starting from 1ms

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

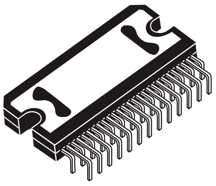
ECOPACK® is an ST trademark.

Figure 32. Flexiwatt27 (horizontal) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D		2.00			0.079	
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.75	1.00	1.25	0.0295	0.040	0.0492
G1	25.70	26.00	26.30	1.0118	1.023	1.0354
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	21.64	22.04	22.44	0.852	0.868	0.883
L1	10.15	10.5	10.85	0.40	0.413	0.427
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5	5.15	5.45	5.85	0.203	0.214	0.23
L6	1.80	1.95	2.10	0.070	0.077	0.083
M	2.75	3.00	3.50	0.108	0.118	0.138
M1		4.73			0.186	
M2		5.61			0.220	
N		2.20			0.086	
P	3.20	3.50	3.80	0.126	0.138	0.15
R		1.70			0.067	
R1		0.50			0.02	
R2		0.30			0.12	
R3		1.25			0.049	
R4		0.50			0.02	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusionincluded

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (Horizontal)

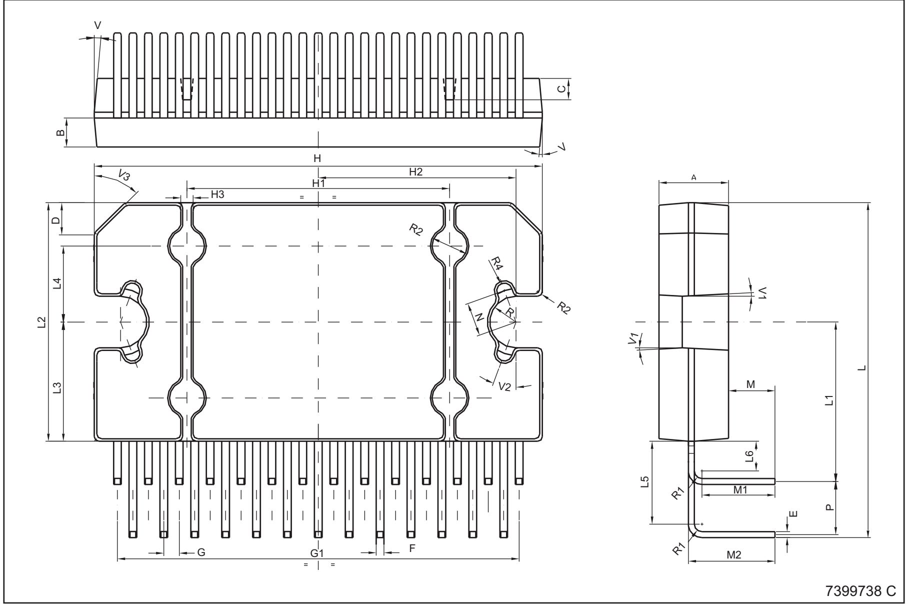
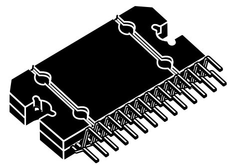


Figure 33. Flexiwatt27 (vertical) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusion included.

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)

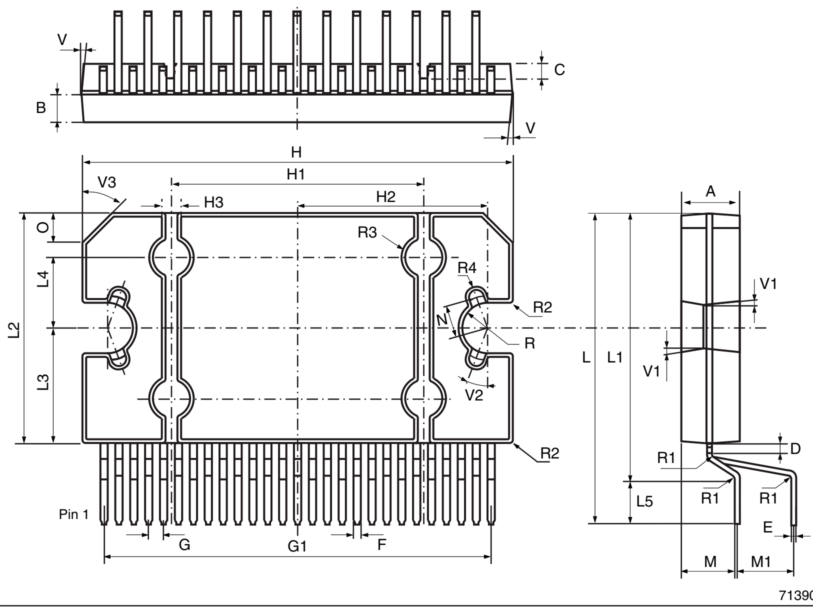


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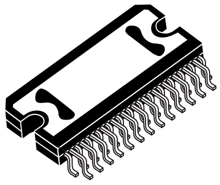
Figure 34. Flexiwatt27 (SMD) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.1752	0.1772	0.1831
B	2.12	2.22	2.32	0.0835	0.0874	0.0913
C		1.40			0.0551	
D		2.00			0.0787	
E	0.36	0.40	0.44	0.0142	0.0157	0.0173
F(**)	0.47	0.51	0.57	0.0185	0.0201	0.0224
G(*)	0.75	1.00	1.25	0.0295	0.0394	0.0492
G1	25.70	26.00	26.30	1.0118	1.0236	1.0354
G2(*)	1.75	2.00	2.25	0.0689	0.0787	0.0886
H(**)	28.85	29.23	29.40	1.1358	1.1508	1.1575
H1		17.00			0.6693	
H2		12.80			0.5039	
H3		0.80			0.0315	
L(**)	15.50	15.70	15.90	0.6102	0.6181	0.6260
L1	7.70	7.85	7.95	0.3031	0.3091	0.3130
L2	14.00	14.20	14.40	0.5512	0.5591	0.5669
L3	11.80	12.00	12.20	0.4646	0.4724	0.4803
L4	1.30	1.48	1.66	0.0512	0.0583	0.0654
L5	2.42	2.50	2.58	0.0953	0.0984	0.1016
L6	0.42	0.50	0.58	0.0165	0.0197	0.0228
M		1.50			0.0591	
N		2.20			0.0866	
N1	1.30	1.48	1.66	0.0512	0.0583	0.0654
N2(*)	2.73	2.83	2.93	0.1075	0.1114	0.1154
P(*)	4.73	4.83	4.93	0.1862	0.1902	0.1941
R		1.70			0.0669	
R1		0.30			0.0118	
R2	0.35	0.40	0.45	0.0138	0.0157	0.0177
R3	0.35	0.40	0.45	0.0138	0.0157	0.0177
R4		0.50			0.0197	
T(*)	-0.08		0.10	-0.0031		0.0039
aaa(*)		0.1			0.0039	
V		45°			45°	
V1		3°			3°	
V2	3°	5°	7°	3°	5°	7°
V3	12°	15°	18°	12°	15°	18°
V4		5°			5°	
V5		20°			20°	

(*) Golden parameters
(**) – Dimension “F” doesn’t include dam-bar protrusion.
– Dimensions "H” and “L" include mold flash or protrusions.

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (SMD)

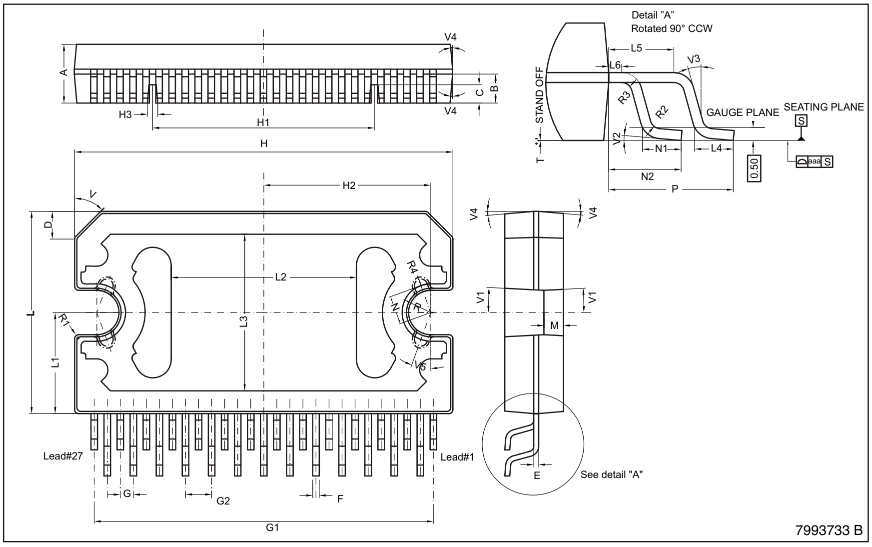
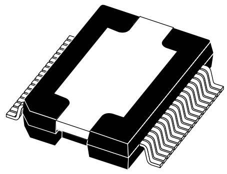


Figure 35. PowerSO36 (slug up) mechanical data and package dimensions

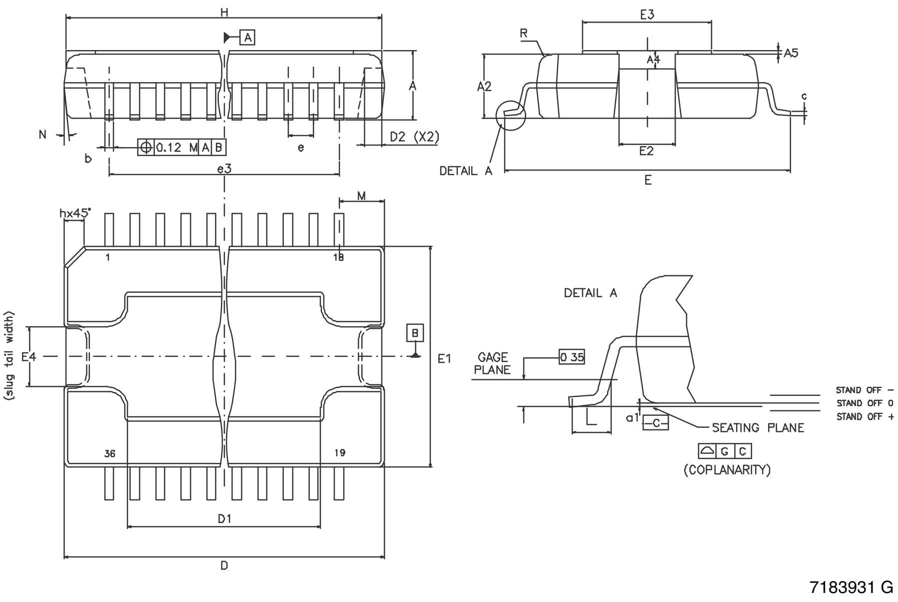
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.270	-	3.410	0.1287	-	0.1343
A2	3.100	-	3.180	0.1220	-	0.1252
A4	0.800	-	1.000	0.0315	-	0.0394
A5	-	0.200	-	-	0.0079	-
a1	0.030	-	-0.040	0.0012	-	-0.0016
b	0.220	-	0.380	0.0087	-	0.0150
c	0.230	-	0.320	0.0091	-	0.0126
D	15.800	-	16.000	0.6220	-	0.6299
D1	9.400	-	9.800	0.3701	-	0.3858
D2	-	1.000	-	-	0.0394	-
E	13.900	-	14.500	0.5472	-	0.5709
E1	10.900	-	11.100	0.4291	-	0.4370
E2	-	-	2.900	-	-	0.1142
E3	5.800	-	6.200	0.2283	-	0.2441
E4	2.900	-	3.200	0.1142	-	0.1260
e	-	0.650	-	-	0.0256	-
e3	-	11.050	-	-	0.4350	-
G	0	-	0.075	0	-	0.0031
H	15.500	-	15.900	0.6102	-	0.6260
h	-	-	1.100	-	-	0.0433
L	0.800	-	1.100	0.0315	-	0.0433
N	-	-	10°	-	-	10°
s	-	-	8°	-	-	8°

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006").
(2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DAT A



PowerSO36 (SLUG UP)



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11 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Feb-2008	1	Initial release.
10-Aug-2012	2	Updated *Section 10: Package information*.
11-Dec-2012	3	Corrected Pin 27 name of the Flexiwatt 27 (vertical) on the *Figure 3 on page 6*. Corrected typeset error of the "a1" dimension on the *Figure 35: PowerSO36 (slug up) mechanical data and package dimensions on page 33*.
17-Sep-2013	4	Updated Disclaimer.
03-Dec-2013	5	Changed “Title” in cover page.

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