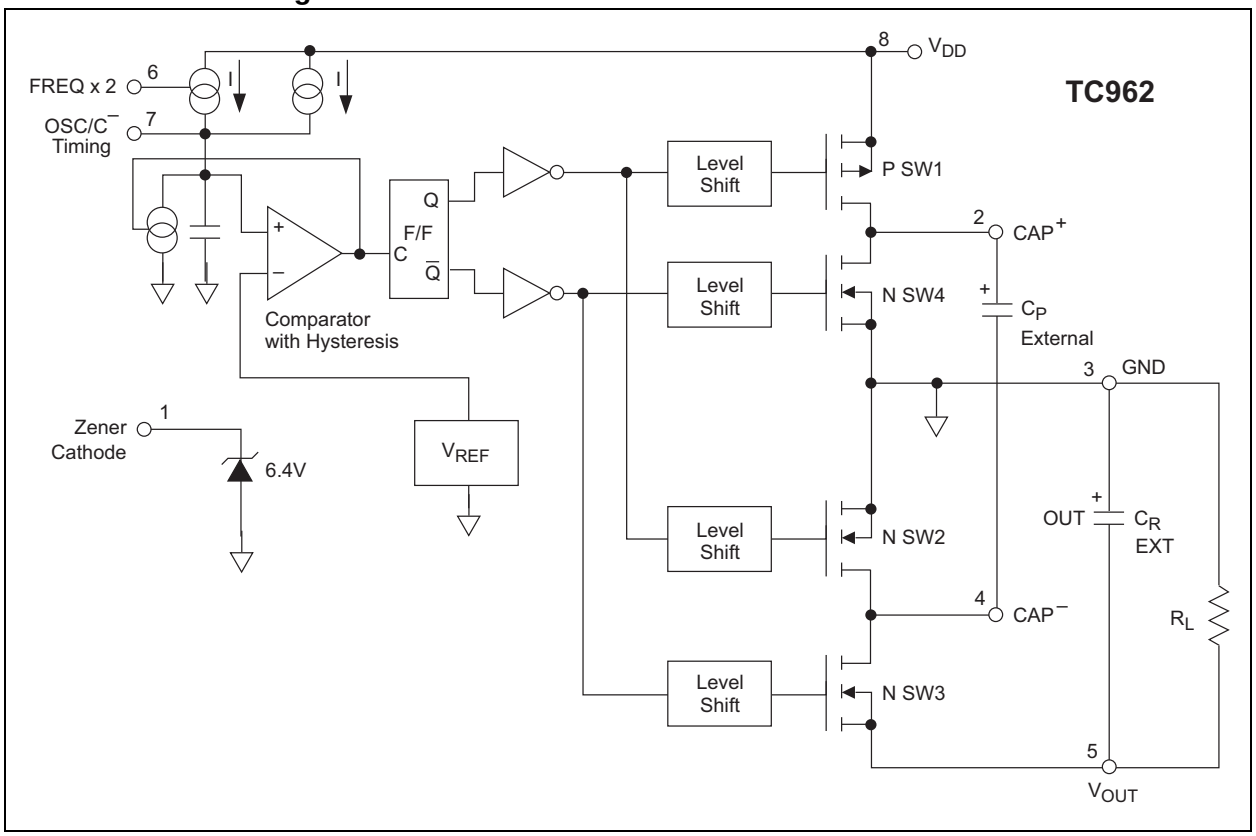
Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V_{DD} to GND) ..... +18V
Input Voltage Any Pin
..... (V_{DD} +0.3) to (V_{SS} -0.3) **(Note 1)**
Current Into Any Pin..... 10 mA
ESD Protection ..... ±2000V
Output Short Circuit ..... Continuous (at 5.5V Input)
Package Power Dissipation ($T_A \leq 70°C$)
SOIC ..... 760 mW
PDIP..... 730 mW
CERDIP ..... 800 mW
Package Thermal Resistance
CERDIP, $R\theta_{J-A}$ ..... 90°C/W
PDIP, $R\theta_{J-A}$ ..... 140°C/W
Operating Temperature Range
CPA, COE ..... 0°C to +70°C
IJA..... -25°C to +85°C
EPA ..... -40°C to +85°C
MJA..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC962 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 15V, T_A = 25°C (See Figure) unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{DD}	Supply Voltage	3	—	18	V	
I_S	Supply Current	—	—	—	µA	$R_L = \infty$
	V_{DD} = 15V	—	510	700		T_A = +25°C
		—	560	—		$0 \leq T_A \leq +70°C$
		—	650	—		$-55°C \leq T_A \leq +125°C$
	V_{DD} = 5V	—	190	—		T_A = +25°C
		—	210	—		$0 \leq T_A \leq +70°C$
		—	210	—		$-55°C \leq T_A \leq +125°C$
R_O	Output Source Resistance	—	32	37	Ω	I_L = 20 mA, V_{DD} = 15V
		—	35	40		I_L = 80 mA, V_{DD} = 15V
		—	—	50		I_L = 3 mA, V_{DD} = 5V
F_{OSC}	Oscillator Frequency	—	12	—	kHz	Pin 6 Open
		—	24	—		Pin 6 GND
P_{EFF}	Power Efficiency	93	97	—	%	R_L = 2 kΩ
		—	—	—		
V_{DEF}	Voltage Efficiency	99	99.9	—	%	$R_L = \infty$
		—	—	—		Over temperature range
		96	—	—		
V_Z	Zener Voltage	6.0	6.2	6.4	V	I_Z = 5 mA
Z_{ZT}	Zener Impedance	—	12	—	Ω	I_L = 2.5 mA to 7.5 mA

Note 1: Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power-up" of the TC962.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin DIP) (8-Pin CERDIP)	Symbol	Description
1	Zener Cathode	Cathode of internal Zener diode.
2	C^+	Positive side of external CP capacitor (pump cap).
3	GND	Ground terminal.
4	C^-	Negative side of external CP capacitor (pump cap).
5	V_{OUT}	Output voltage.
6	FREQ x 2	If grounded, frequency doubles.
7	C_{OSC}	Capacitor to GND will decrease frequency.
8	V_{DD}	Input voltage.

Pin No. (16-Pin SOIC)	Symbol	Description
1	Zener Cathode	Cathode of internal Zener diode.
2	NC	No connect.
3	C^+	Positive side of external CP capacitor (pump cap).
4	NC	No connect.
5	GND	Ground terminal.
6	NC	No connect.
7	C^-	Negative side of external CP capacitor (pump cap).
8	NC	No connect.
9	NC	No connect.
10	V_{OUT}	Output voltage.
11	NC	No connect.
12	FREQ x 2	If grounded, frequency doubles.
13	NC	No connect.
14	C_{OSC}	Capacitor to GND will decrease frequency.
15	NC	No connect.
16	V_{DD}	Input voltage.

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3.0 APPLICATIONS INFORMATION

3.1 Theory of Operation

The TC962 is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional block diagram shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown:

$$3\ (R_{DS(ON)}\ C_P) < C_P/(0.5\ f_{OSC})$$

In the next cycle, SW1 and SW2 are turned off and after a very short interval of all switches being off (this prevents large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C_P is then transferred to C_R, *but with the polarity inverted*. In this way, a negative voltage is now derived.

An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is returned to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC962. Grounding pin 6 will turn on a current source and double the frequency. This will double the charge current going into the internal capacitor, as well as any capacitor added to pin 7.

A Zener diode has been added to the TC962 for use as a reference in building external regulators. This Zener runs from pin 1 to ground.

3.2 Latch-Up

All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input from going above or below the supply rail, or latch-up will occur. The result of latch-up is an effective short between V_{DD} and V_{SS}. Unless the power supply input has a current limit, this latch-up phenomena will result in damage to the device. (*See AN763, Latch-up Protection for MOSFET Drivers*.)

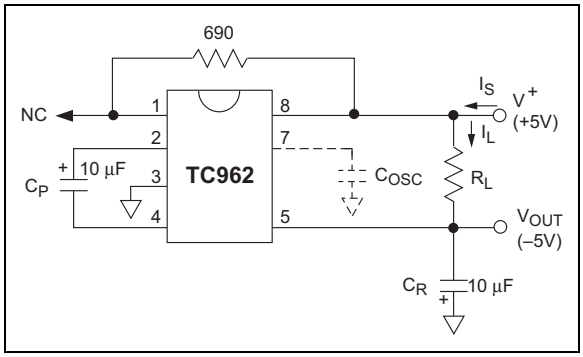

FIGURE 3-1: *Test Circuit*

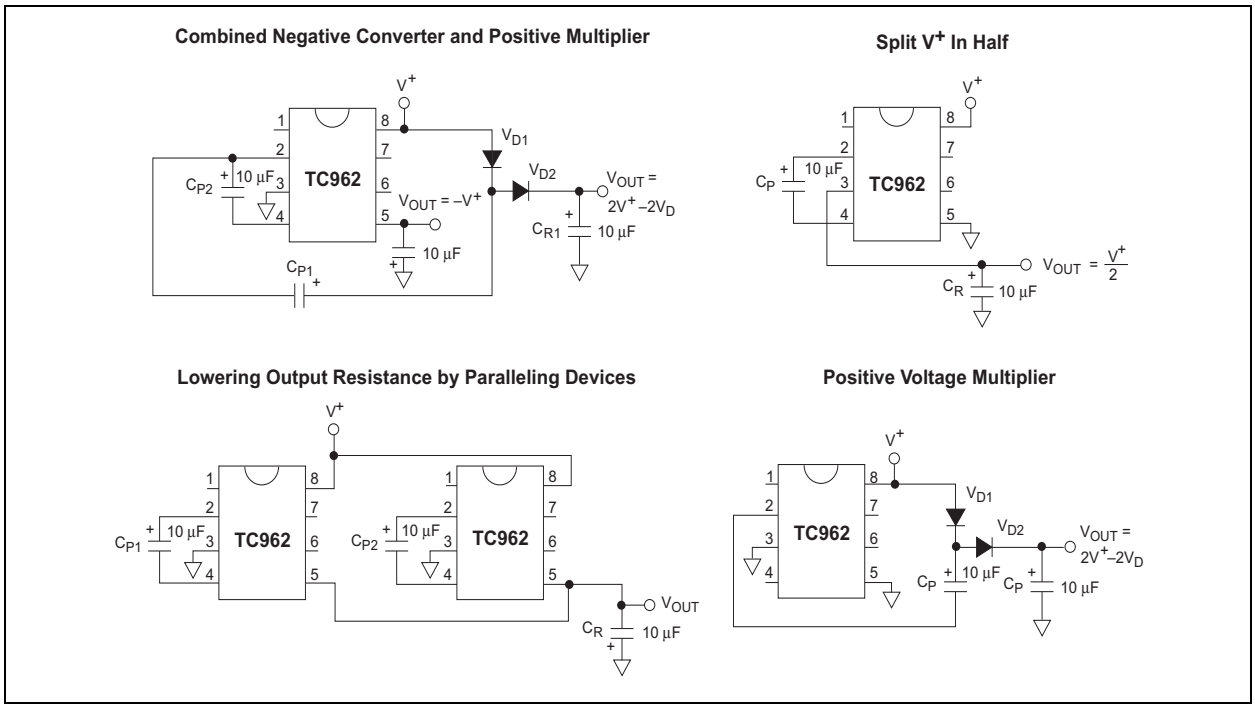

FIGURE 3-2: *Typical Applications*

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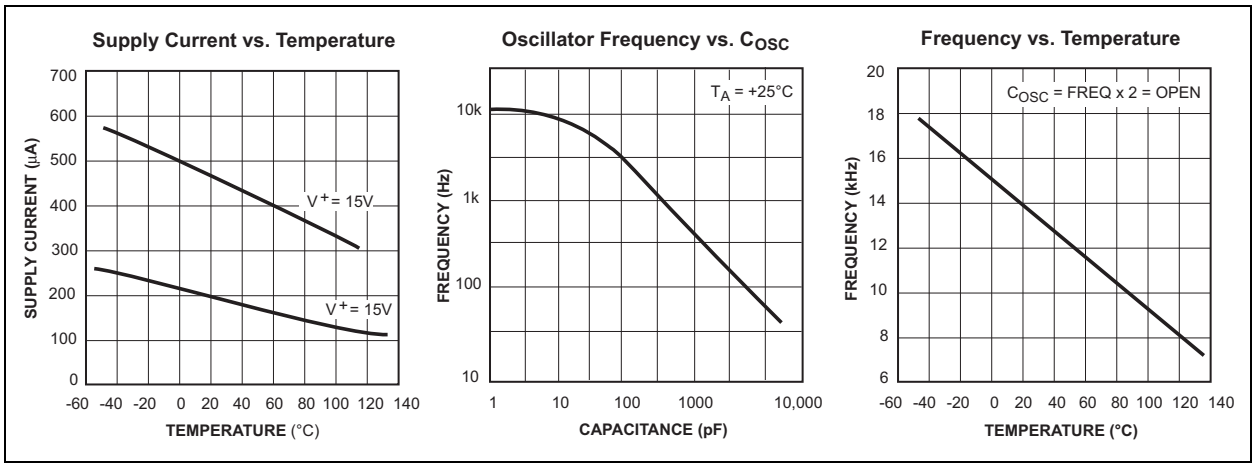
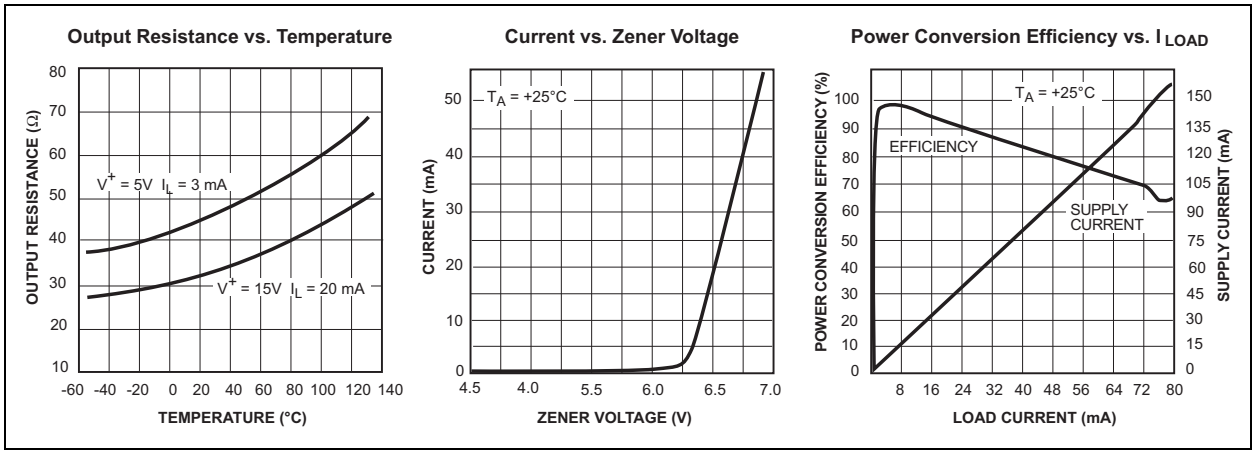
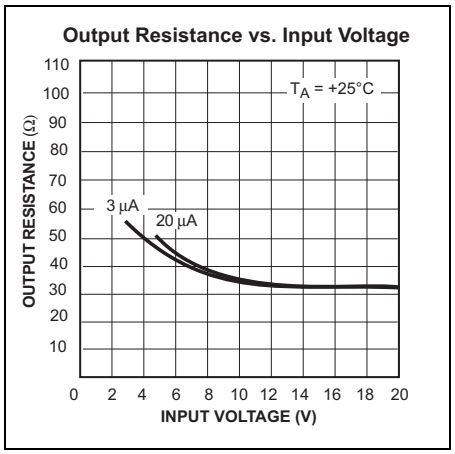
4.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Circuit of Figure , $C_P = C_R = 10\ \mu F$, $C_{PESR} \approx C_{RESR} \approx 1\Omega$.







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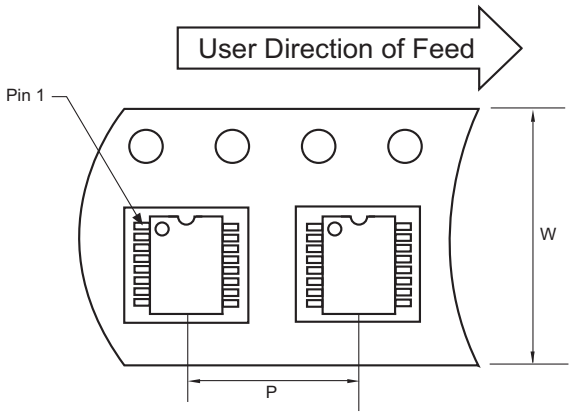
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Form

Component Taping Orientation for 16-Pin SOIC (Wide) Devices



Standard Reel Component Orientation
for 713 Suffix Device

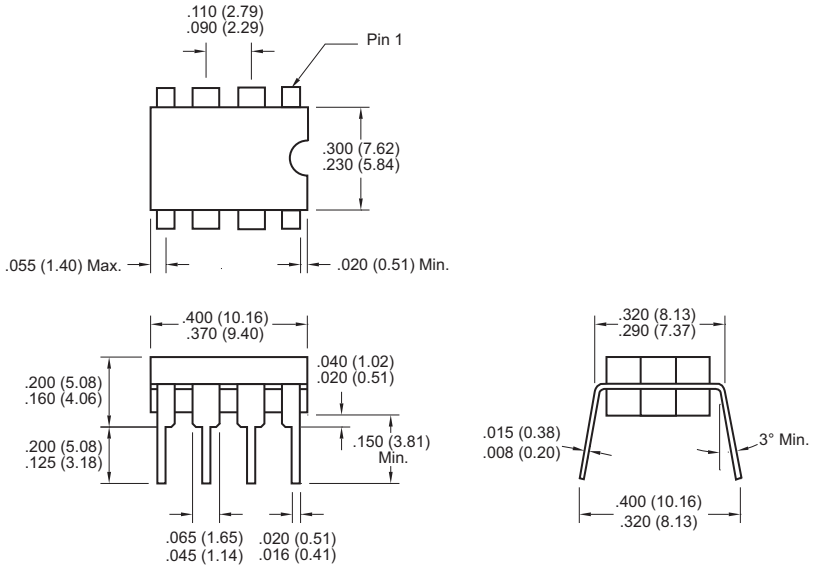
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin SOIC (W)	16 mm	12 mm	1000	13 in

5.3 Package Dimensions

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Pin CDIP (Narrow)



Dimensions: inches (mm)

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Package Dimensions (Continued)

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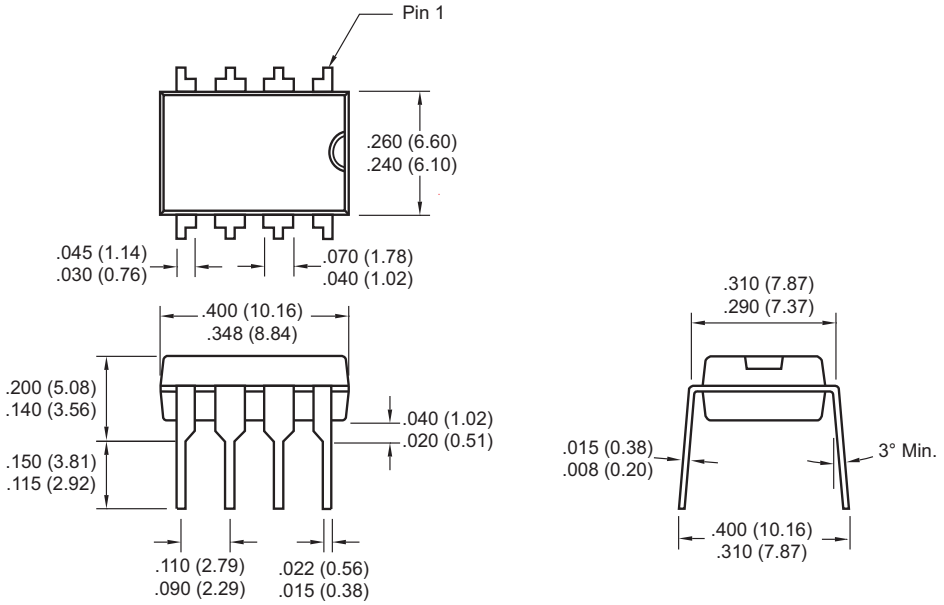
8-Pin Plastic DIP



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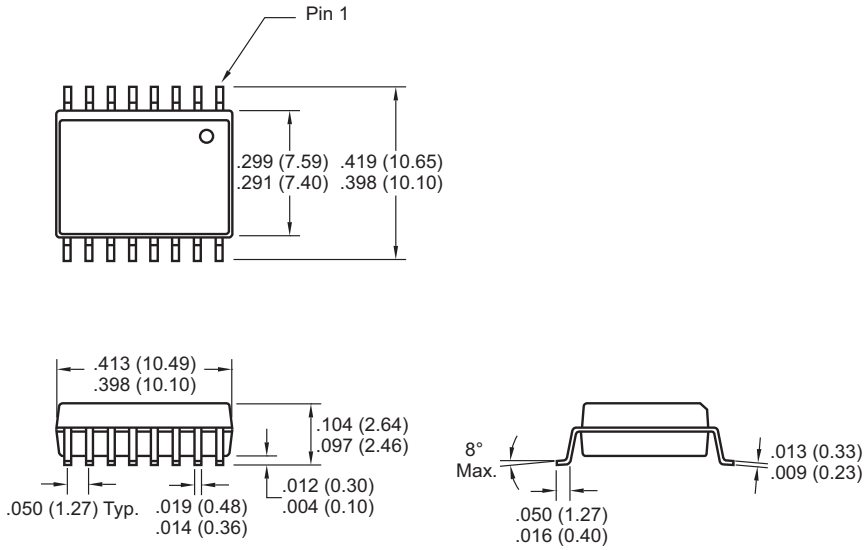
16-Pin SOIC (Wide)



Dimensions: inches (mm)

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6.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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NOTES:

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