Block Diagram
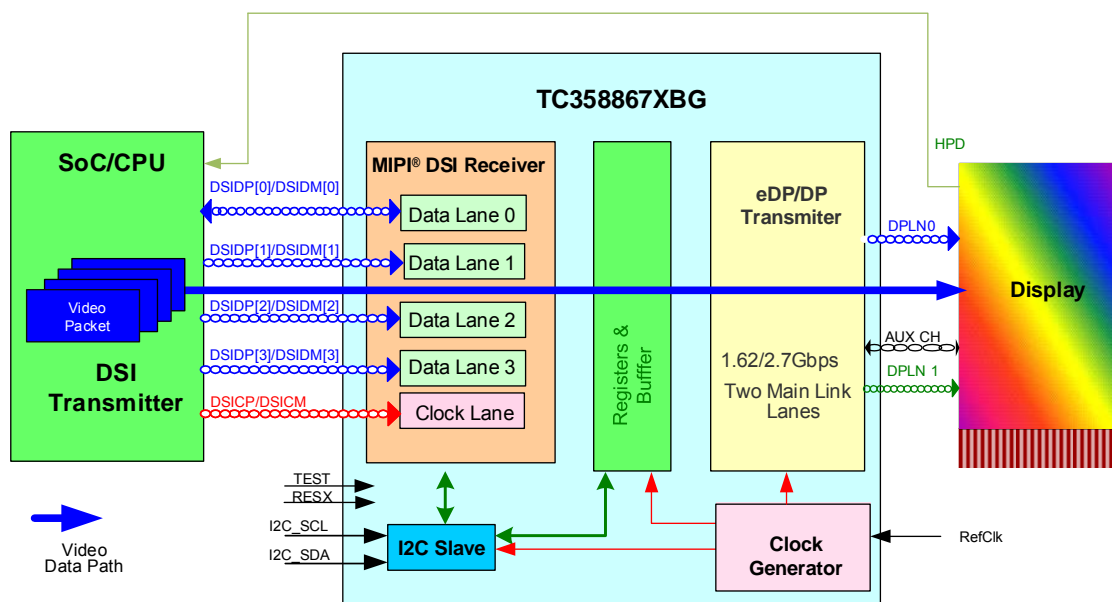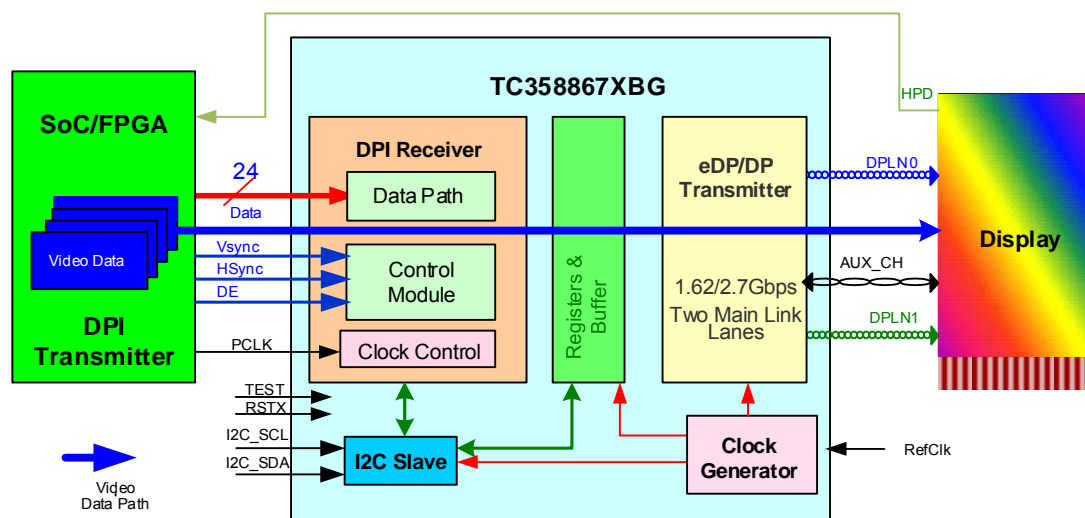
(1) MIPI® DSI to eDP/DP conversion

(2) MIPI® DPI（RGB parallel）to eDP/DP conversion
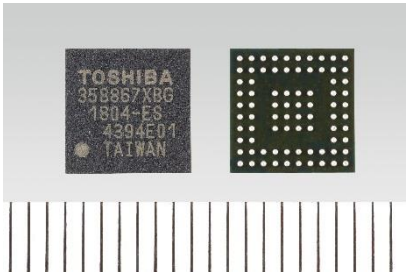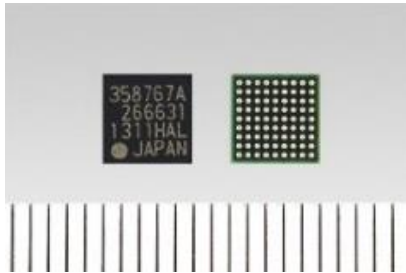

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.
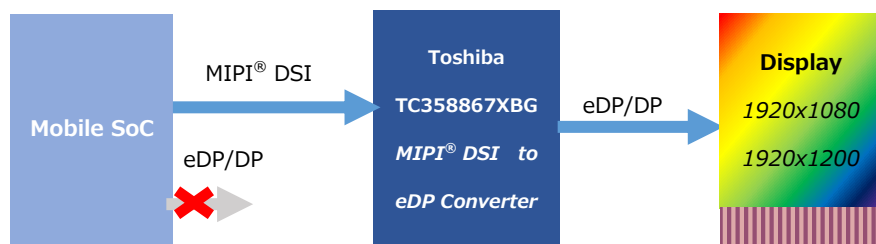
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Product Specifications

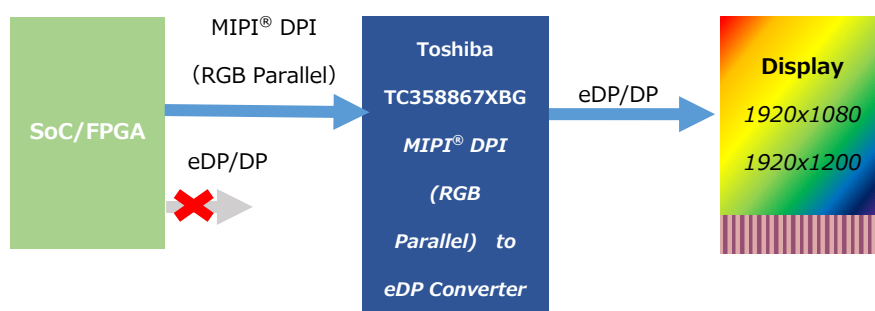| Item	Description	
Input video stream format (Rx)	MIPI® DSI 1.01	MIPI® DPI 2.0 (RGB Parallel)
Rx data rate	1Gbps/lane x 4	24bit, PCLK 154MHz (Max)
Audio input	2 channels	
Output video stream (Tx)	VESA® DisplayPort™ 1.1a	
Tx data rate	1.62Gbps/lane x 2or 2.7Gbps/lane x 2	
Maximum resolution	WUXGA （1920×1200）	
Voltage	Core, MIPI® D-PHY: 1.2 V ± 0.06 V, Digital I/O: 1.8 V ± 0.09 V, DisplayPort™: 1.8 V ± 0.09 V, 1.2 V ± 0.06 V	

Package Line-up

Part number	TC358867XBG	TC358767AXBG
Overview		
Package type	BGA	BGA
Ball pitch	0.65 mm	0.5 mm
Ball count	80	81
Package size	7 × 7 mm	5 × 5 mm
ES	Available	Available
MP	April, 2018	Available

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Application Circuit Example

(1) Connection from mobile SoC to eDP display panel

Mobile SoC → MIPI® DSI → Toshiba TC358867XBG MIPI® DSI to eDP Converter → eDP/DP → Display 1920x1080 1920x1200

eDP/DP ✖

(2) Connection from SoC or FPGA to eDP display panel

SoC/FPGA → MIPI® DPI (RGB Parallel) → Toshiba TC358867XBG MIPI® DPI (RGB Parallel) to eDP Converter → eDP/DP → Display 1920x1080 1920x1200

eDP/DP ✖

(3) Dual panel

Mobile SoC → MIPI® DSI → Toshiba TC358867XBG MIPI® DSI to eDP Converter → eDP/DP → Display 1920x1080 1920x1200

Mobile SoC → eDP/DP → Display 1920x1080 1920x1200
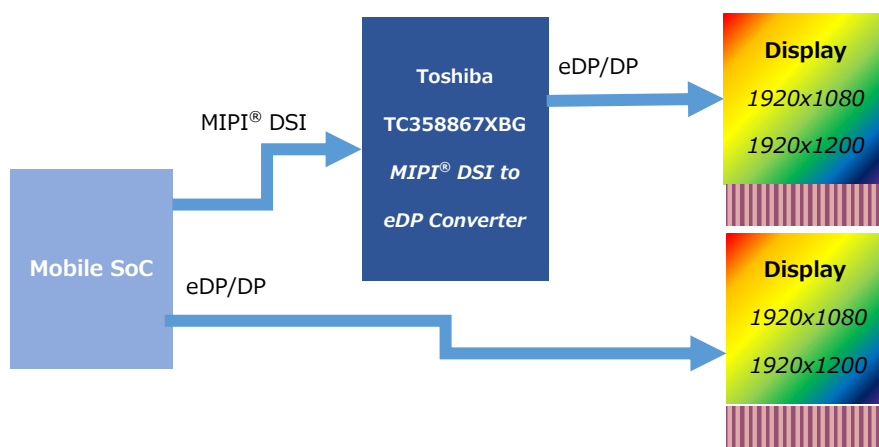
Note: The system configuration example shown above is provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Any license to any industrial property rights is not by providing this example.

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*DisplayPort™ is a trademark owned by the Video Electronics Standards Association (VESA®) in the United States and other countries.

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