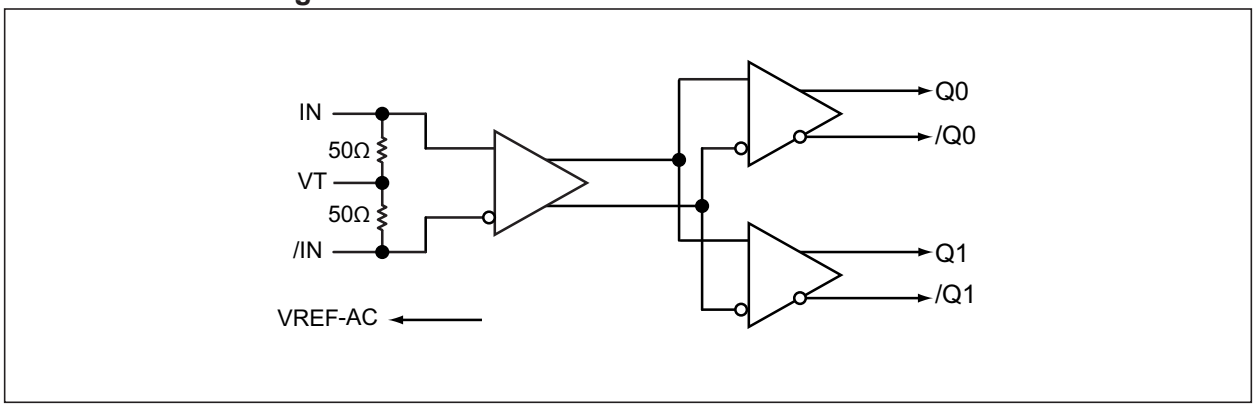
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
    Continuous ..... 50 mA
    Surge ..... 100 mA
Termination Current (I_{VT})
    Source or Sink on VT Pin ..... ±100 mA
Input Current
    Source or Sink Current on IN, /IN ..... ±50 mA
Reference Current (V_{REF-AC})
    V_{REF-AC} Current ..... ±1.5 mA
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings ††

Supply Voltage (V_{CC}) ..... +2.375V to +3.63V
Operating Temperature Range (T_A) ..... –40°C to +85°C

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	V_{CC}	2.375	—	3.63	V	—
Power Supply Current	I_{CC}	—	55	80	mA	No load, max. V_{CC}
Input HIGH Voltage IN, /IN	V_{IH}	V_{CC} – 1.6	—	V_{CC}	V	Note 2
Input LOW Voltage IN, /IN	V_{IL}	0	—	V_{IH} – 0.1	V	—
Input Voltage Swing IN, /IN	V_{IN}	0.1	—	1.7	V	See Figure 4-1
Differential Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	See Figure 4-2
IN to VT Resistance	R_{IN}	40	50	60	Ω	—
Voltage from Input to VT	V_{T_IN}	—	—	1.28	V	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: $V_{IH(MIN)}$ not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage Q0, /Q01, Q1, /Q1	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output Low Voltage Q0, /Q01, Q1, /Q1	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Output Differential Swing Q0, /Q01, Q1, /Q1	V_{OUT}	550	800	—	mV	See Figure 4-1
Differential Output Voltage Swing Q0, /Q01, Q1, /Q1	V_{DIFF_OUT}	1100	1600	—	mV	See Figure 4-2

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Frequency	f_{MAX}	—	5	—	Gbps	NRZ (Data)
		5	—	—	GHz	$V_{OUT} \geq$ 400 mV (Clock)
Propagation Delay	t_{PD}	110	170	260	ps	$V_{IN} \geq$ 100 mV
Channel-to-Channel Skew	t_{CHAN}	—	75	—	ps	Note 3
Part-to-Part Skew	t_{SKEW}	—	—	100	ps	Note 3
Additive Phase Jitter	t_{JITTER}	—	37	—	fs	622 MHz Integration Range: 12 kHz to 20 MHz
		—	97	—		156.25 MHz Integration Range: 12 kHz to 20 MHz
		—	167	—		100 MHz Integration Range: 12 kHz to 20 MHz
Output Rise/Fall Time	t_r/t_f	35	80	110	ps	20% to 80% at full swing

Note 1: High frequency AC parameters are guaranteed by design and characterization.

2: Input-to-input skew is the difference in time from and input-to-output in comparison to any other input-to-output.

3: Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, 3x3 QFN-16Lead	θ_{JA}	—	60	—	°C/W	Still-air
			54	—0		500 lpfm
	Ψ_{JB}	—	33	—	°C/W	Junction-to-board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400 mV, T_A = +25°C, unless otherwise stated.

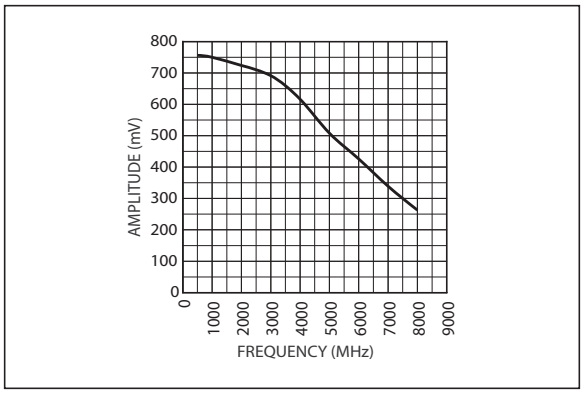


FIGURE 2-1: *Frequency vs. Amplitude.*

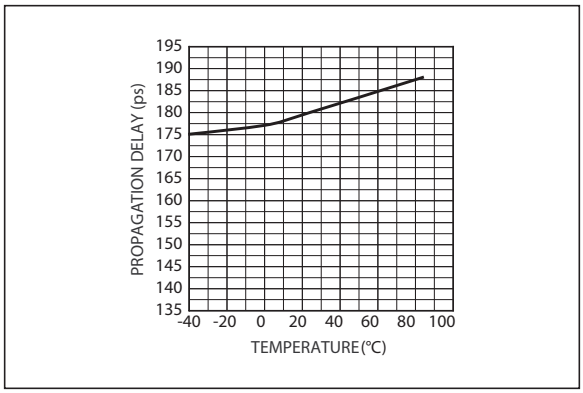


FIGURE 2-4: *Propagation Delay vs Temperature.*

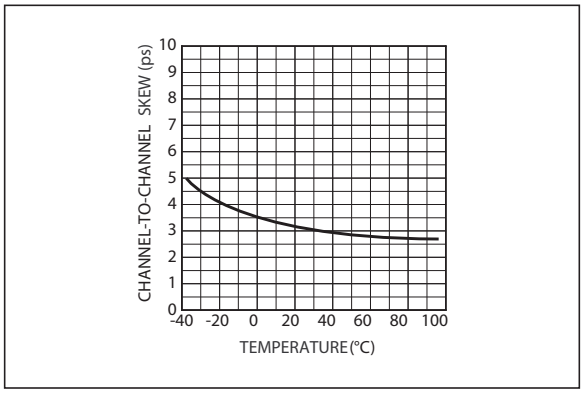


FIGURE 2-2: *Channel-To-Channel Skew vs. Temperature.*

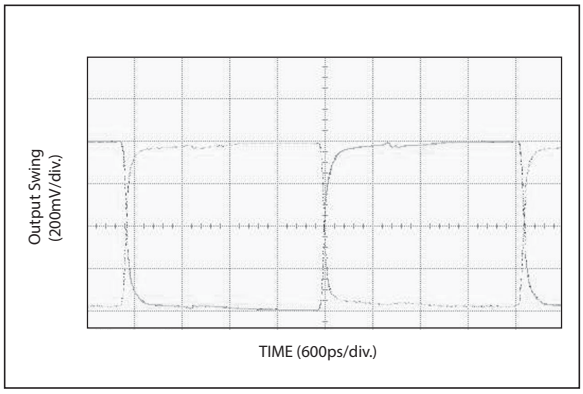


FIGURE 2-5: *200 MHz Output.*

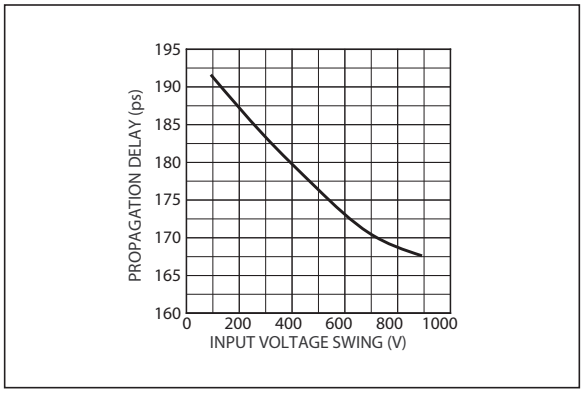


FIGURE 2-3: *Propagation Delay vs. Input Voltage Swing.*

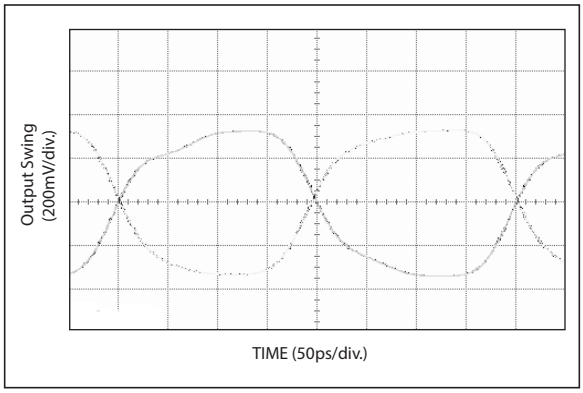


FIGURE 2-6: *2.5 GHz Output.*

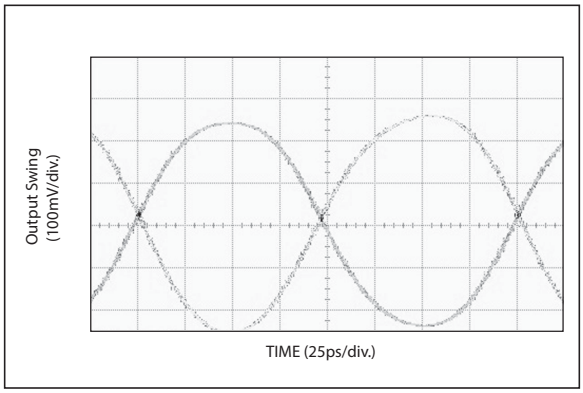


FIGURE 2-7: *5 GHz Output.*

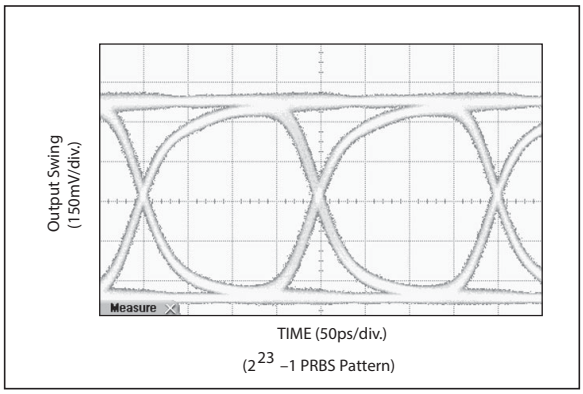


FIGURE 2-8: *5 Gbps Output.*

3.0 PHASE NOISE PLOTS

V_{CC} = +3.3V, T_A = +25°C.

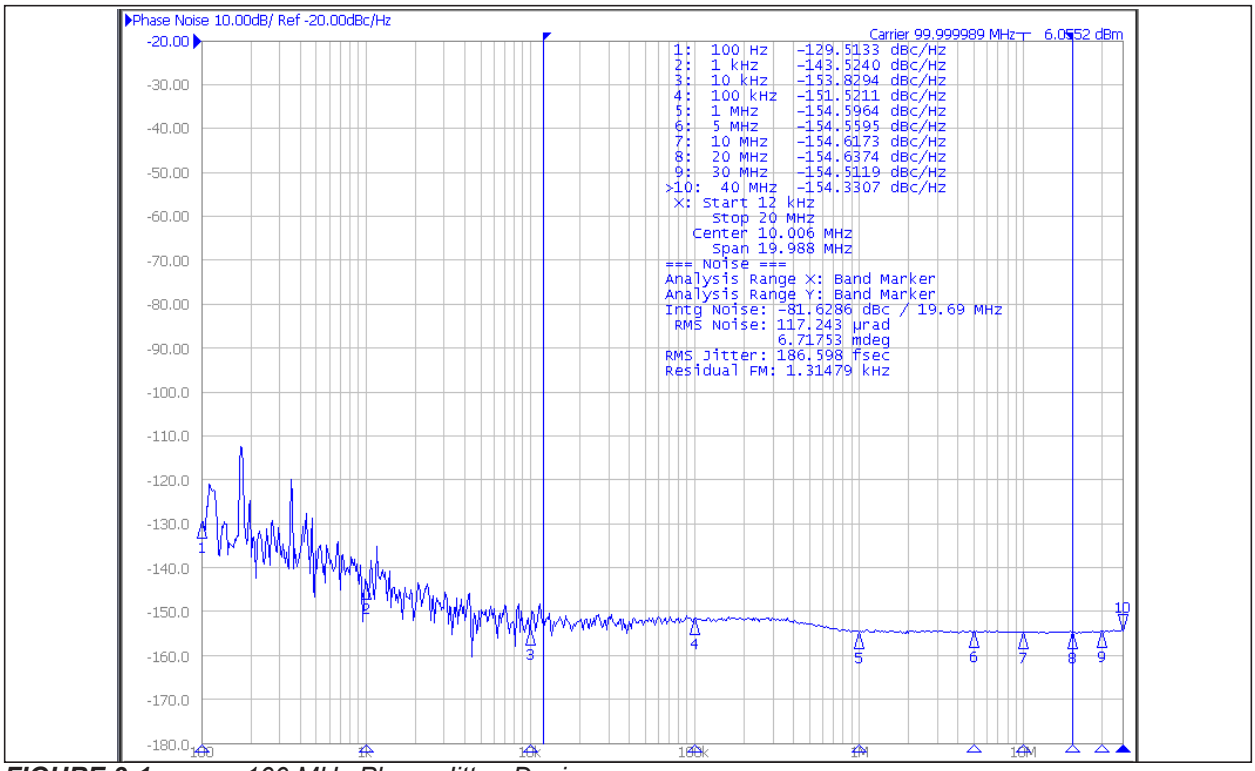


FIGURE 3-1: *100 MHz Phase Jitter, Device.*

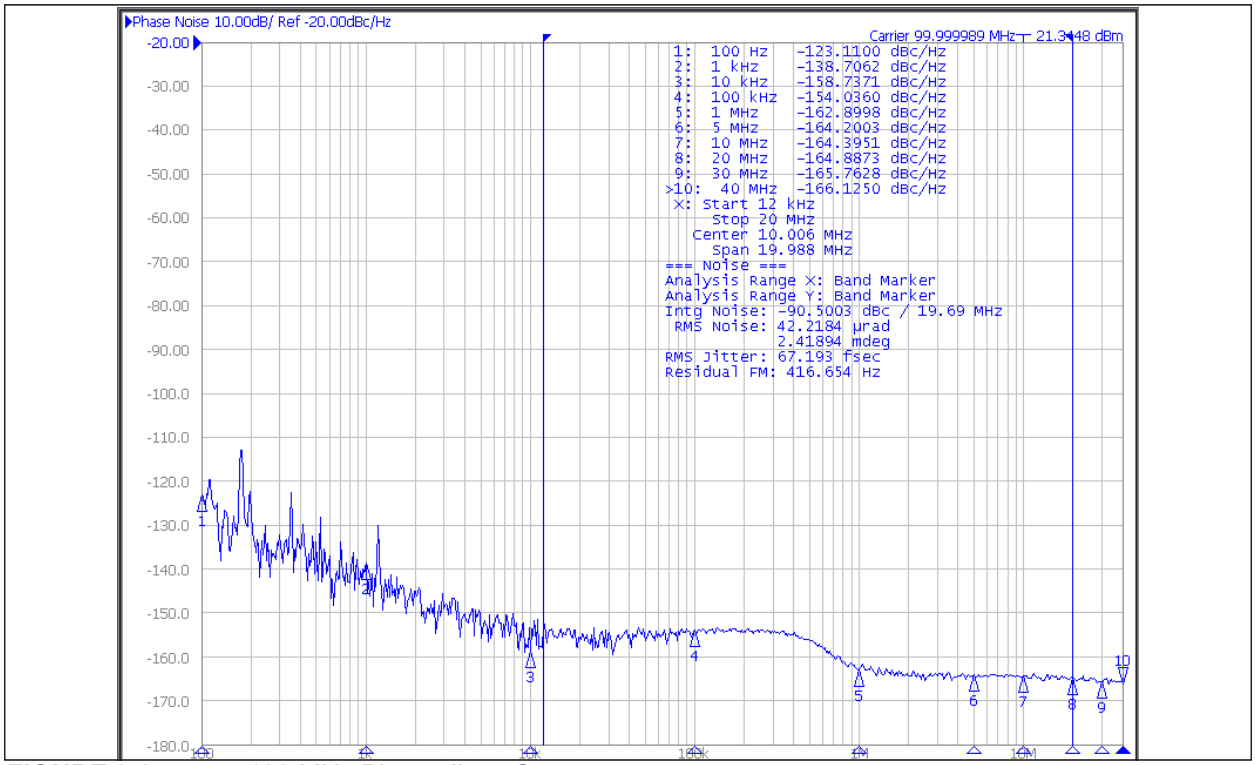


FIGURE 3-2: *100 MHz Phase Jitter, Source.*

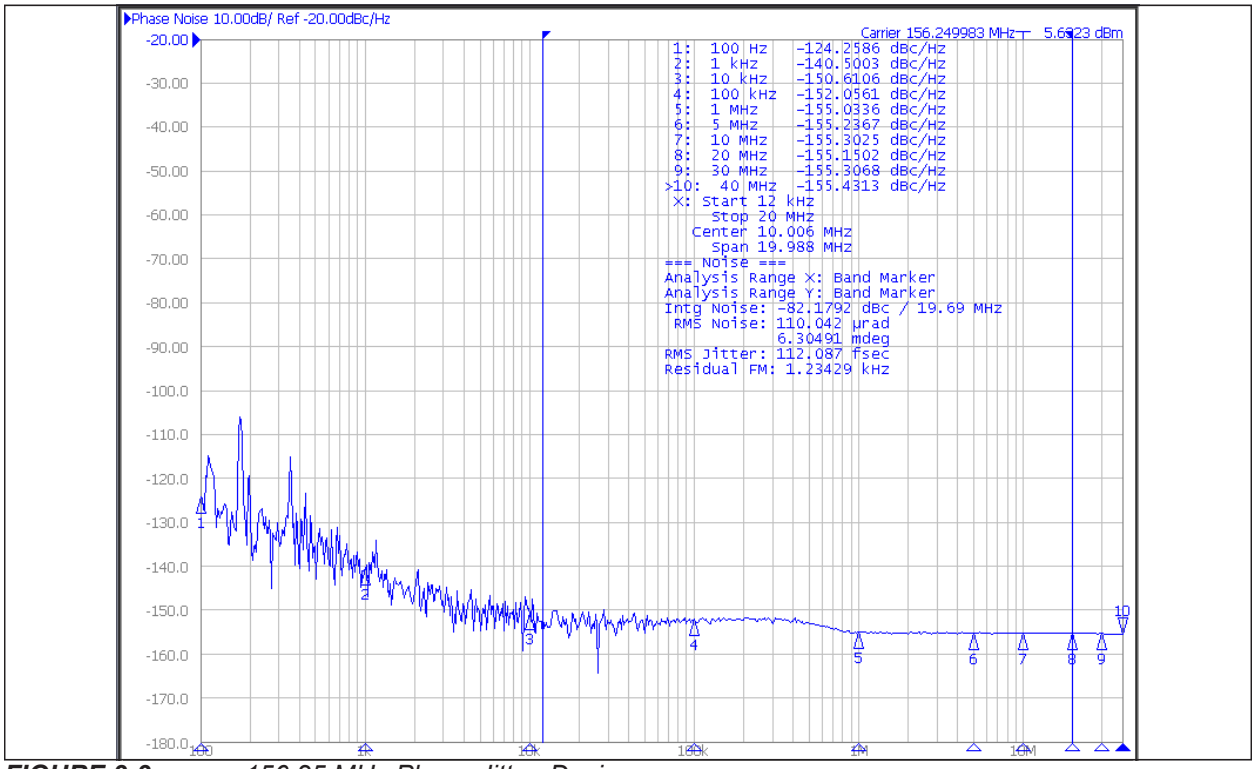


FIGURE 3-3: *156.25 MHz Phase Jitter, Device.*

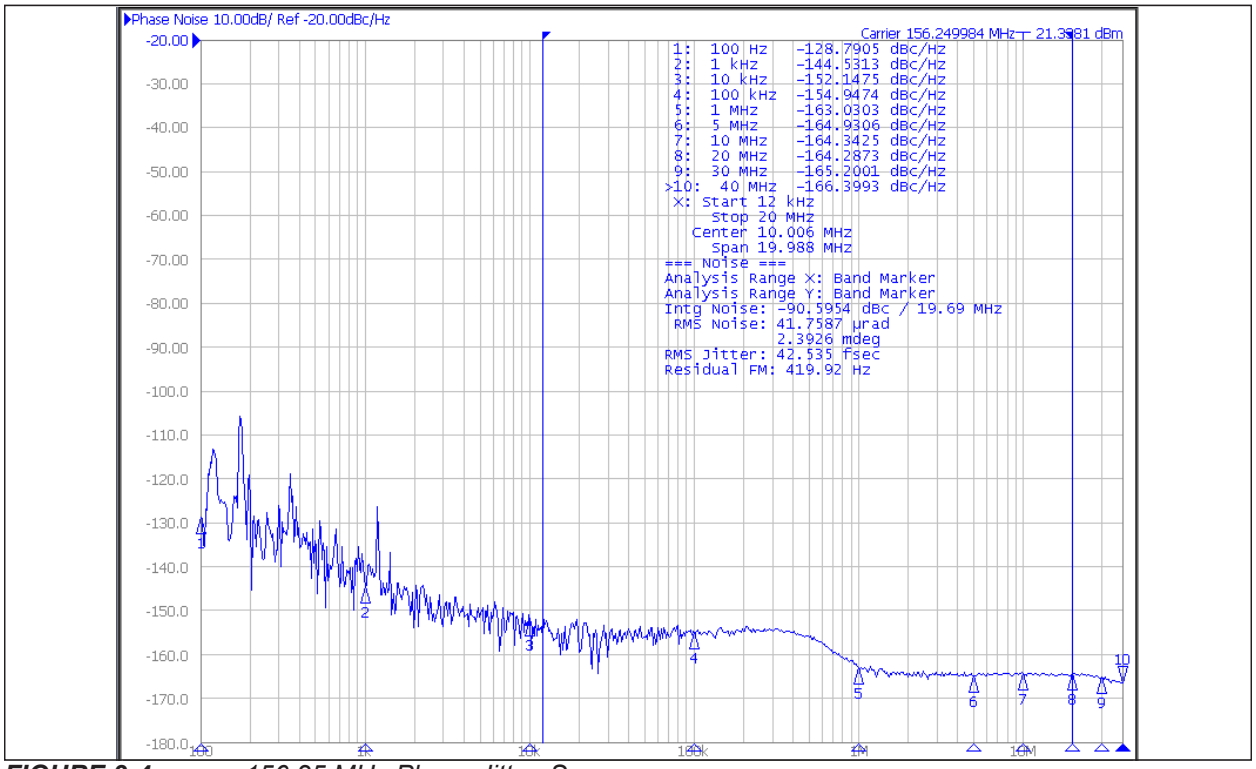


FIGURE 3-4: *156.25 MHz Phase Jitter, Source.*

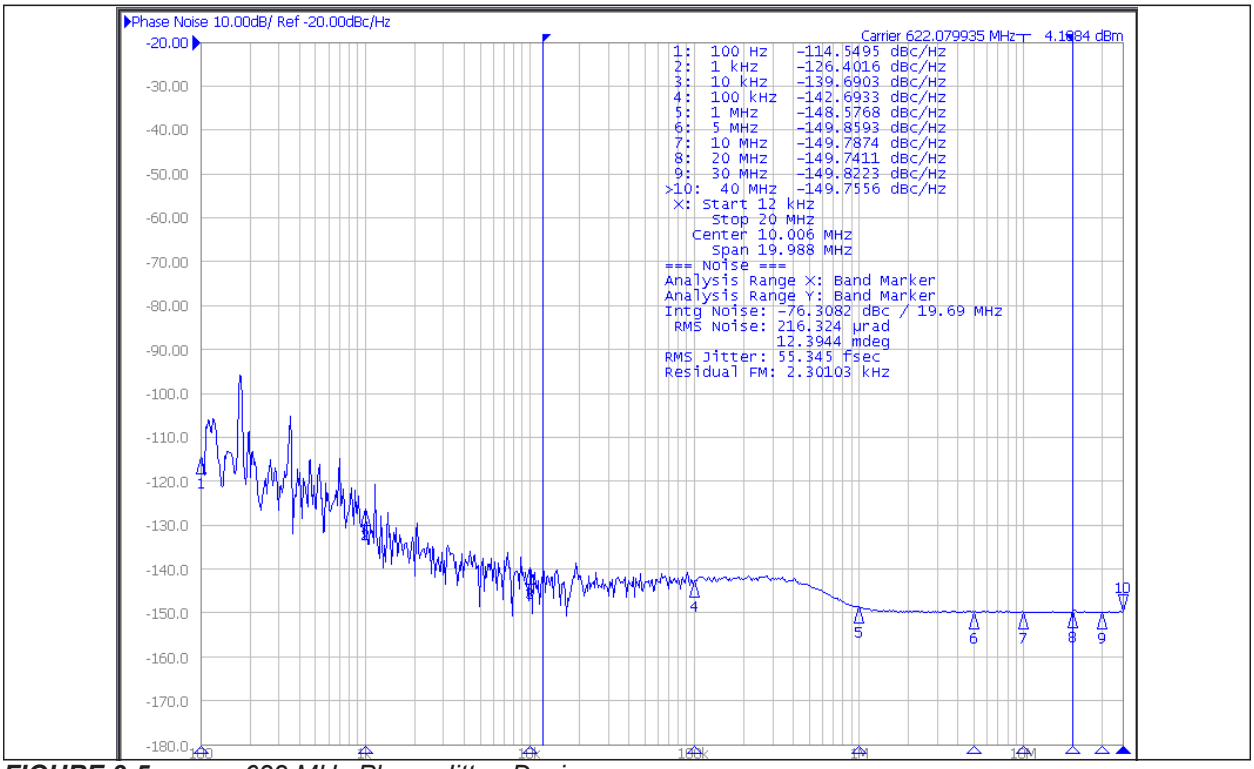


FIGURE 3-5: *622 MHz Phase Jitter, Device.*

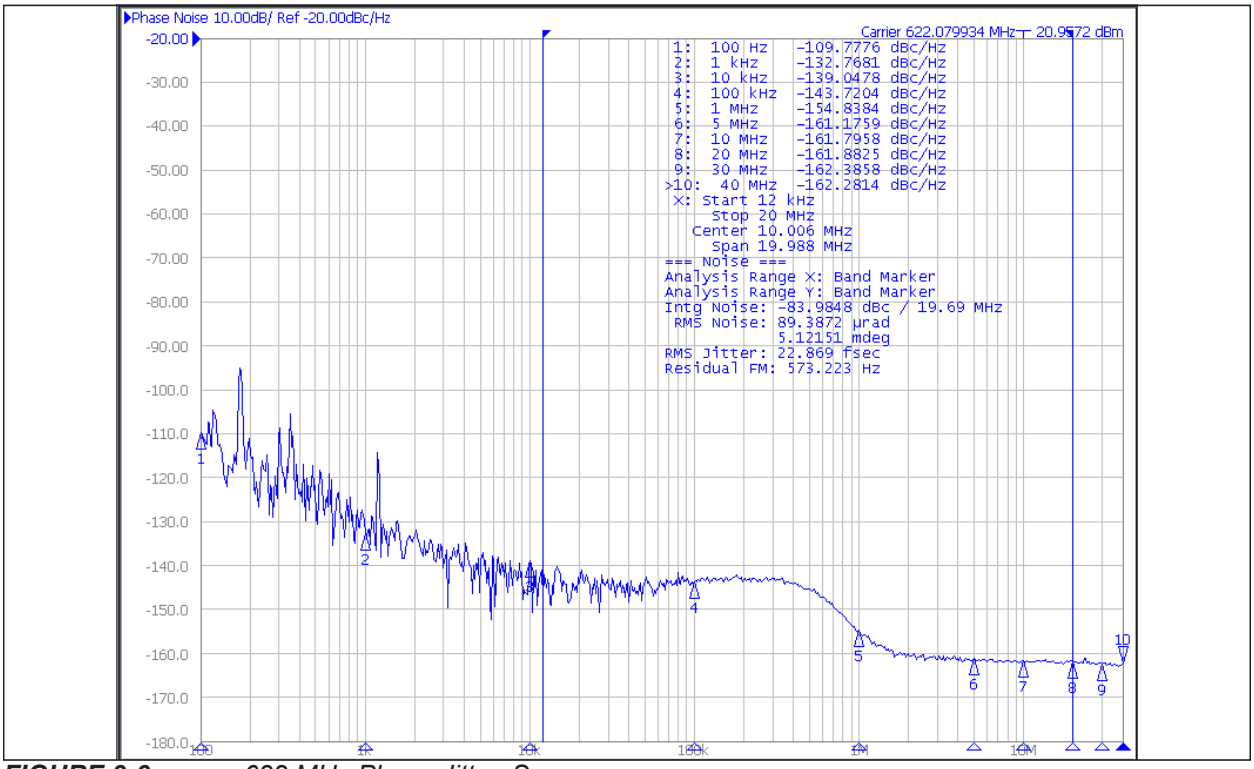


FIGURE 3-6: *622 MHz Phase Jitter, Source.*

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See **Section 5.0 "Input Interface Applications"**.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See **Section 5.0 "Input Interface Applications"**.
3	VREF_AC	Reference Output Voltage: This output biases to V_{CC} – 1.2V. It is used when AC-coupling the inputs (IN, /IN). Connect VREF_AC directly to the VT pin. Bypass with 0.01 µF low ESR capacitor to VCC. Maximum current source or sink is 0.5 mA. See **Section 5.0 "Input Interface Applications"**.
5, 8, 13, 16	VCC	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors. 0.01 µF capacitor should be as close to VCC pin as possible.
12, 11, 9, 10	Q0, /Q0 Q1, /Q1	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 800 mV. Unused output pairs may be left floating with no impact on jitter. See **Section 6.0 "LVPECL Output Applications"**.
6, 7, 14, 15	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.

Single-Ended and Differential Swings

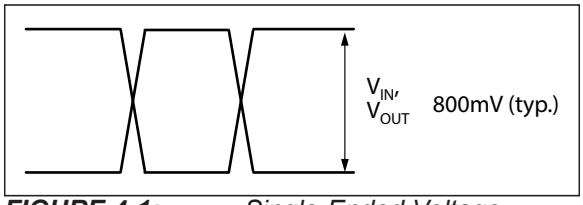


FIGURE 4-1: *Single-Ended Voltage Swing.*

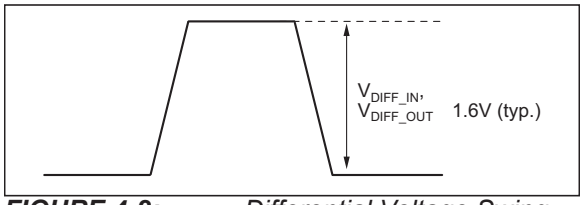
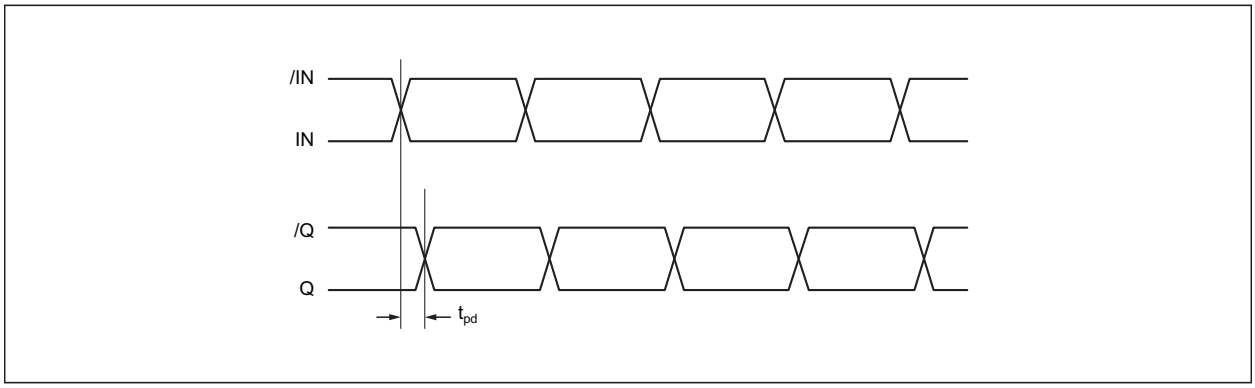


FIGURE 4-2: *Differential Voltage Swing.*

Timing Diagram



Input Stage

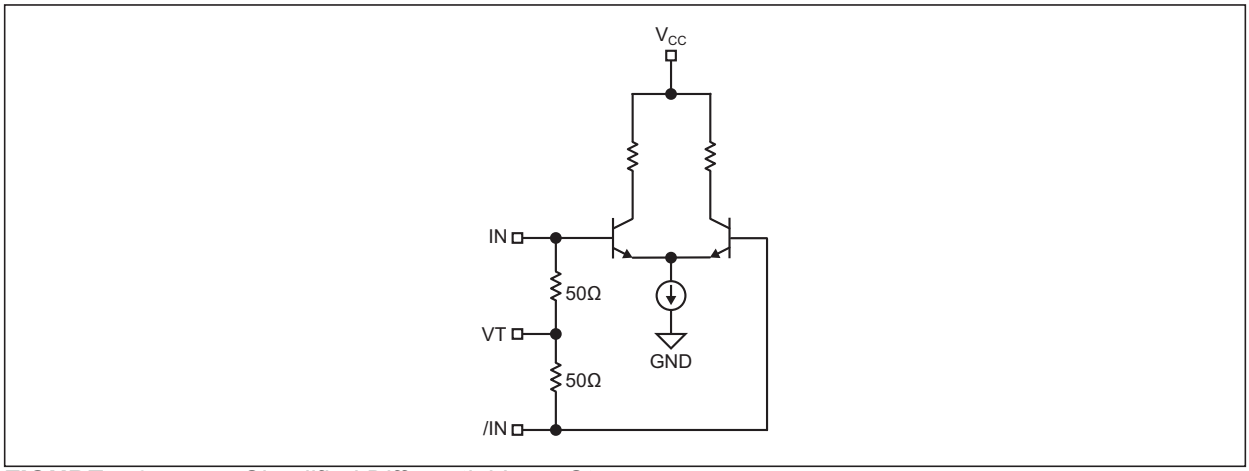


FIGURE 4-3: *Simplified Differential Input Stage.*

5.0 INPUT INTERFACE APPLICATIONS

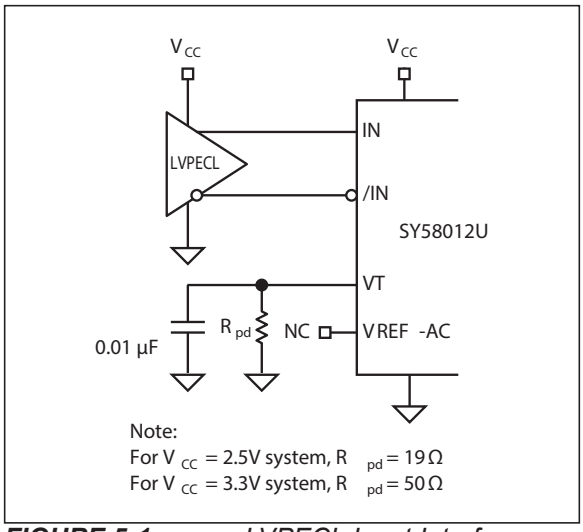


FIGURE 5-1: *LVPECL Input Interface.*

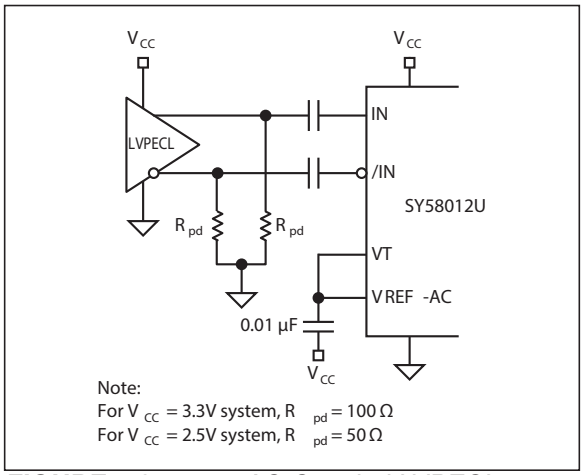


FIGURE 5-2: *AC-Coupled LVPECL Interface.*

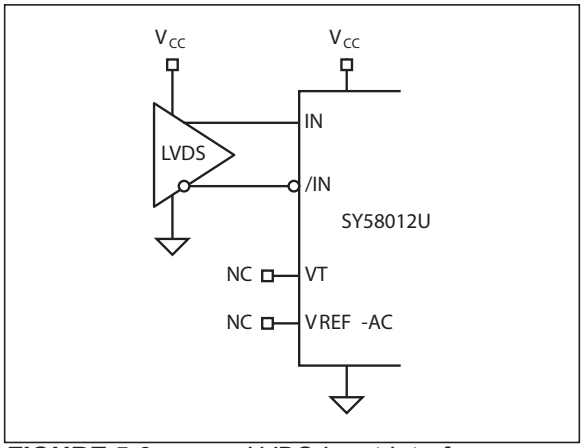


FIGURE 5-3: *LVDS Input Interface.*

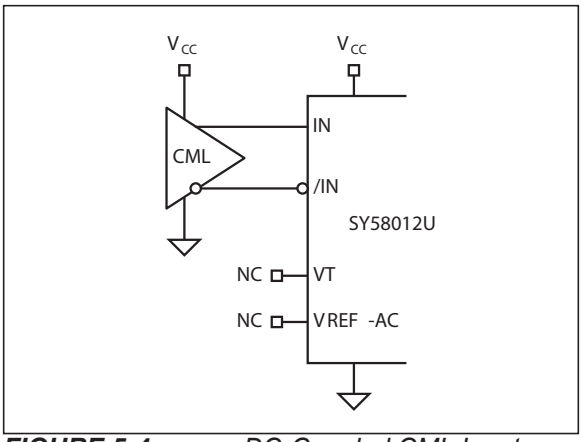


FIGURE 5-4: *DC-Coupled CML Input Interface.*

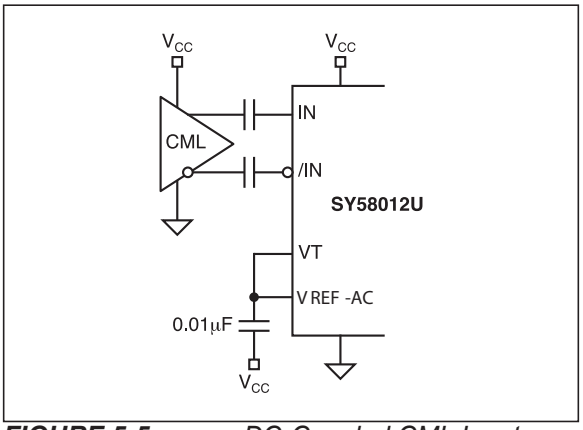


FIGURE 5-5: *DC-Coupled CML Input Interface.*

6.0 LVPECL OUTPUT APPLICATIONS

LVPECL output have very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figure 6-1 through Figure 6-3.

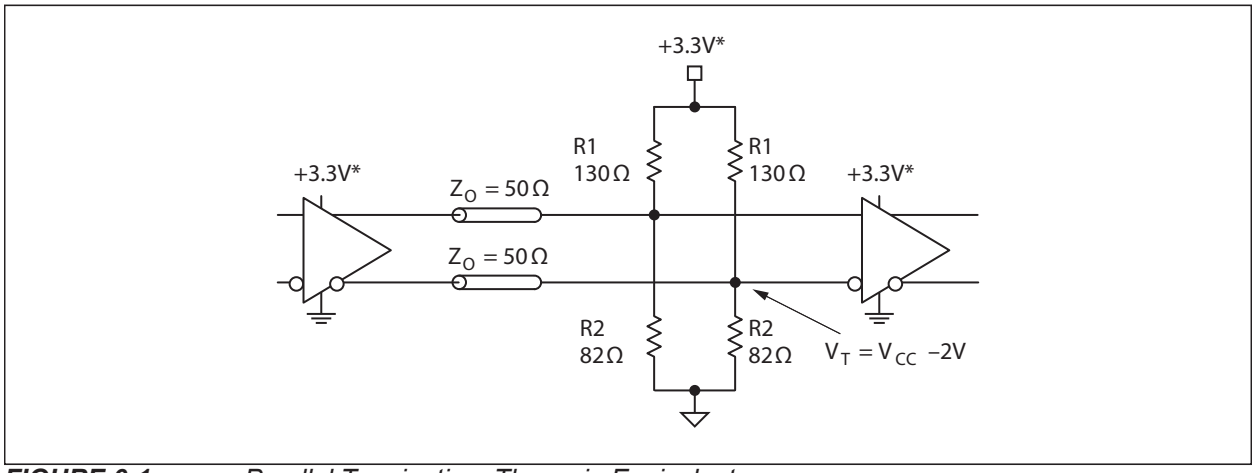


FIGURE 6-1: *Parallel Termination: Thevenin Equivalent.*

Note 1: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω

2: For +3.3V systems: R1 = 130Ω, R2 = 82Ω

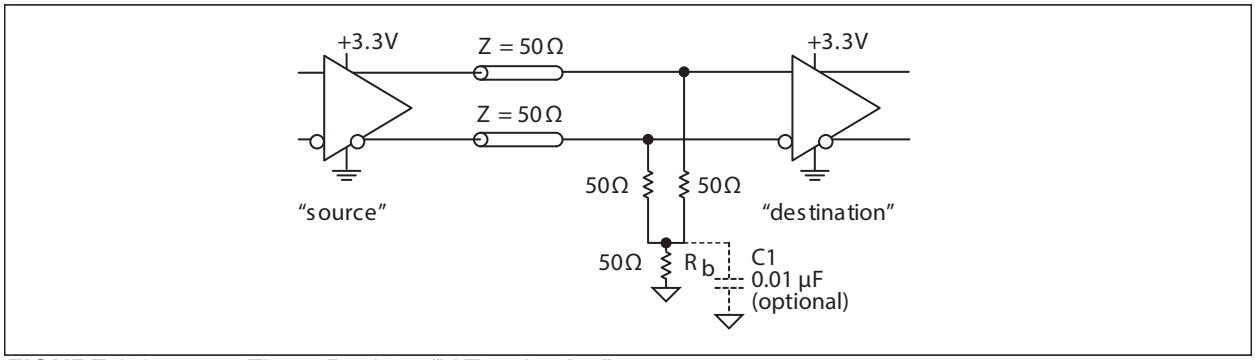


FIGURE 6-2: *Three-Resistor "Y-Termination".*

Note 1: Power-saving alternative to Thevenin termination.

2: Place termination resistors as close to destination inputs as possible.

3: R_b resistor sets the DC bias voltage, equal to V_T.

For +2.5V systems R_b = 19Ω.

For +3.3V systems R_b = 46Ω to 50Ω.

4: C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

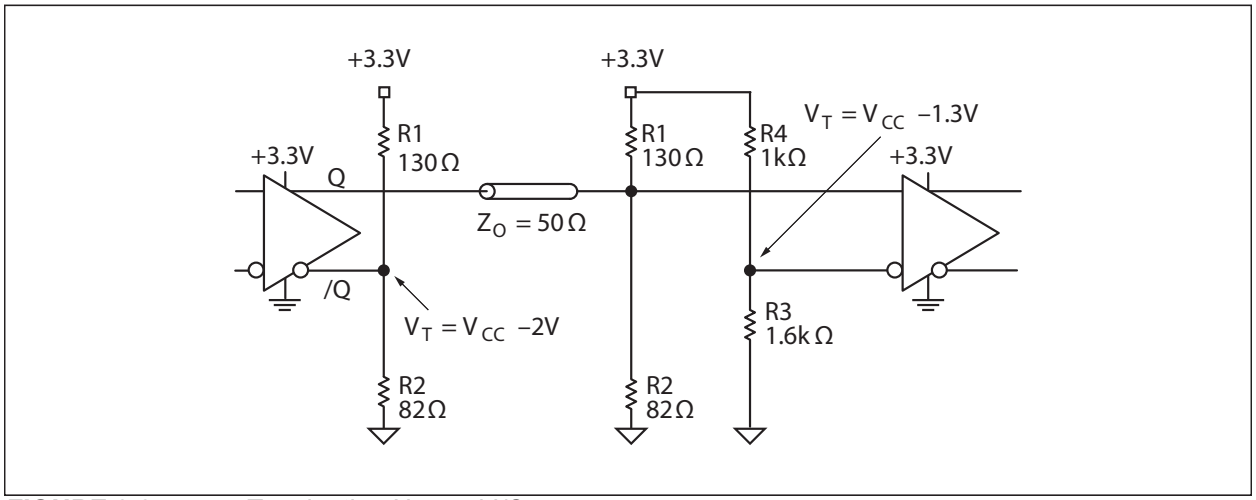


FIGURE 6-3: *Terminating Unused I/O.*

Note 1: Unused output (/Q) must be terminated to balance the output.

2: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25 kΩ, R4 = 1.2 kΩ.
For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1 kΩ, R4 = 1.6 kΩ.

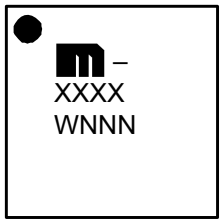
3: C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

4: Unused output pairs (Q and /Q) may be left floating.

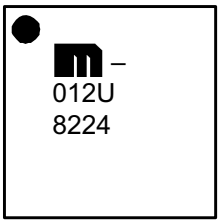
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

16-Lead QFN*



Example

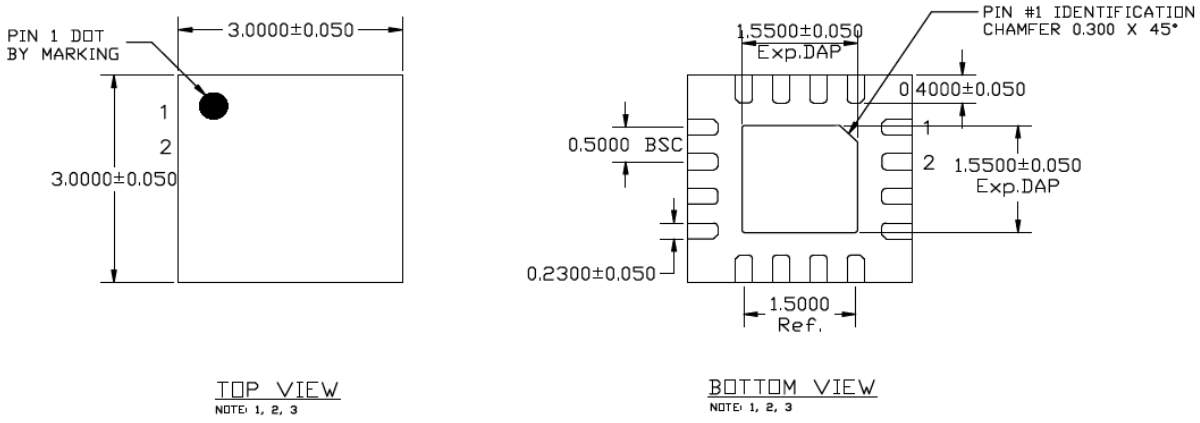


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

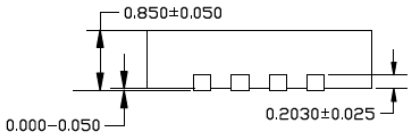
TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN33-16LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3

BOTTOM VIEW
NOTE: 1, 2, 3

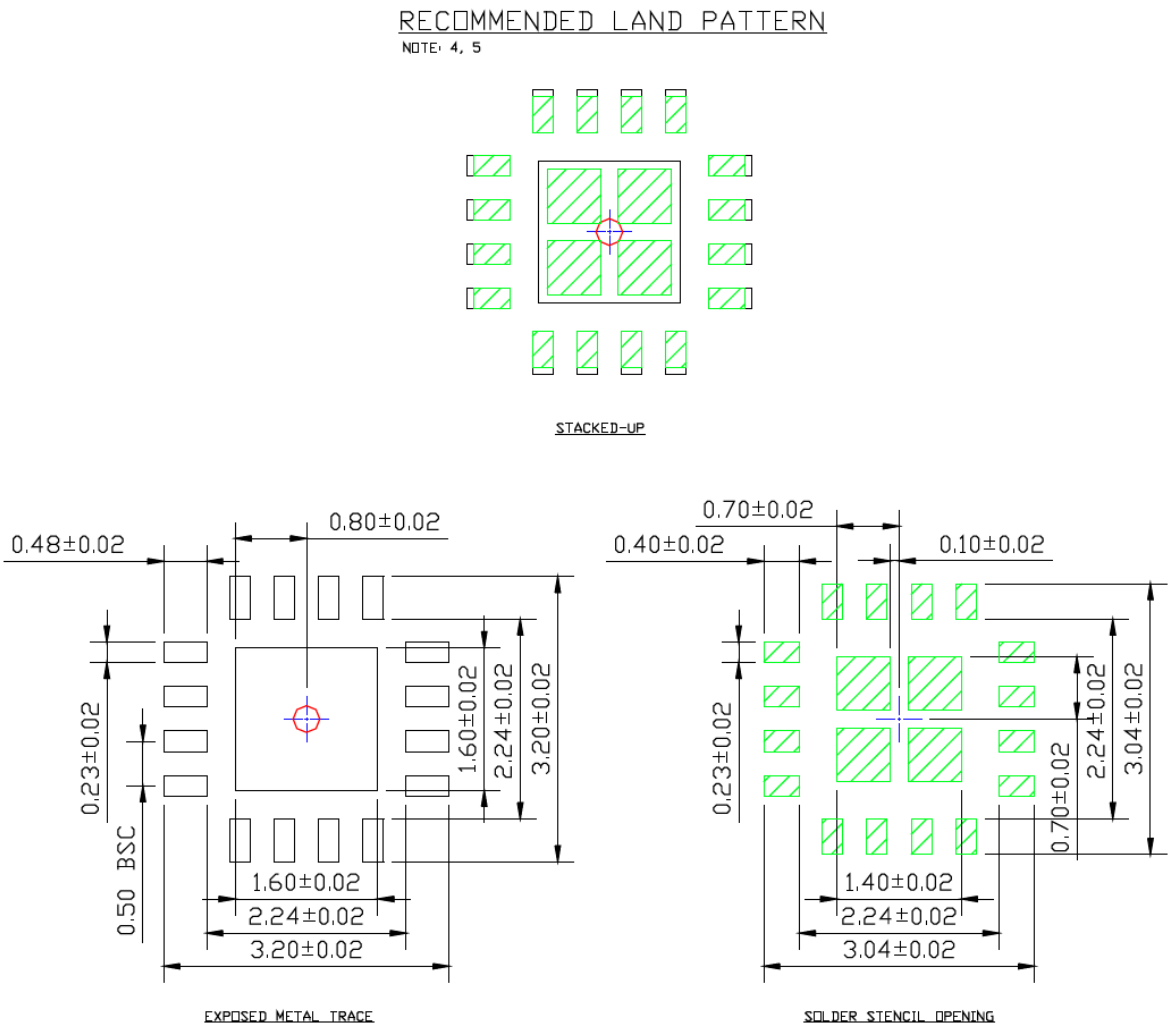


SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern drawing # QFN33-16LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2020)

- Converted Micrel document SY58012U to Microchip data sheet template DS20006319A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	XX
Device	Supply Voltage	Package	Temperature Range	Tape and Reel

Device:	SY58012:	5 GHz 1:2 LVPECL 1:2 Fanout Buffer/ Translator with Internal Input Termination	
Supply Voltage:	U	=	2.5V/3.3V
Package:	M	=	3 mm x 3 mm QFN-16 (NiPdAu Lead-Free)
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) SY58012UMG: SY58012, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 100/Tube

b) SY58012UMG-TR: SY58012, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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