SUP90N08-7m7P

Vishay Siliconix



SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{DS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	75			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		4.5	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}$			1	μА
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$			250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	70			Α
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0063	0.0077	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.0100	0.0125	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		43		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		4250		pF
Output Capacitance	C _{oss}			580		
Reverse Transfer Capacitance	C _{rss}			230		
Total Gate Charge ^c	Q_g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 50 A		69	105	nC
Gate-Source Charge ^c	Q _{gs}			23		
Gate-Drain Charge ^c	Q_{gd}			21		
Gate Resistance	R _g	f = 1 MHz		1.2	2.4	Ω
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 30 \text{ V, } R_L = 0.6 \ \Omega$ $I_D \cong 50 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \ \Omega$		17	30	ns
Rise Time ^c	t _r			5	10	
Turn-Off Delay Time ^c	t _{d(off)}			22	40	
Fall Time ^c	t _f			6	15	
Source-Drain Diode Ratings and Ch	aracteristics 7	_C = 25 °C ^b				
Continuous Current	Is				90	A
Pulsed Current	I _{SM}				180	
Forward Voltage ^a	V_{SD}	I _F = 20 A, V _{GS} = 0 V		0.83	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 75 A, dl/dt = 100 A/μs		65	100	ns
Peak Reverse Recovery Current	I _{RM(REC)}			2.5	5	Α
Reverse Recovery Charge	Q _{rr}			85	150	nC

Notes:

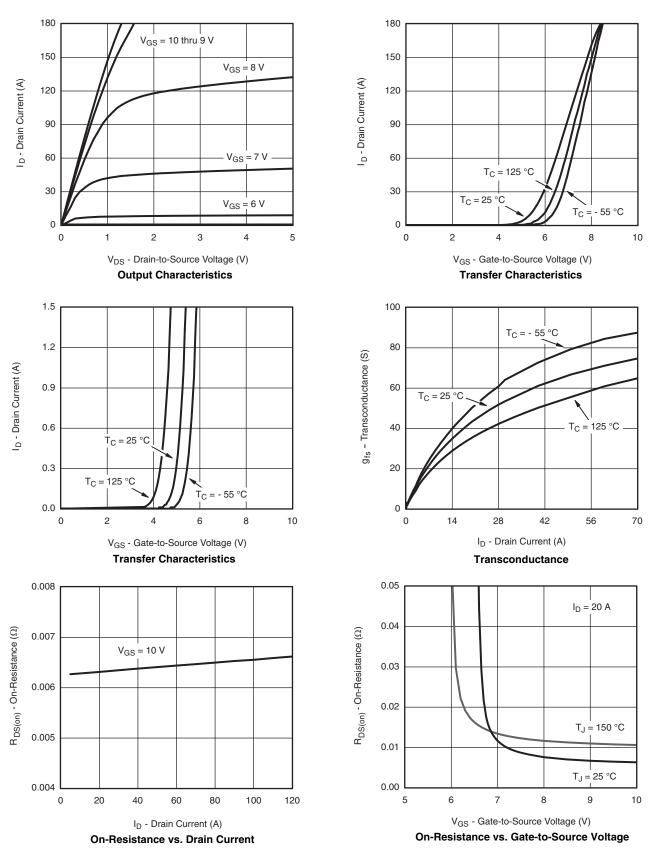
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- $\ \ \, \text{c. Independent of operating temperature.}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

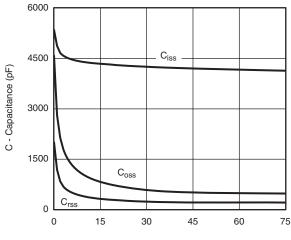


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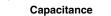
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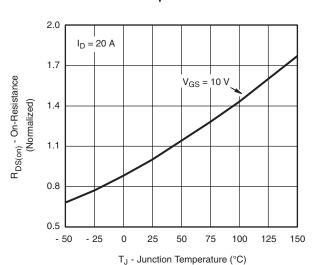
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

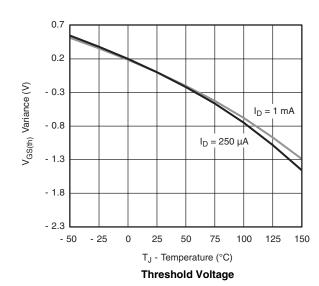


 $V_{\mbox{\footnotesize DS}}$ - Drain-to-Source Voltage (V)

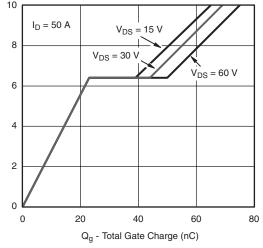




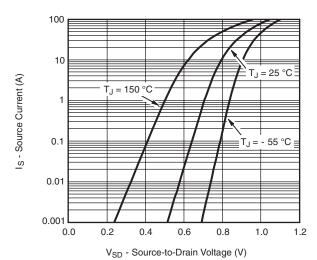
On-Resistance vs. Junction Temperature



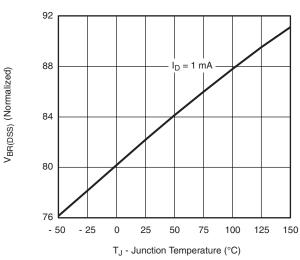
V_{GS} - Gate-to-Source Voltage (V)



Gate Charge



Source-Drain Diode Forward Voltage

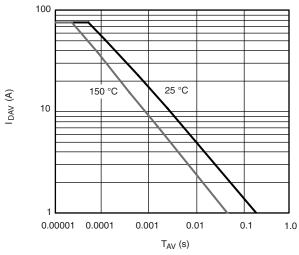


On-Resistance vs. Junction Temperature

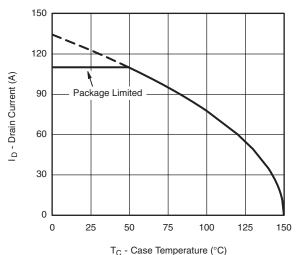


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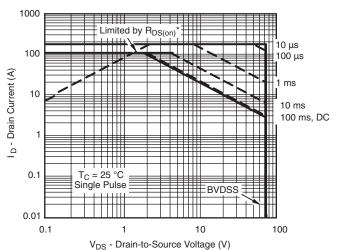
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Single Pulse Avalanche Current Capability vs. Time

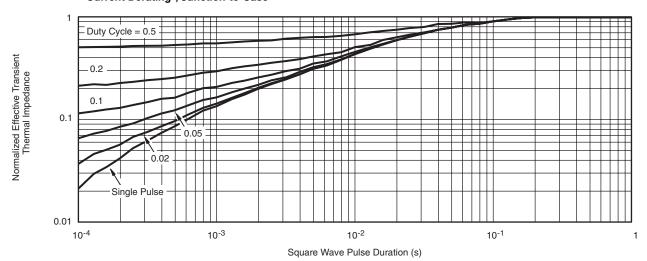


Current Derating*, Junction-to-Case



* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified **Safe Operating Area, Junction-to-Case**

 * The power dissipation P_D is based on $T_{J(max)}=150\,^{\circ}\text{C},$ using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

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