

Contents

1	Internal block diagram and pin configuration	3
2	Electrical ratings	5
2.1	Absolute maximum ratings	5
2.2	Thermal data	6
3	Electrical characteristics	7
3.1	Control part	9
3.1.1	NTC thermistor	11
3.2	Waveform definitions	12
4	Applications information	13
4.1	Recommendations	14
5	Package information	15
5.1	SDIP-25L package information	15
5.2	Packing information	17
6	Revision history	18

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

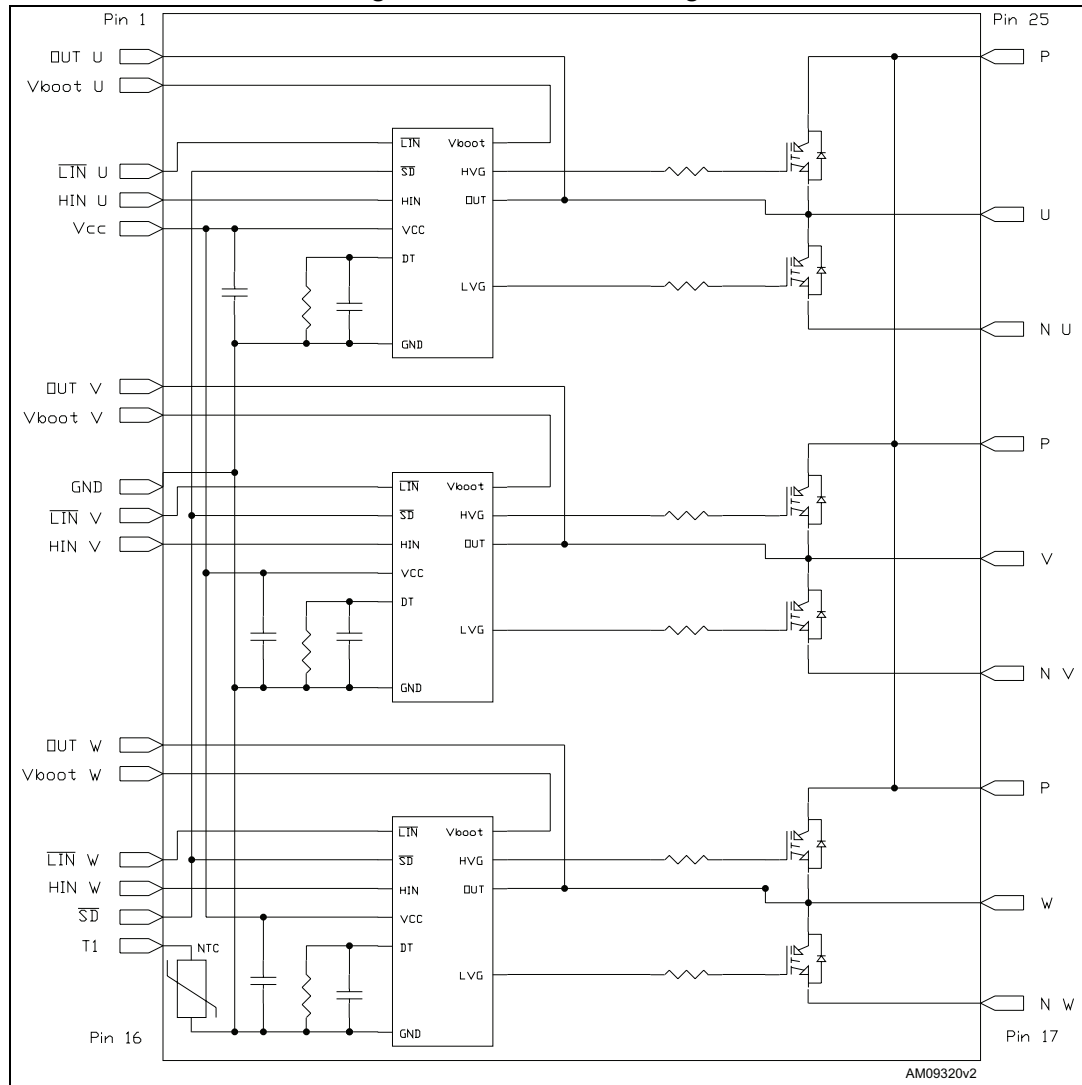
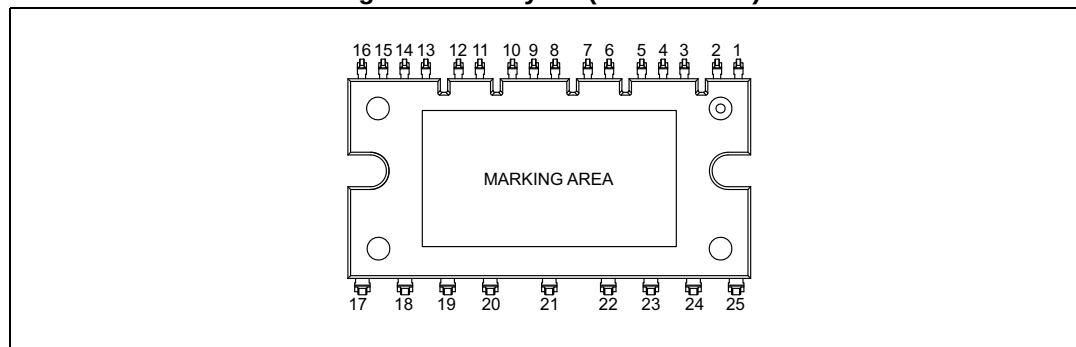


Table 2. Pin description

Pin n°	Symbol	Description
1	OUT _U	High side reference output for U phase
2	V _{boot U}	Bootstrap voltage for U phase
3	LIN _U	Low side logic input for U phase
4	HIN _U	High side logic input for U phase
5	V _{CC}	Low voltage power supply
6	OUT _V	High side reference output for V phase
7	V _{boot V}	Bootstrap voltage for V phase
8	GND	Ground
9	LIN _V	Low side logic input for V phase
10	HIN _V	High side logic input for V phase
11	OUT _W	High side reference output for W phase
12	V _{boot W}	Bootstrap voltage for W phase
13	LIN _W	Low side logic input for W phase
14	HIN _W	High side logic input for W phase
15	SD	Shut down logic input (active low)
16	T1	NTC thermistor terminal
17	N _W	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N _V	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N _U	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U , N_V , N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - N_U , N_V , N_W	500	V
V_{CES}	Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$)	600	V
$\pm I_C^{(2)}$	Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$	14	A
$\pm I_{CP}^{(3)}$	Each IGBT pulsed collector current	30	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25^\circ\text{C}$	42	W
t_{scw}	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN(1)} = 0 \div 5\text{ V}$	5	μs

1. Applied between HIN_i , $\overline{LIN}_i$ and G_{ND} for $i = U, V, W$
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied between OUT_U , OUT_V , OUT_W - GND	$V_{boot} - 21$	$V_{boot} + 0.3$	V
V_{CC}	Low voltage power supply	- 0.3	21	V
V_{CIN}	Comparator input voltage	- 0.3	$V_{CC} + 0.3$	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{IN}	Logic input voltage applied between HIN , $\overline{LIN}$ and GND	- 0.3	15	V
V_{SD}	SD voltage	- 0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$)	2500	V
T_C	Module case operation temperature	-40 to 125	$^\circ\text{C}$
T_J	Power chips operating junction temperature	-40 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT	3	°C/W
	Thermal resistance junction-case single diode	5.5	°C/W

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 7\text{ A}$	-	2.1	2.5	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 7\text{ A}$, $T_J = 125\text{ °C}$	-	1.8		
I_{CES}	Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$	-		150	μA
V_F	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 7\text{ A}$	-		2.1	V
Inductive load switching time and energy						
t_{on}	Turn-on time	$V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 7\text{ A}$ (see Figure 5)	-	270	-	ns
$t_{c(on)}$	Crossover time (on)		-	130	-	
t_{off}	Turn-off time		-	520	-	
$t_{c(off)}$	Crossover time (off)		-	140	-	
t_{rr}	Reverse recovery time		-	130	-	
E_{on}	Turn-on switching losses		-	150	-	μJ
E_{off}	Turn-off switching losses		-	110	-	

1. Applied between HIN_i , $\overline{LIN_i}$ and G_{ND} for $i = U, V, W$ ($\overline{LIN}$ inputs are active-low).

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

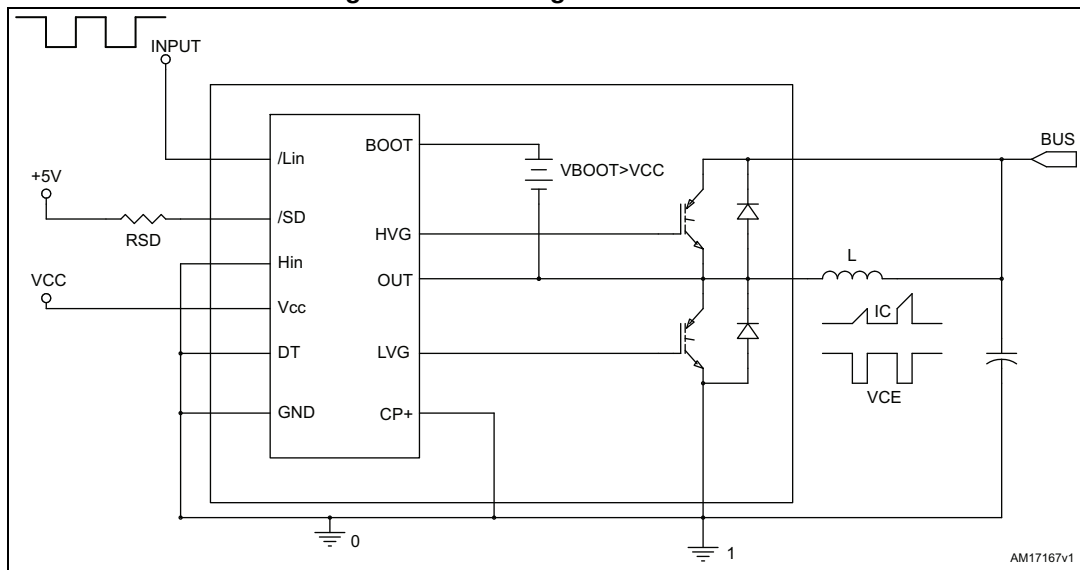
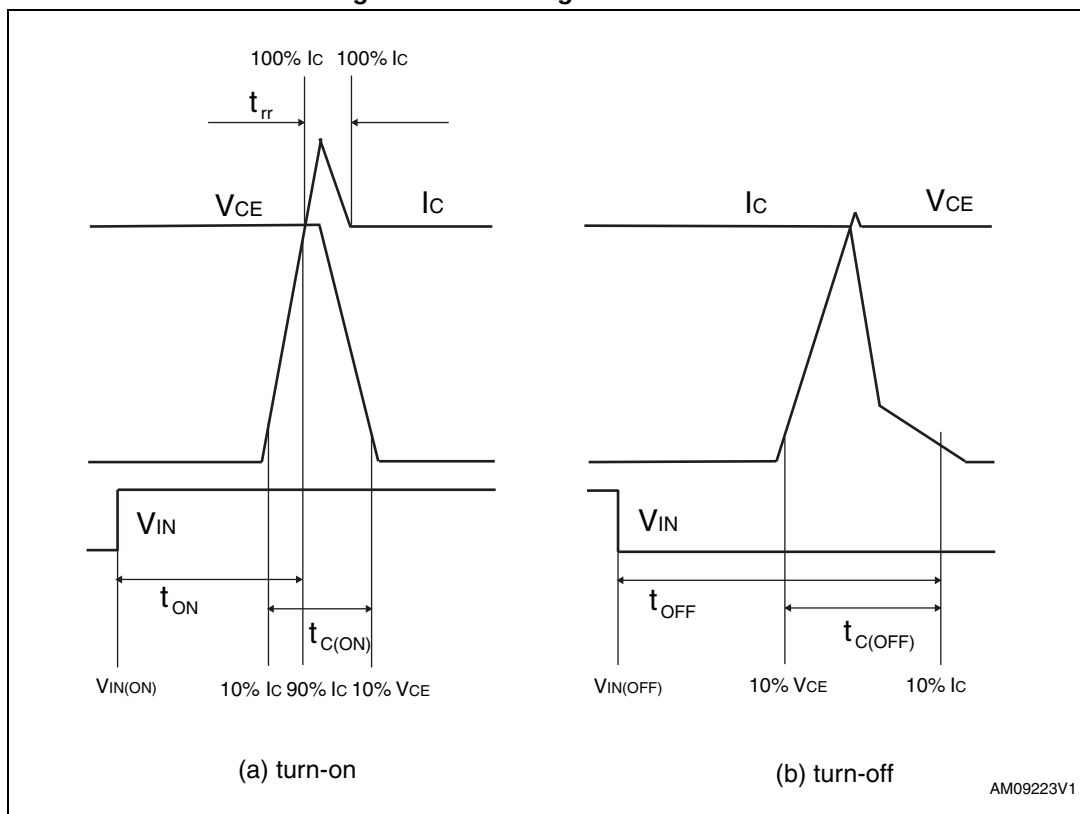


Figure 4. Switching time definition



Note: *Figure 4: Switching time definition* refers to HIN inputs (active high). For $\overline{\text{LIN}}$ inputs (active low), V_{IN} polarity must be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $H_{IN} = 0$			450	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$ $H_{IN} = 0$			3.5	mA

Table 9. Bootstrapped voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	$V_{BS} < 9\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN}$ and $H_{IN} = 5\text{ V}$		70	110	μA
I_{QBS}	V_{BS} quiescent current	$V_{BS} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN}$ and $H_{IN} = 5\text{ V}$		200	300	μA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage		0.8		1.1	V
V_{ih}	High logic level voltage		1.9		2.25	V
I_{HINh}	HIN logic "1" input bias current	$H_{IN} = 15\text{ V}$	110	175	260	μA
I_{HINl}	HIN logic "0" input bias current	$H_{IN} = 0\text{ V}$			1	μA
I_{LINl}	$\overline{LIN}$ logic "1" input bias current	$\overline{LIN} = 0\text{ V}$	3	6	20	μA
I_{LINh}	$\overline{LIN}$ logic "0" input bias current	$\overline{LIN} = 15\text{ V}$			1	μA
I_{SDh}	$\overline{SD}$ logic "0" input bias current	$\overline{SD} = 15\text{ V}$	30	120	300	μA
I_{SDl}	$\overline{SD}$ logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	μA
Dt	Dead time	see Figure 9		600		ns

Table 11. Shut down characteristics ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{sd}	Shut down to high / low side driver propagation delay	$V_{OUT} = 0$, $V_{boot} = V_{CC}$, $V_{IN} = 0$ to 3.3 V	50	125	200	ns

Table 12. Truth table

Condition	Logic input (V_I)			Output	
	$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 "logic state" half-bridge tri-state	H	H	L	L	L
1 "logic state" low side direct driving	H	L	L	H	L
1 "logic state" high side direct driving	H	H	H	L	H

Note: X: don't care

Figure 5. Maximum $I_{C(RMS)}$ current vs. switching frequency ⁽¹⁾

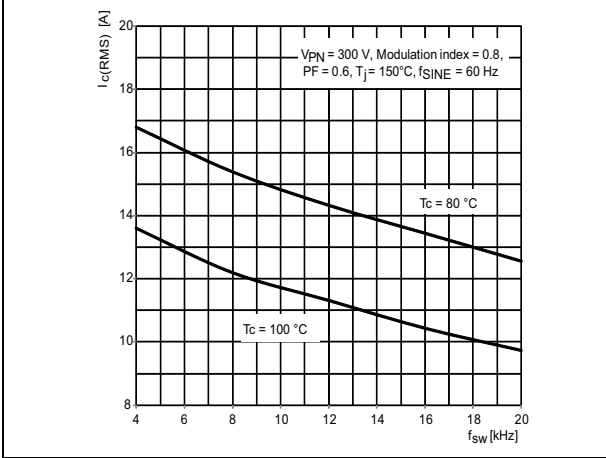
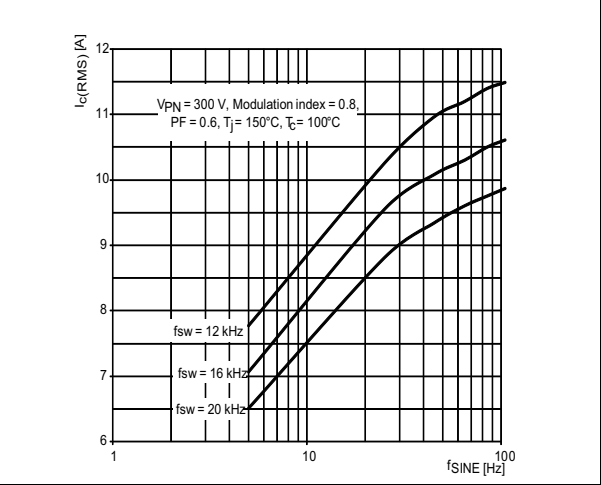


Figure 6. Maximum $I_{C(RMS)}$ current vs. f_{SINE} ⁽¹⁾



1. Simulated curves refer to typical IGBT parameters and maximum R_{thj-c} .

3.1.1 NTC thermistor

Table 13. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R ₂₅	Resistance	T = 25°C		4.7		kΩ
R ₁₂₅	Resistance	T = 125°C		160		Ω
B	B-constant	T = 25°C to 85°C		3950		K
T	Operating temperature		-40		150	°C

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where T are temperatures in Kelvins

Figure 7. NTC resistance vs. temperature

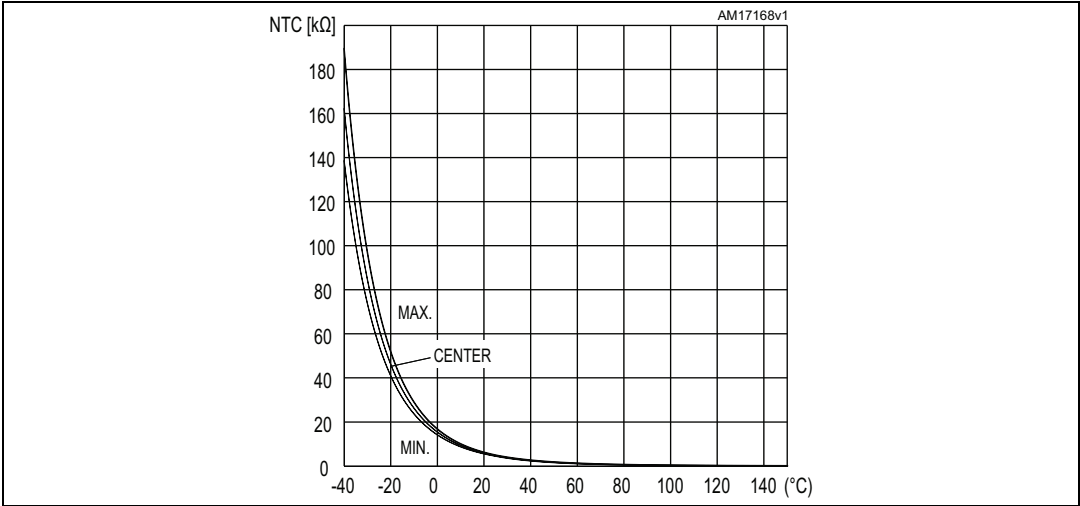
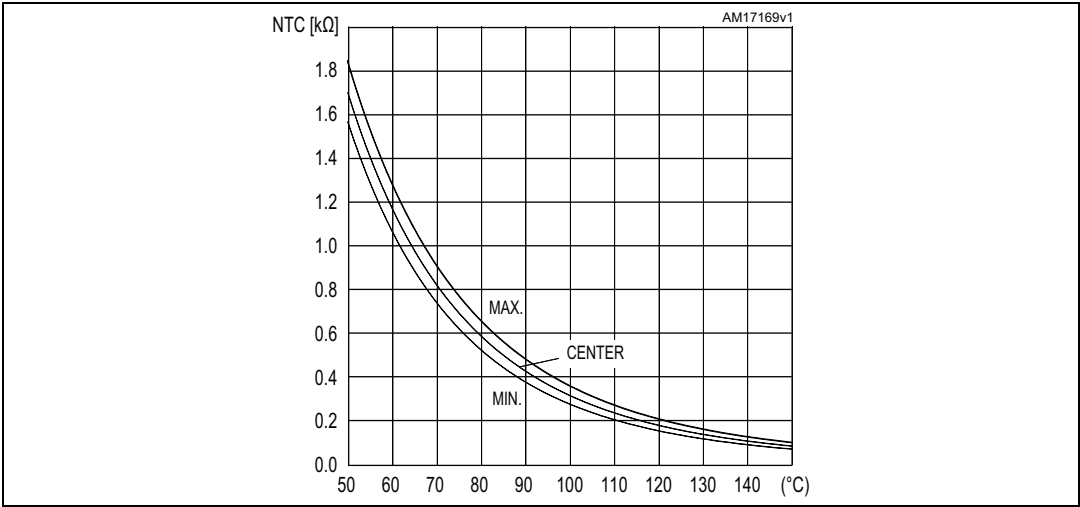
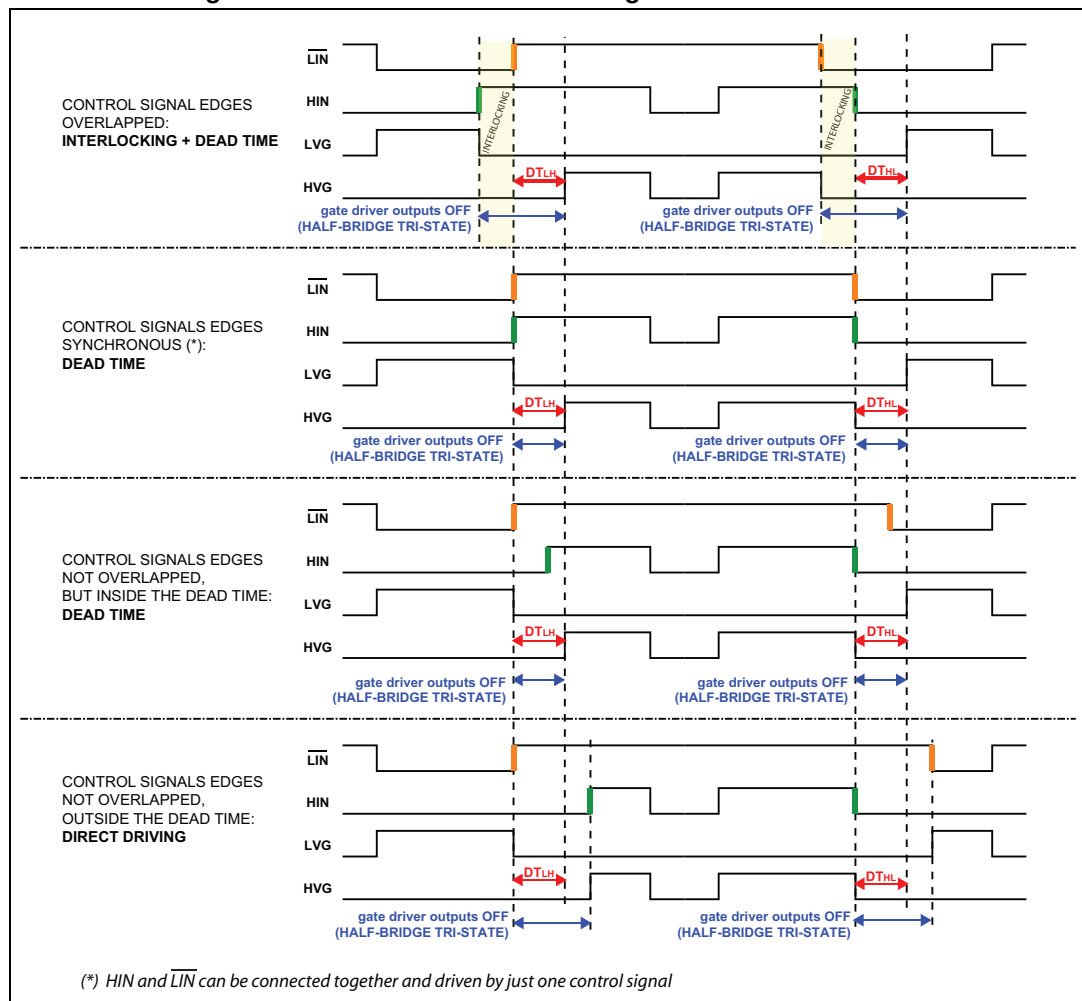


Figure 8. NTC resistance vs. temperature (zoom)



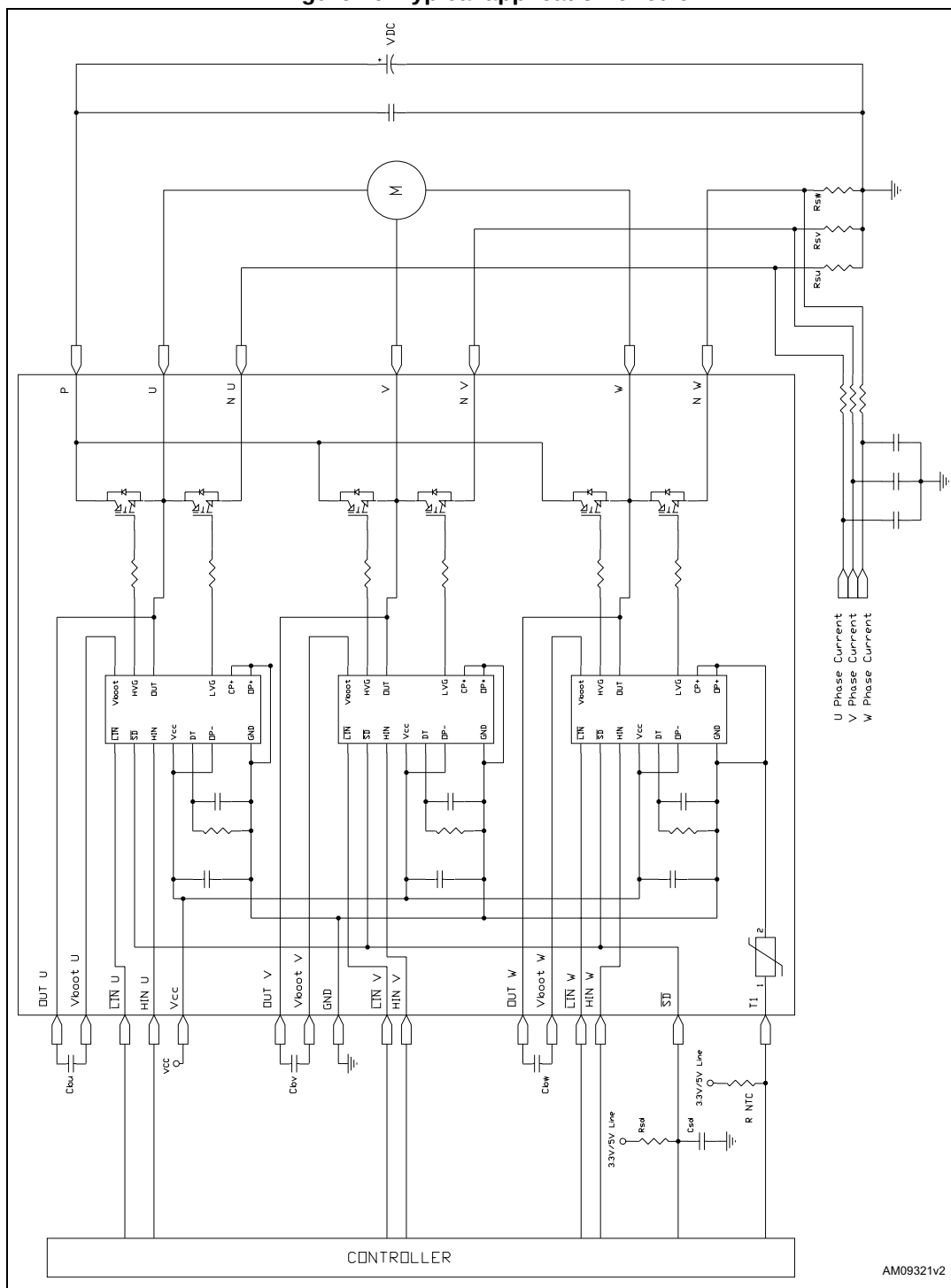
3.2 Waveform definitions

Figure 9. Dead time and interlocking waveform definitions



4 Applications information

Figure 10. Typical application circuit



4.1 Recommendations

- Input signal HIN is active high logic. A 85 k Ω (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- Input signal /LIN is active low logic. A 720 k Ω (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{SD}$ signal should be pulled up to 5 V / 3.3 V with an external resistor.

Table 14. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V _{PN}	Supply Voltage	Applied between P-Nu, Nv, Nw		300	400	V
V _{CC}	Control supply voltage	Applied between V _{CC} -GND	13.5	15	18	V
V _{BS}	High side bias voltage	Applied between V _{BOOTi} -OUT _i for i = U, V, W	13		18	V
t _{dead}	Blanking time to prevent Arm-short	For each input signal	1			μ s
f _{PWM}	PWM input signal	-40°C < T _C < 100°C -40°C < T _J < 125°C			20	kHz
T _C	Case operation temperature				100	°C

Note: For further details, refer to AN3338.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

5.1 SDIP-25L package information

Figure 11. SDIP-25L package outline

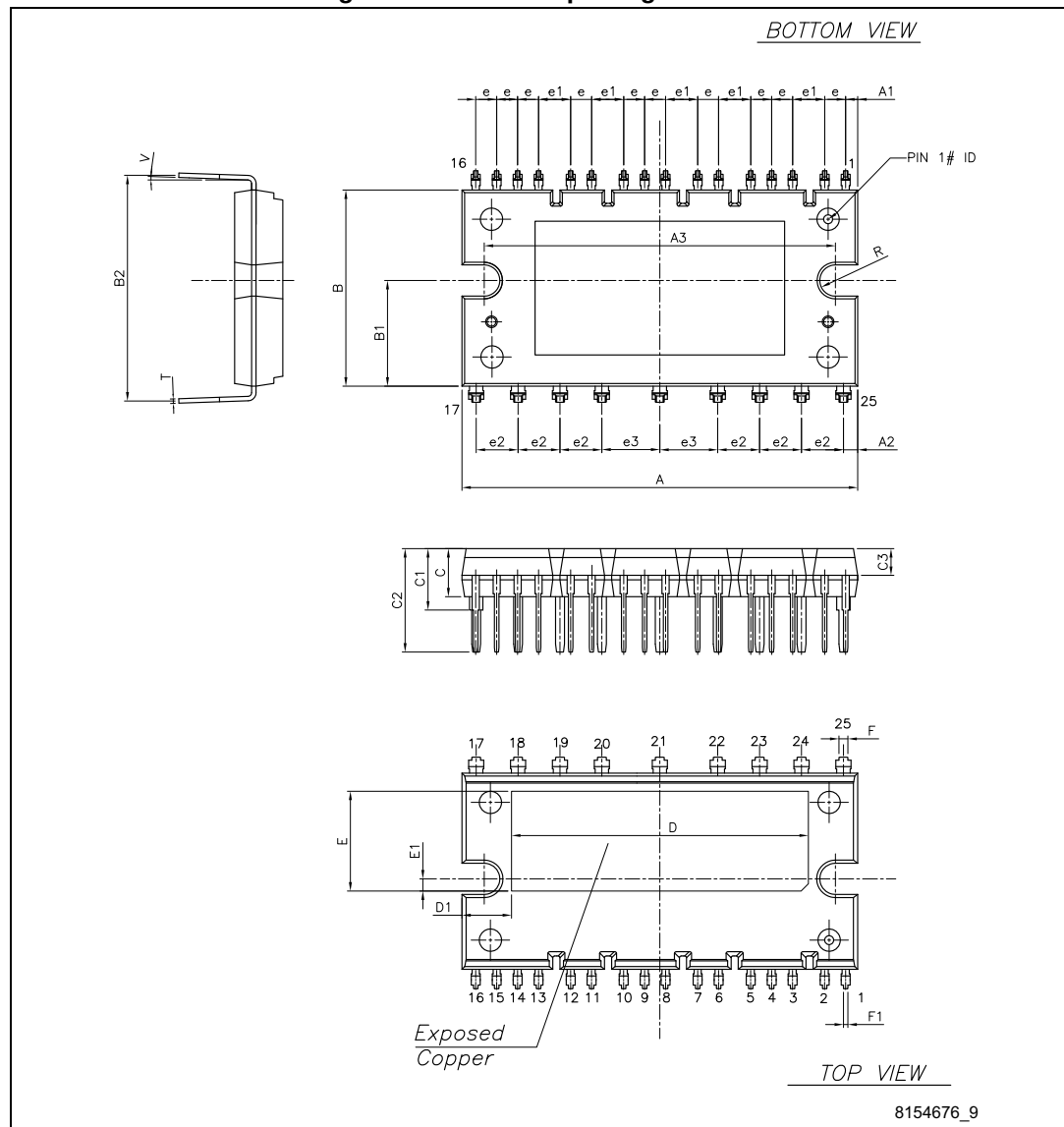
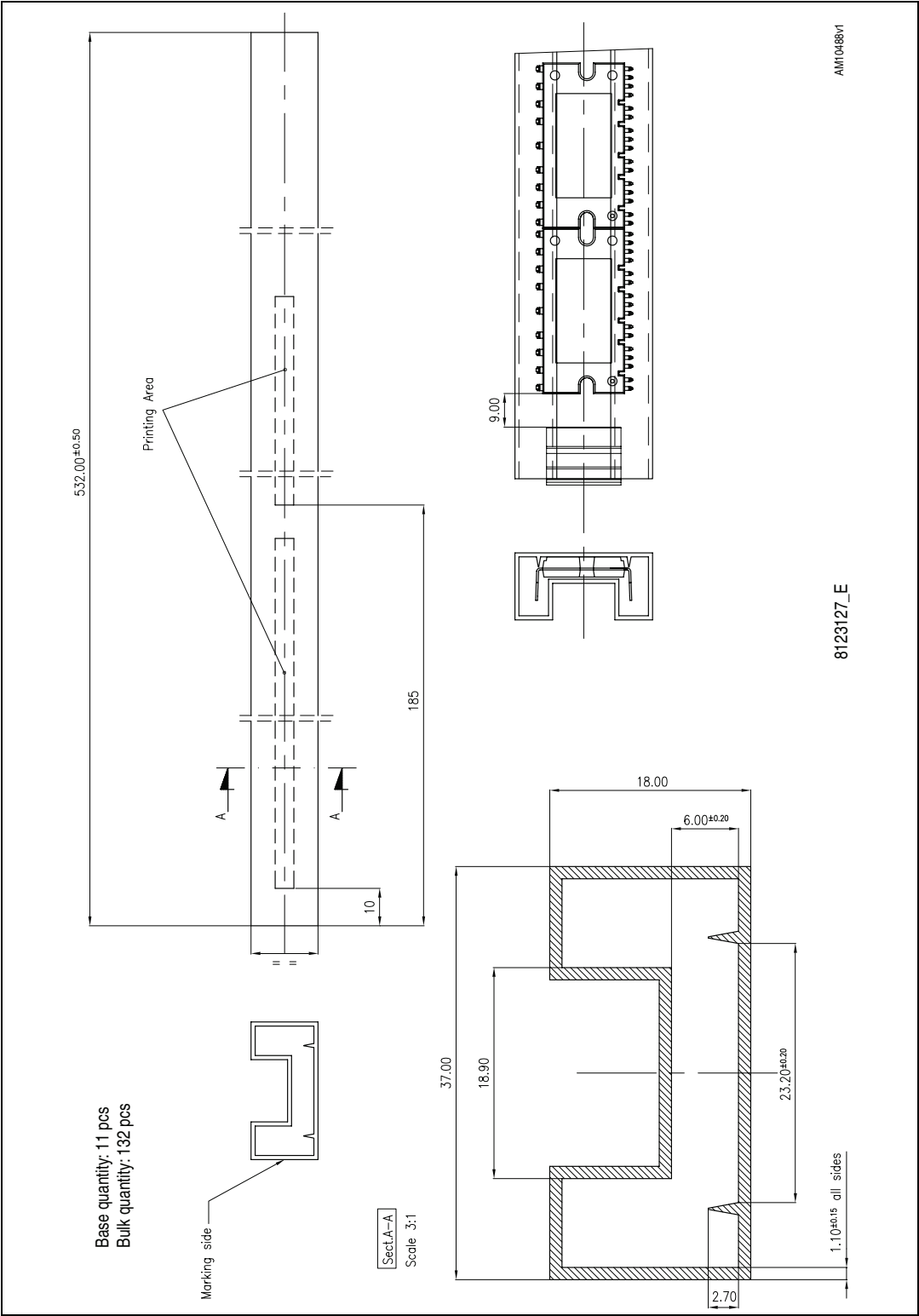


Table 15. SDIP-25L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	43.90	44.40	44.90
A1	1.15	1.35	1.55
A2	1.40	1.60	1.80
A3	38.90	39.40	39.90
B	21.50	22.00	22.50
B1	11.25	11.85	12.45
B2	24.83	25.23	25.63
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	11.20	11.70	12.20
C3	2.90	3.00	3.10
e	2.15	2.35	2.55
e1	3.40	3.60	3.80
e2	4.50	4.70	4.90
e3	6.30	6.50	6.70
D		33.30	
D1		5.55	
E		11.20	
E1		1.40	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

5.2 Packing information

Figure 12. SDIP-25L packing information (dimensions are in mm.)



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
07-Mar-2011	1	Initial release.
14-Sep-2011	2	Update Section 3.1.1 on page 11 .
28-Aug-2012	3	Modified: Min. and Max. value Table 4 on page 5 . Updated: Table 15 on page 15 , Figure 11 on page 15 , Figure 12 on page 17 . Added: Figure 13 on page 18 .
15-May-2013	4	Modified: description pin 15 Table 2 on page 4 and V_{SD} parameter Table 4 on page 5 .
15-Apr-2015	5	Text edits and formatting changes throughout document Updated Figure 2: Pin layout (bottom view) Updated Section 5: Package information

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